M16C/63, 64A, 65, and 65C Groups

Remote Control Signal Receiver Setting by Format Type

R01AN0390EJ0100
Rev. 1.00
Dec. 28, 2010

Abstract

This document describes remote control signal reception by format type for the M16C/63, 64A, 65, and 65C Groups.

Products

MCUs: M16C/63, 64A, 65, and 65C Groups

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Remote Control Signal Receive Waveform

This application note describes the six format waveforms shown in Figure 1.1 to Figure 1.6 as the receive operation example using PMC0 circuit and PMC1 circuit pattern match mode.

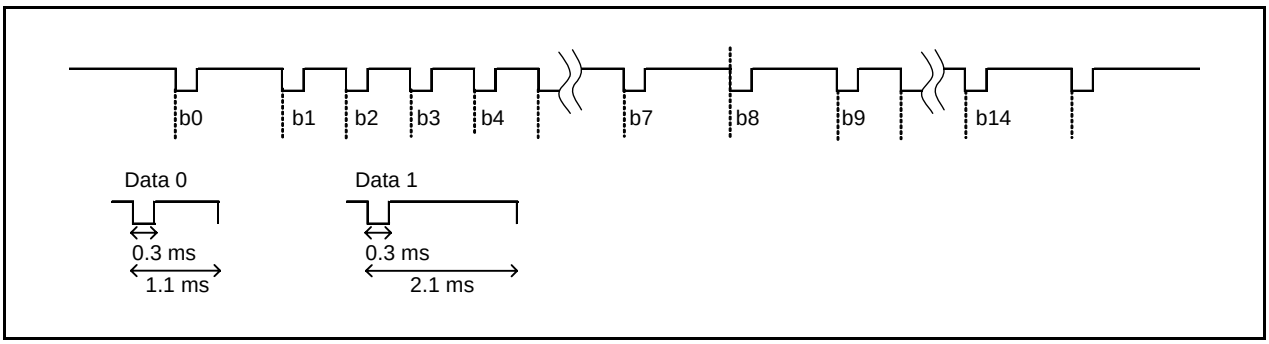


Figure 1.1 Pattern 1: Remote Control Format without Header Pattern

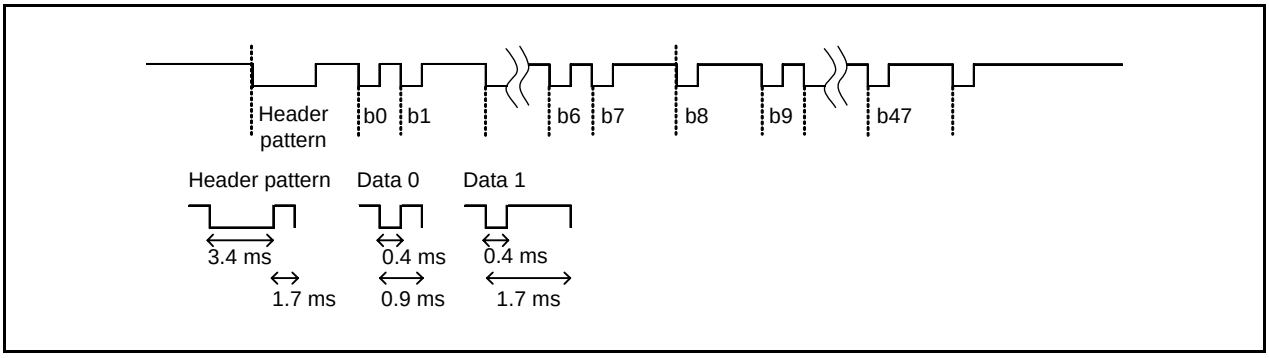


Figure 1.2 Pattern 2: Remote Control Format with Header Pattern

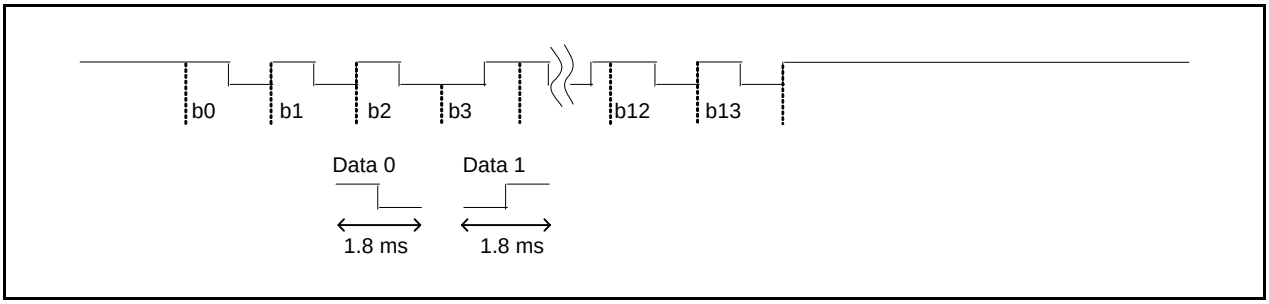


Figure 1.3 Pattern 3: Bi-Phase Remote Control Format

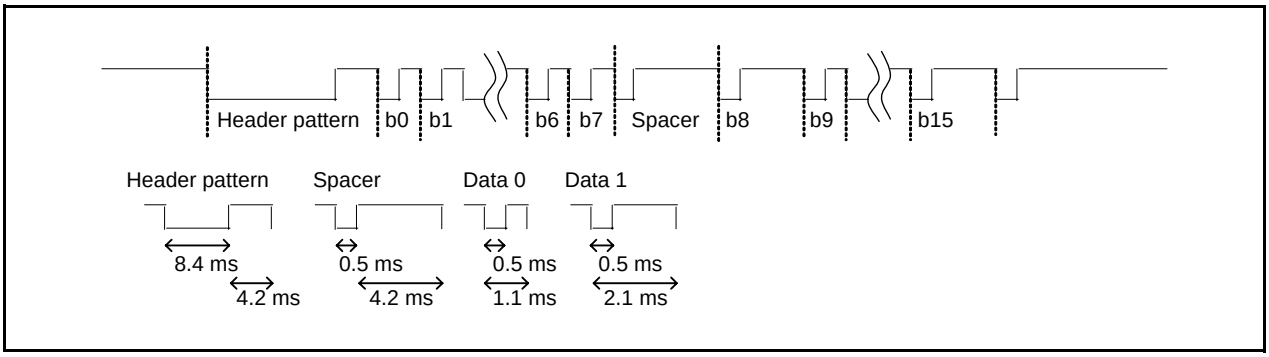


Figure 1.4 Pattern 4: Remote Control Format with Header Pattern and Spacer

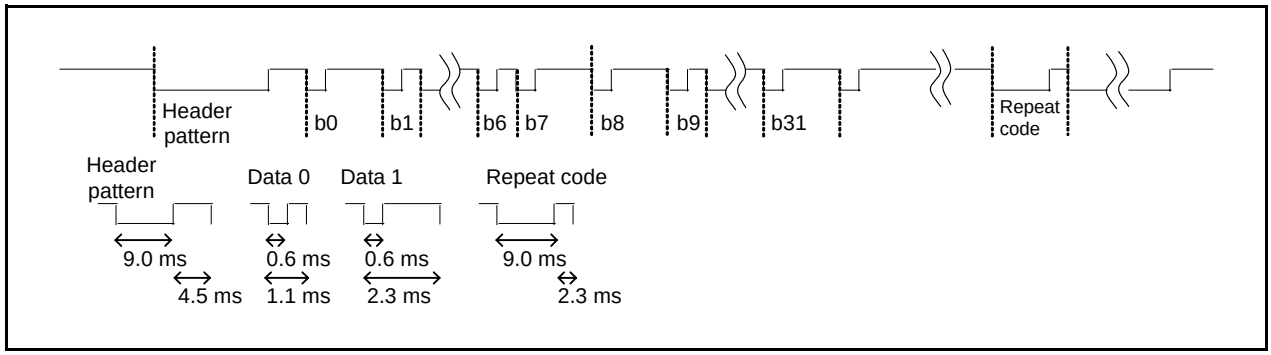


Figure 1.5 Pattern 5: Remote Control Format with Header Pattern and Repeat Code

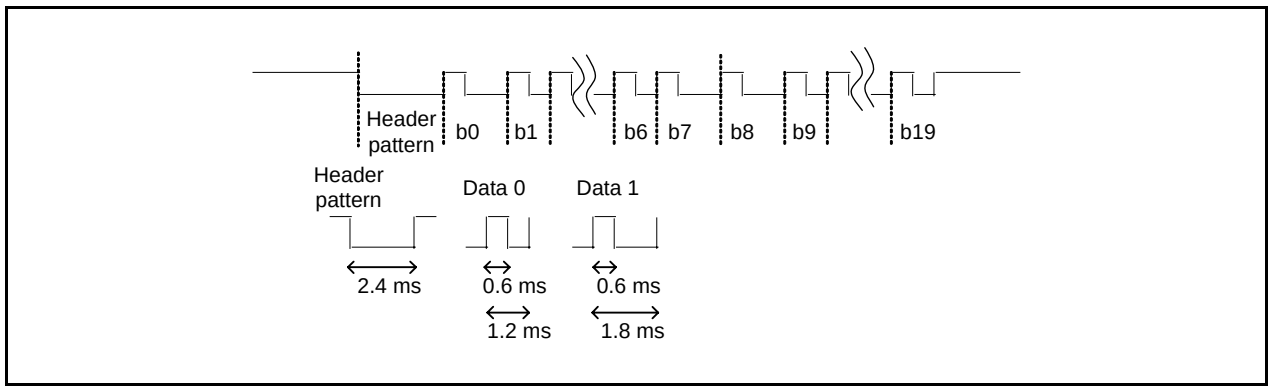


Figure 1.6 Pattern 6: Remote Control Format with Special Header Pattern

Table 1.1 lists the Reception in Pattern Match Operation Corresponding Circuit.

Table 1.1 Reception in Pattern Match Operation Corresponding Circuit

Pattern	PMC0 Independent Operation	PMC1 Independent Operation	PMC0/PMC1 Combined Operation
Pattern 1	See 3.1. (1)	See 4.1. (1)	Not needed
Pattern 2	See 3.2. (1)	See 4.2. (1)	Not needed
Pattern 3	Not needed	See 4.3. (1)	Not needed
Pattern 4	See 6. (2)	See 6. (2)	See 5.1. (1)
Pattern 5	See 6. (2)	See 6. (2)	See 5.2. (3)
Pattern 6	See 3.3. (1)	Not needed	Not needed

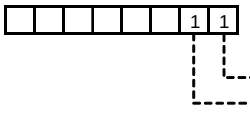
Notes:
1. Available without timer measure interrupt (low software process load).
2. Available by software processed pulse width analysis with timer measure interrupt (causes software process load for pulse width analysis).
3. Another timer is used for the repeat code.

2. Remote Control Signal Receiver Initialization

To enable the remote control signal receiver, follow the procedure below to set the registers.
This procedure will set the “Sub Clock Control” and “Enabling Remote Control Signal Receive Interrupt”.

Sub Clock Setting for the M16C/64A, 65, and 65C Groups

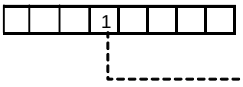
Protect Register



Symbol	Address
PRCR	000Ah

Bit Symbol	Bit Name	Function
PRC0	Protect bit 0	1: CM0 register write enabled
PRC1	Protect bit 1	1: PM2 register write enabled

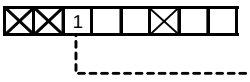
System Clock Control Register 0



Symbol	Address
CM0	0006h

Bit Symbol	Bit Name	Function
CM04	Port XC select bit	1: XCIN-XCOUT oscillation function

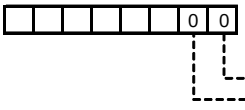
Processor Mode Register 2



Symbol	Address
PM2	001Eh

Bit Symbol	Bit Name	Function
PM25	Peripheral clock fC provide bit	1: Provided

Protect Register

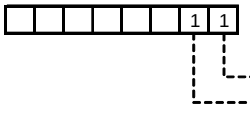


Symbol	Address
PRCR	000Ah

Bit Symbol	Bit Name	Function
PRC0	Protect bit 0	0: CM0 register write protected
PRC1	Protect bit 1	0: PM2 register write protected

Sub Clock Setting for the M16C/63 Group

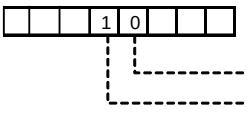
Protect Register



Symbol	Address
PRCR	000Ah

Bit Symbol	Bit Name	Function
PRC0	Protect bit 0	1: CM0 register write enabled
PRC1	Protect bit 1	1: PM2 register write enabled

System Clock Control Register 0

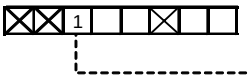


Symbol	Address
CM0	0006h

Bit Symbol	Bit Name	Function
CM03	XCIN clock stop bit	0: On
CM04	Port XC select bit	1: XCIN-XCOUT oscillation function

The CM03 bit becomes 1 (off) while the CM04 bit is 0 (P8_6, P8_7 are input ports).

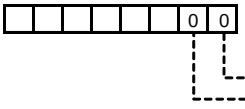
Processor Mode Register 2



Symbol	Address
PM2	001Eh

Bit Symbol	Bit Name	Function
PM25	Peripheral clock fC provide bit	1: Provided

Protect Register

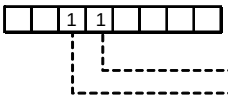


Symbol	Address
PRCR	000Ah

Bit Symbol	Bit Name	Function
PRC0	Protect bit 0	0: CM0 register write protected
PRC1	Protect bit 1	0: PM2 register write protected

Enabling the Remote Control Signal Receive interrupt

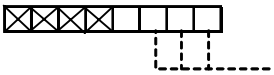
Interrupt Factor Select Register 2



Symbol	Address
IFSR2A	0206h

Bit Symbol	Bit Name	Function
IFSR24	Interrupt request source select bit	1: Remote control 0
IFSR25	Interrupt request source select bit	1: Remote control 1

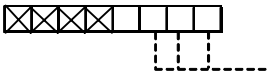
Interrupt Control Register 0



Symbol	Address
PMC0IC	0071h

Bit Symbol	Bit Name	Function
ILVL2 to ILVL0	Interrupt priority level select bit	000: Level 0 (interrupt disabled) 001: Level 1 010: Level 2 011: Level 3 100: Level 4 101: Level 5 110: Level 6 111: Level 7

Interrupt Control Register 1



Symbol	Address
PMC1IC	0072h

Bit Symbol	Bit Name	Function
ILVL2 to ILVL0	Interrupt priority level select bit	000: Level 0 (interrupt disabled) 001: Level 1 010: Level 2 011: Level 3 100: Level 4 101: Level 5 110: Level 6 111: Level 7

3. Individual Operation of the PMC0 Circuit in Pattern Match Mode

3.1 Remote Control Signal Reception without Header Pattern

Figure 3.1 shows how to receive the remote control signal when using the pattern match mode of the PMC0 circuit.

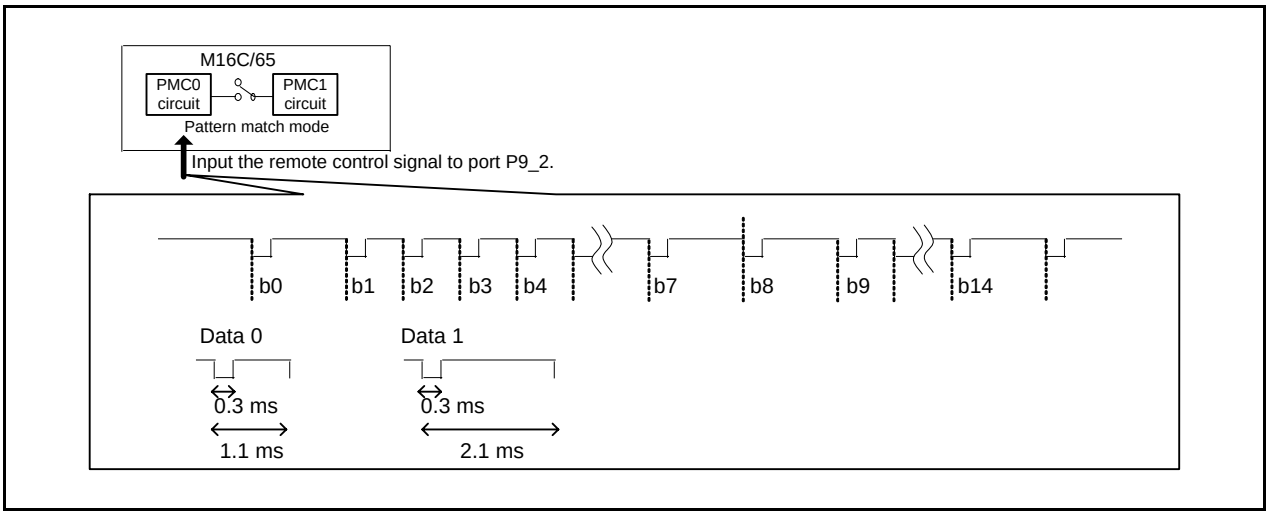


Figure 3.1 Outline of the Remote Control Format without Header Pattern

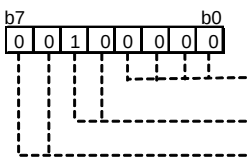
The detection pattern is designed to accept a tolerance of ±10% from the format width shown in Figure 3.1. See the following table for settings.

Table 3.1 PMC0 Circuit Settings

Item		Description
Count sources	Clock source	fC
	Division	No division
Operation mode		Pattern match mode
Pattern match mode	Detect patterns	Data 0 or data 1 match
	Interrupt request generation timing	Completion of data reception
	Selectable functions	Input signal inversion
		Digital filter
		Error flag hold
Input port		P9_2

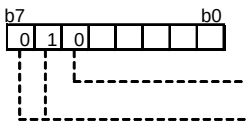
Register Settings

PMC0 Function Select Register 3



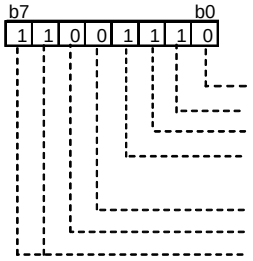
Symbol	Address	
PMC0CON3	01F3h	
Bit Symbol	**Bit Name**	**Function**
PD/CST/CFR/CRE	Mode select bit	0000: Pattern match mode
CSRC1 to CSRC0	Clock source select bit	10: fC
CDIV1 to CDIV0	Count source divisor select bit	00: No division

PMC0 Function Select Register 2



Symbol	Address	
PMC0CON2	01F2h	
Bit Symbol	**Bit Name**	**Function**
CEINT	Counter overflow interrupt enable bit	0: Disabled
PSEL1 to PSEL0	Input pin select bit	01: PMC0 pin

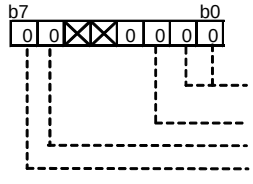
PMC0 Function Select Register 0



Symbol	Address
PMC0CON0	01F0h

Bit Symbol	Bit Name	Function
EN	PMC0 operation enable bit	0: Operation disabled
SINV	Input signal polarity invert bit	1: Inverted
FIL	Filter enable bit	1: Filter enabled
EHOLD	Error flag hold bit	Status of the REFLG bit in the PMC0STS register: 1: Held even after next data received
HDEN	Header pattern enable bit	0: Header disabled
SDEN	Special data pattern enable bit	0: Special data pattern disabled
DRINT1 to DRINT0	Receive interrupt control bit	11: Interrupt request is generated when compare match and no receive error occurs, and reception completed (1)

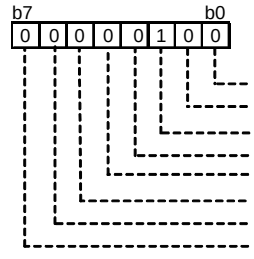
PMC0 Function Select Register 1



Symbol	Address
PMC0CON1	01F1h

Bit Symbol	Bit Name	Function
TYP1 to TYP0	Receive mode select bit	00: Period measurement (between rising edge and rising edge)
CSS	Counter start control bit	0: Counters operate individually
EXSDEN	Special pattern detect block select bit	0: PMC0
EXHDEN	Header pattern detect block select bit	0: PMC0

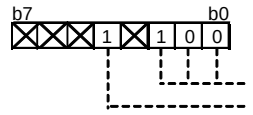
PMC0 Interrupt Source Register



Symbol	Address
PMC0INT	01F5h

Bit Symbol	Bit Name	Function
CPINT	Compare match flag interrupt enable bit	0: Disabled
REINT	Receive error flag interrupt enable bit	0: Disabled
DRINT	Data reception complete interrupt enable bit	1: Enabled
BFULINT	Receive buffer full flag interrupt enable bit	0: Disabled
PTHDINT	Header match flag interrupt enable bit	0: Disabled
PTDINT	Data 0/1 match flag interrupt enable bit	0: Disabled
TIMINT	Timer measure interrupt enable bit	0: Disabled
SDINT	Special data match flag interrupt enable bit	0: Disabled

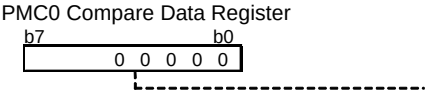
PMC0 Compare Control Register



Symbol	Address
PMC0CPC	01F6h

Bit Symbol	Bit Name	Function
CPN2 to CPN0	Compare bit specified bit	Bits 4 to 0 are compared
CPEN	Compare enable bit	1: Compare enabled

PMC0 Compare Data Register

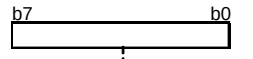


Symbol	Address
PMC0CPD	01F7h

Function: Compare with 00000b

See Note 2.

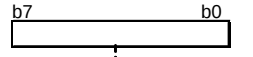
PMC0 Data 0 Pattern Set Register (MIN)



Symbol	Address
PMC0D0PMIN	D084h

Function: 1.1 [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 31

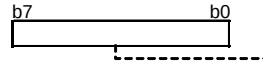
PMC0 Data 0 Pattern Set Register (MAX)



Symbol	Address
PMC0D0PMAX	D085h

Function: 1.1 [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 39

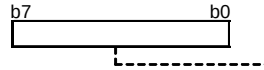
PMC0 Data 1 Pattern Set Register (MIN)



Symbol	Address
PMC0D1PMIN	D086h

Function: 2.1 [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 61

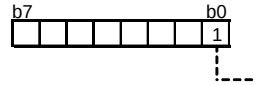
PMC0 Data 1 Pattern Set Register (MAX)



Symbol	Address
PMC0D1PMAX	D087h

Function: 2.1 [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 75

PMC0 Function Select Register 0



Symbol	Address
PMC0CON0	01F0h

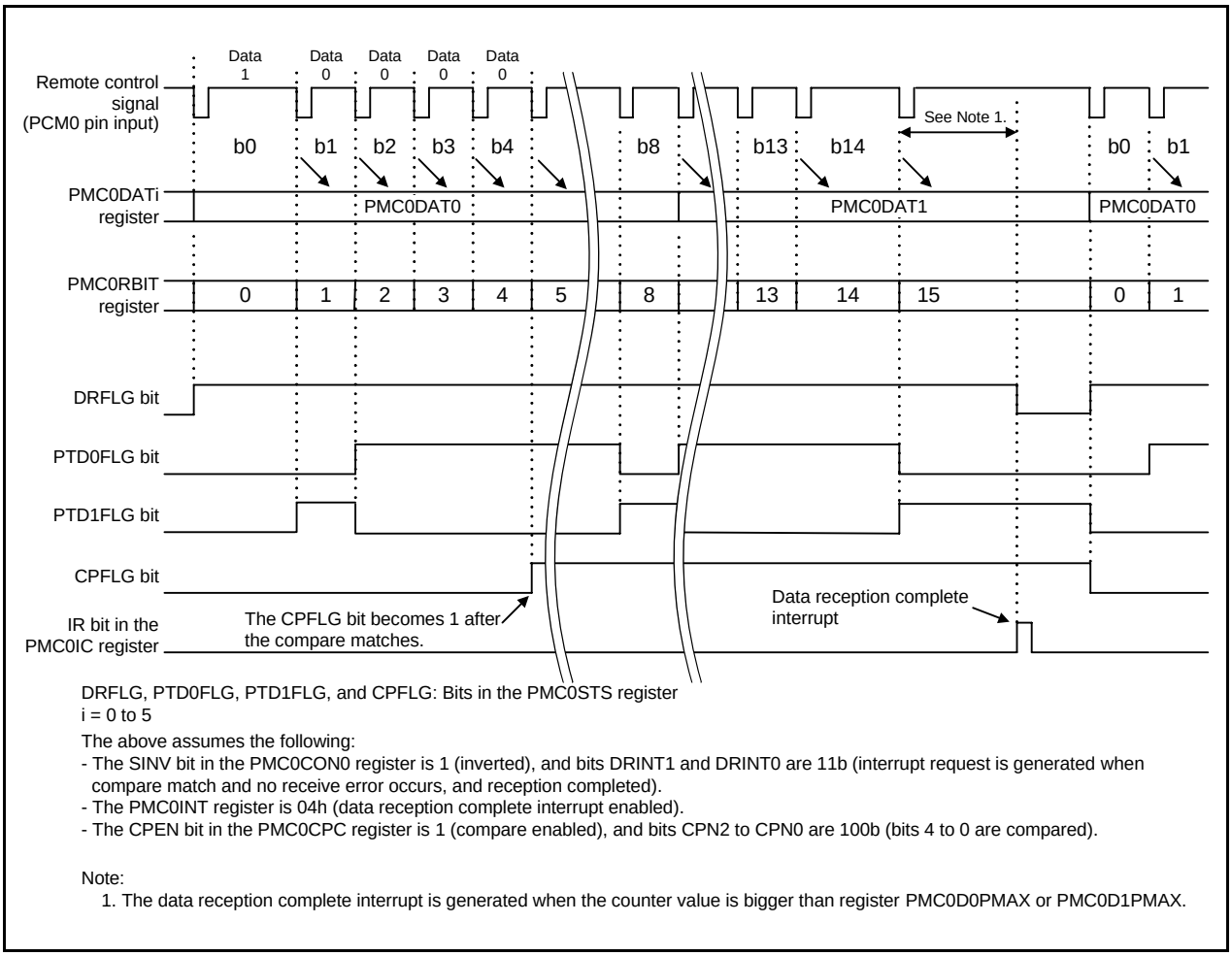
Bit Symbol	Bit Name	Function
EN	PMC0 operation enable bit	1: Operation enabled

Notes:
1. Set bits DRINT1 to DRINT0 to 00b when the compare match function is not used.
2. Set all bits to 0 when the compare match function is not used.
   Check the specification to set the compared value when the compare match function is used.

Operation

(1) The receive operation starts at the falling edge of b0 in the receive data.
(2) During the receive operation, the receive data is stored bit by bit in the PMC0DATi register (i = 0 to 5).
(3) After receiving the 15th bit, if there is no falling edge during the maximum time set to data 0 or data 1, a data reception complete interrupt is generated.
(4) Read registers PMC0DATi and PMC0RBIT in the data reception complete interrupt.

Figure 3.2 shows the condition of the status flags and the interrupt request generation timing of the PMC0 circuit in remote control reception.



DRFLG, PTD0FLG, PTD1FLG, and CPFLG: Bits in the PMC0STS register
i = 0 to 5

The above assumes the following:
- The SINV bit in the PMC0CON0 register is 1 (inverted), and bits DRINT1 and DRINT0 are 11b (interrupt request is generated when compare match and no receive error occurs, and reception completed).
- The PMC0INT register is 04h (data reception complete interrupt enabled).
- The CPEN bit in the PMC0CPC register is 1 (compare enabled), and bits CPN2 to CPN0 are 100b (bits 4 to 0 are compared).

Note:
1. The data reception complete interrupt is generated when the counter value is bigger than register PMC0D0PMAX or PMC0D1PMAX.

Figure 3.2 PMC0 Receive Operation of the Remote Control Format without Header Pattern

3.2 Receive Operation of the Remote Control Format with Header Pattern

Figure 3.3 shows how to receive the remote control signal when using the pattern match mode of the PMC0 circuit.

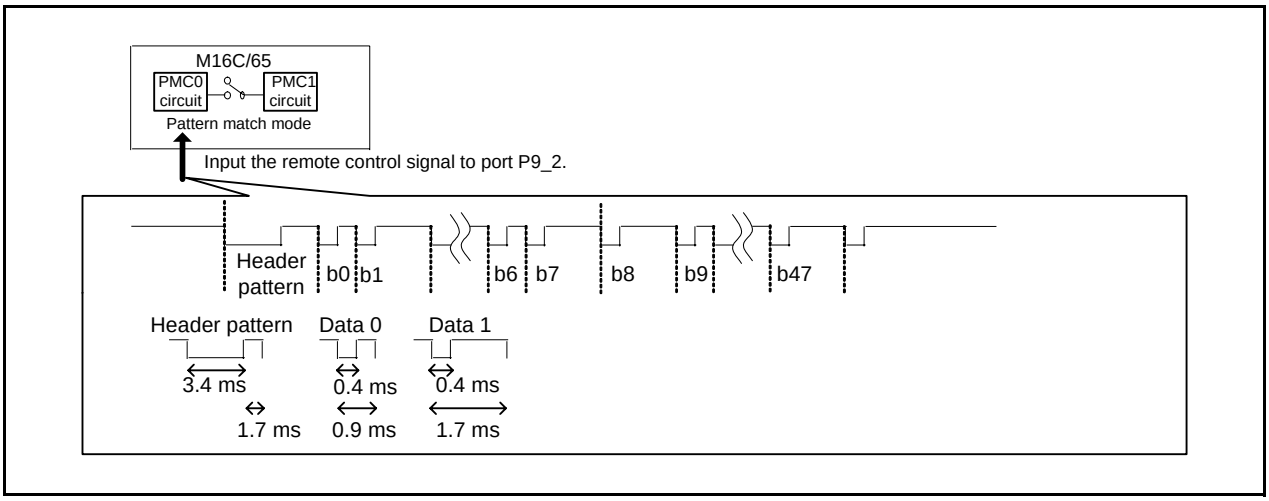


Figure 3.3 Outline of the Remote Control Format with Header Pattern

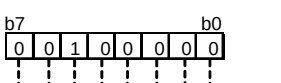
The detection pattern is designed to accept a tolerance of ±10% from the format width shown in Figure 3.3. See the following table for settings.

Table 3.2 PMC0 Circuit Settings

Item		Description
Count sources	Clock source	fC
	Division	No division
Operation mode		Pattern match mode
Pattern match mode	Detect patterns	Header
		Data 0 or data 1 match
	Interrupt request generation timing	Completion of data reception
	Selectable functions	Input signal inversion
		Digital filter
		Error flag hold
Input port		P9_2

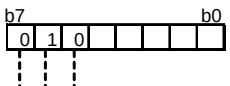
Register settings

PMC0 Function Select Register 3



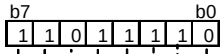
Symbol	Address	
PMC0CON3	01F3h	
Bit Symbol	Bit Name	Function
PD/CST/CFR/CRE	Mode select bit	0000: Pattern match mode
CSRC1 to CSRC0	Clock source select bit	10: fC
CDIV1 to CDIV0	Count source divisor select bit	00: No division

PMC0 Function Select Register 2



Symbol	Address	
PMC0CON2	01F2h	
Bit Symbol	Bit Name	Function
CEINT	Counter overflow interrupt enable bit	0: Disabled
PSEL1 to PSEL0	Input pin select bit	01: PMC0 pin

PMC0 Function Select Register 0



Symbol	Address
PMC0CON0	01F0h

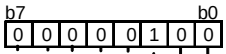
Bit Symbol	Bit Name	Function
EN	PMC0 operation enable bit	0: Operation disabled
SINV	Input signal polarity invert bit	1: Inverted
FIL	Filter enable bit	1: Filter enabled
EHOLD	Error flag hold bit	Status of the REFLG bit in the PMC0STS register: 1: Held even after next data received
HDEN	Header pattern enable bit	1: Header enabled
SDEN	Special data pattern enable bit	0: Special data pattern disabled
DRINT1 to DRINT0	Receive interrupt control bit	11: Interrupt request is generated when compare match and no receive error occurs, and reception completed. (1)

PMC0 Function Select Register 1

Symbol	Address
PMC0CON1	01F1h

Bit Symbol	Bit Name	Function
TYP1 to TYP0	Receive mode select bit	00: Period measurement (between rising edge and rising edge)
CSS	Counter start control bit	0: Counters operate individually
EXSDEN	Special pattern detect block select bit	0: PMC0
EXHDEN	Header pattern detect block select bit	0: PMC0

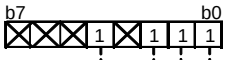
PMC0 Interrupt Source Register



Symbol	Address
PMC0INT	01F5h

Bit Symbol	Bit Name	Function
CPINT	Compare match flag interrupt enable bit	0: Disabled
REINT	Receive error flag interrupt enable bit	0: Disabled
DRINT	Data reception complete interrupt enable bit	1: Enabled
BFULINT	Receive buffer full flag interrupt enable bit	0: Disabled
PTHDINT	Header match flag interrupt enable bit	0: Disabled
PTDINT	Data 0/1 match flag interrupt enable bit	0: Disabled
TIMINT	Timer measure interrupt enable bit	0: Disabled
SDINT	Special data match flag interrupt enable bit	0: Disabled

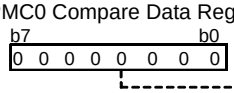
PMC0 Compare Control Register



Symbol	Address
PMC0CPC	01F6h

Bit Symbol	Bit Name	Function
CPN2 to CPN0	Compare bit specified bit	Bits 7 to 0 are compared
CPEN	Compare enable bit	1: Compare enabled

PMC0 Compare Data Register



Symbol	Address
PMC0CPD	01F7h

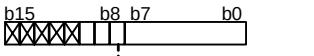
Function
Compare with 00000000b

See Note 2.

Notes:
1. Set bits DRINT1 to DRINT0 to 00b when the compare match function is not used.
2. Set all bits to 0 when the compare match function is not used.
   Check the specification to set the compared value when the compare match function is used.

PMC0 Header Pattern Set Register (MIN)

Symbol	Address
PMC0HDPMIN	D081h to D080h

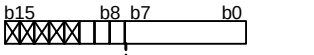


Function

(3.4 + 1.7) [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 149

PMC0 Header Pattern Set Register (MAX)

Symbol	Address
PMC0HDPMAX	D083h to D082h

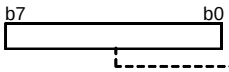


Function

(3.4 + 1.7) [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 183

PMC0 Data 0 Pattern Set Register (MIN)

Symbol	Address
PMC0D0PMIN	D084h

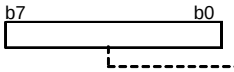


Function

0.9 [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 26

PMC0 Data 0 Pattern Set Register (MAX)

Symbol	Address
PMC0D0PMAX	D085h

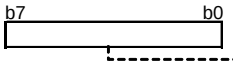


Function

0.9 [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 31

PMC0 Data 1 Pattern Set Register (MIN)

Symbol	Address
PMC0D1PMIN	D086h

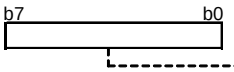


Function

1.7 [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 49

PMC0 Data 1 Pattern Set Register (MAX)

Symbol	Address
PMC0D1PMAX	D087h

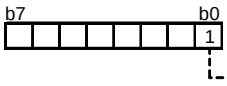


Function

1.7 [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 60

PMC0 Function Select Register 0

Symbol	Address
PMC0CON0	01F0h

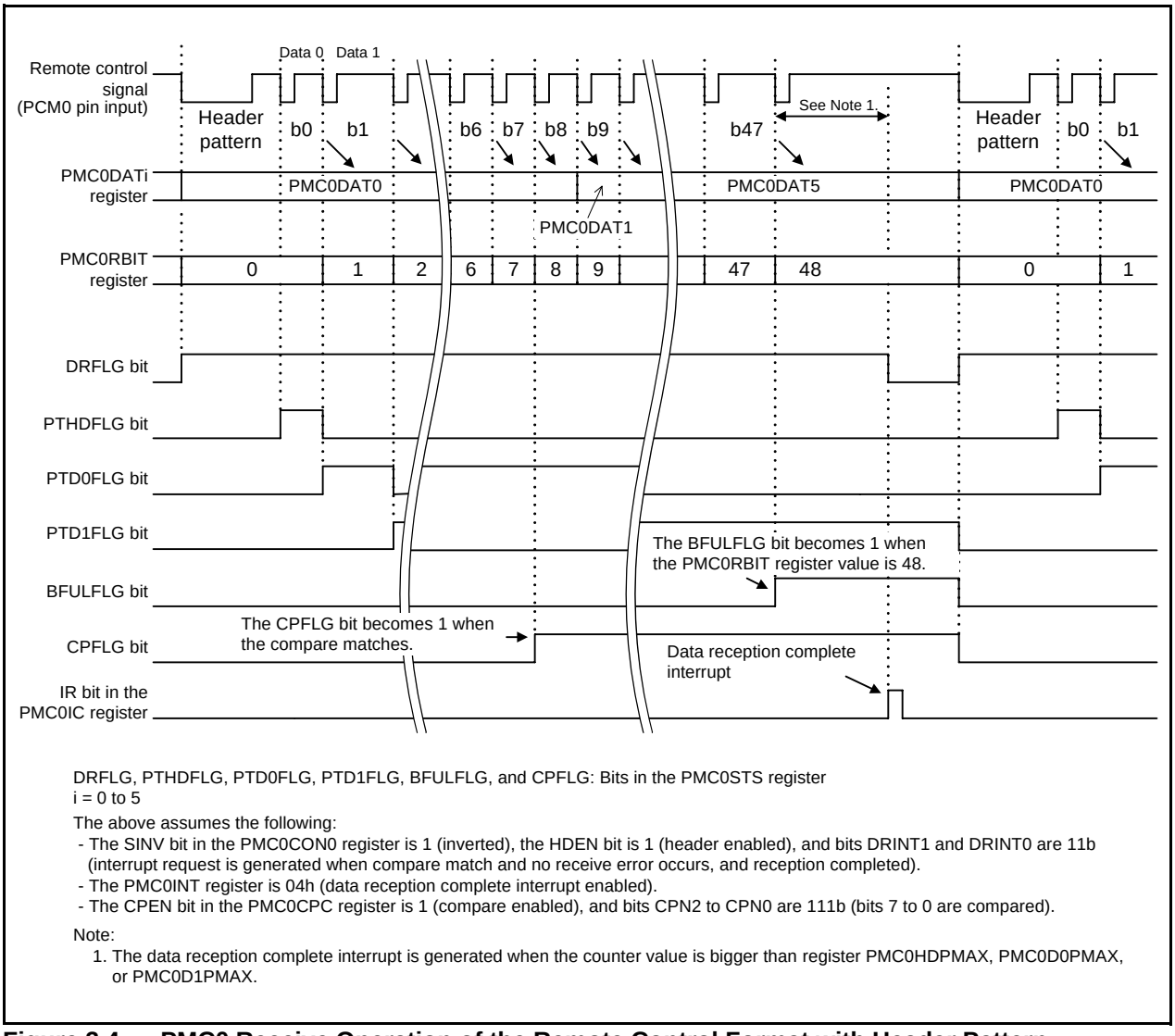


Bit Symbol	Bit Name	Function
EN	PMC0 operation enable bit	1: Operation enabled

Operation

(1) The receive operation starts at the first falling edge of the header.
(2) The receive data is stored bit by bit in PMC0DATi (i = 0 to 5).
(3) After receiving the 48th bit, if a falling edge is not detected by the time the maximum time set to the header, data 0, or data 1 has elapsed, a data reception complete interrupt is generated.
(4) Read registers PMC0DATi and PMC0RBIT in the data reception complete interrupt.

Figure 3.4 shows the condition of the status flags and the interrupt generation timing of the PMC0 circuit in remote control reception.



DRFLG, PTHDFLG, PTD0FLG, PTD1FLG, BFULFLG, and CPFLG: Bits in the PMC0STS register
i = 0 to 5

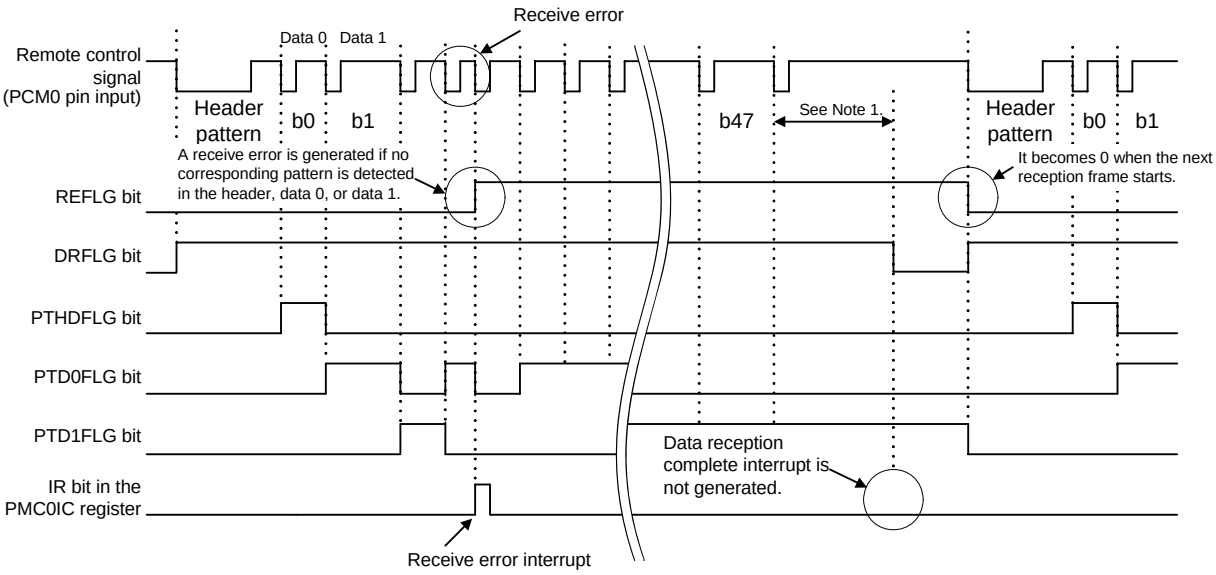
The above assumes the following:
- The SINV bit in the PMC0CON0 register is 1 (inverted), the HDEN bit is 1 (header enabled), and bits DRINT1 and DRINT0 are 11b (interrupt request is generated when compare match and no receive error occurs, and reception completed).
- The PMC0INT register is 04h (data reception complete interrupt enabled).
- The CPEN bit in the PMC0CPC register is 1 (compare enabled), and bits CPN2 to CPN0 are 111b (bits 7 to 0 are compared).

Note:
1. The data reception complete interrupt is generated when the counter value is bigger than register PMC0HDPMAX, PMC0D0PMAX, or PMC0D1PMAX.

Figure 3.4 PMC0 Receive Operation of the Remote Control Format with Header Pattern

3.2.1 Receive Error of the PMC0 Circuit in Pattern Match Mode

Figure 3.5 shows the change of the status flags and the interrupt generation timing when a receive error is generated in 3.2 "Receive Operation of the Remote Control Format with Header Pattern". The SFR settings in section 3.2 enable the receive error interrupt.



REFLG, DRFLG, PTHDFLG, PTD0FLG, and PTD1FLG: Bits in the PMC0STS register

The above assumes the following:
- The EHOLD bit in the PMC0CON0 register is 1 (state of the REFLG bit in the PMCiSTS register is held even after next data received), the SINV bit is 1 (inverted), the HDEN bit is 1 (header enabled), and bits DRINT1 and DRINT0 are 11b (interrupt request is generated when compare match and no receive error occurs, and reception completed).
- The PMC0INT register is 06h (receive error flag interrupt enabled, data reception complete interrupt enabled).

Note:
1. The data reception complete interrupt is generated when the counter value is bigger than register PMC0HDPMAX, PMC0D0PMAX, or PMC0D1PMAX.

Figure 3.5 PMC0 Receive Operation of the Remote Control Format with Header Pattern When Receive Error Occurs

A receive error is generated if no corresponding pattern is detected in the header, data 0, or data 1, and a receive error interrupt request is generated.
Acknowledge the receive error in the receive error interrupt handling.
A data reception complete interrupt will not be generated at this time because bits DRINT1 to DRINT0 are 11b (interrupt request is generated when a compare match and no receive error occurs, and reception completed).

3.3 Remote Control Signal Receiver with Special Header Pattern

Figure 3.6 shows the outline of the remote control format with special header reception of the PMC0 individual circuit operation in the pattern match mode.

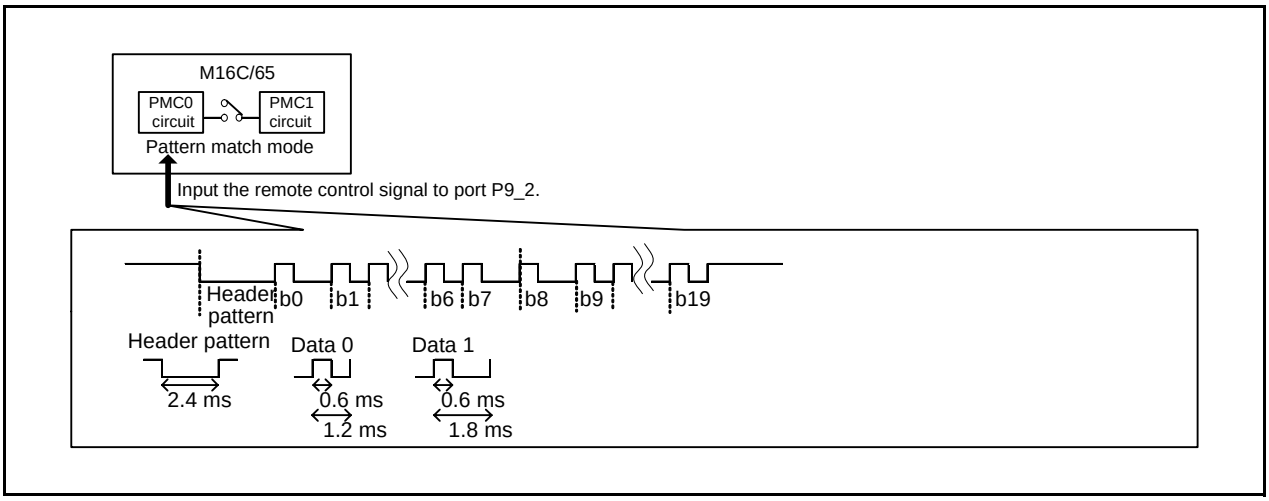


Figure 3.6 Outline of the Remote Control Format with Special Header Pattern

The detection pattern is designed to accept a tolerance of ±10% from the format width shown in Figure 3.6. See the following table for settings.

Table 3.3 PMC0 Circuit Settings

Item		Description
Count sources	Clock source	fC
	Division	No division
Operation mode		Pattern match mode
Pattern match mode	Detect patterns	Header
		Data 0 or data 1 match
	Interrupt request generation timing	Completion of data reception
	Selectable functions	Input signal not inverted
		Digital filter
		Error flag hold
Input port		P9_2

Register settings

PMC0 Function Select Register 3

b7 b0: 0 0 1 0 0 0 0 0

Bit Symbol	Bit Name	Function
PD/CST/CFR/CRE	Mode select bit	0000: Pattern match mode
CSRC1 to CSRC0	Clock source select bit	10: fC
CDIV1 to CDIV0	Count source divisor select bit	00: No division

Symbol: PMC0CON3 Address: 01F3h

PMC0 Function Select Register 2

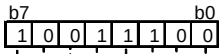
b7 b0: 0 1 0

Bit Symbol	Bit Name	Function
CEINT	Counter overflow interrupt enable bit	0: Disabled
PSEL1 to PSEL0	Input pin select bit	01: PMC0 pin

Symbol: PMC0CON2 Address: 01F2h

PMC0 Function Select Register 0

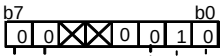
Symbol	Address
PMC0CON0	01F0h



Bit Symbol	Bit Name	Function
EN	PMC0 operation enable bit	0: Operation disabled
SINV	Input signal polarity invert bit	0: Not inverted
FIL	Filter enable bit	1: Filter enabled
EHOLD	Error flag hold bit	State of the REFLG bit in the PMC0STS register: 1: Held even after next data received
HDEN	Header pattern enable bit	1: Header enabled
SDEN	Special data pattern enable bit	0: Special data pattern disabled
DRINT1 to DRINT0	Receive interrupt control bit	10: Interrupt requested is generated when no receive error occurs and reception completed

PMC0 Function Select Register 1

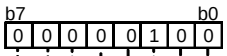
Symbol	Address
PMC0CON1	01F1h



Bit Symbol	Bit Name	Function
TYP1 to TYP0	Receive mode select bit	10: Pulse width measurement (between rising edge and falling edge, and falling edge and rising edge)
CSS	Counter start control bit	0: Counters operate individually
EXSDEN	Special pattern detect block select bit	0: PMC0
EXHDEN	Header pattern detect block select bit	0: PMC0

PMC0 Interrupt Source Register

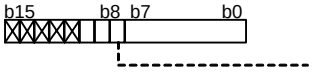
Symbol	Address
PMC0INT	01F5h



Bit Symbol	Bit Name	Function
CPINT	Compare match flag interrupt enable bit	0: Disabled
REINT	Receive error flag interrupt enable bit	0: Disabled
DRINT	Data reception complete interrupt enable bit	1: Enabled
BFULINT	Receive buffer full flag interrupt enable bit	0: Disabled
PTHDINT	Header match flag interrupt enable bit	0: Disabled
PTDINT	Data 0/1 match flag interrupt enable bit	0: Disabled
TIMINT	Timer measure interrupt enable bit	0: Disabled
SDINT	Special data match flag interrupt enable bit	0: Disabled

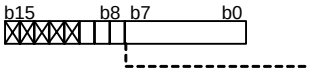
PMC0 Header Pattern Set Register (MIN)

Symbol	Address
PMC0HDPMIN	D081h to D080h



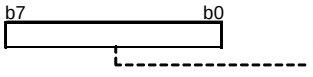
PMC0 Header Pattern Set Register (MAX)

Symbol	Address
PMC0HDPMAX	D083h to D082h



PMC0 Data 0 Pattern Set Register (MIN)

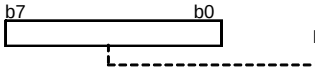
Symbol	Address
PMC0D0PMIN	D084h



Function: 0.6 [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 17

PMC0 Data 0 Pattern Set Register (MAX)

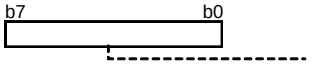
Symbol	Address
PMC0D0PMAX	D085h



Function: 0.6 [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 21

PMC0 Data 1 Pattern Set Register (MIN)

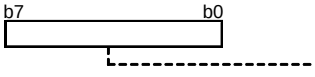
Symbol	Address
PMC0D1PMIN	D086h



Function: 1.2 [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 34

PMC0 Data 1 Pattern Set Register (MAX)

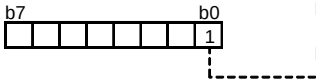
Symbol	Address
PMC0D1PMAX	D087h



Function: 1.2 [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 42

PMC0 Function Select Register 0

Symbol	Address
PMC0CON0	01F0h

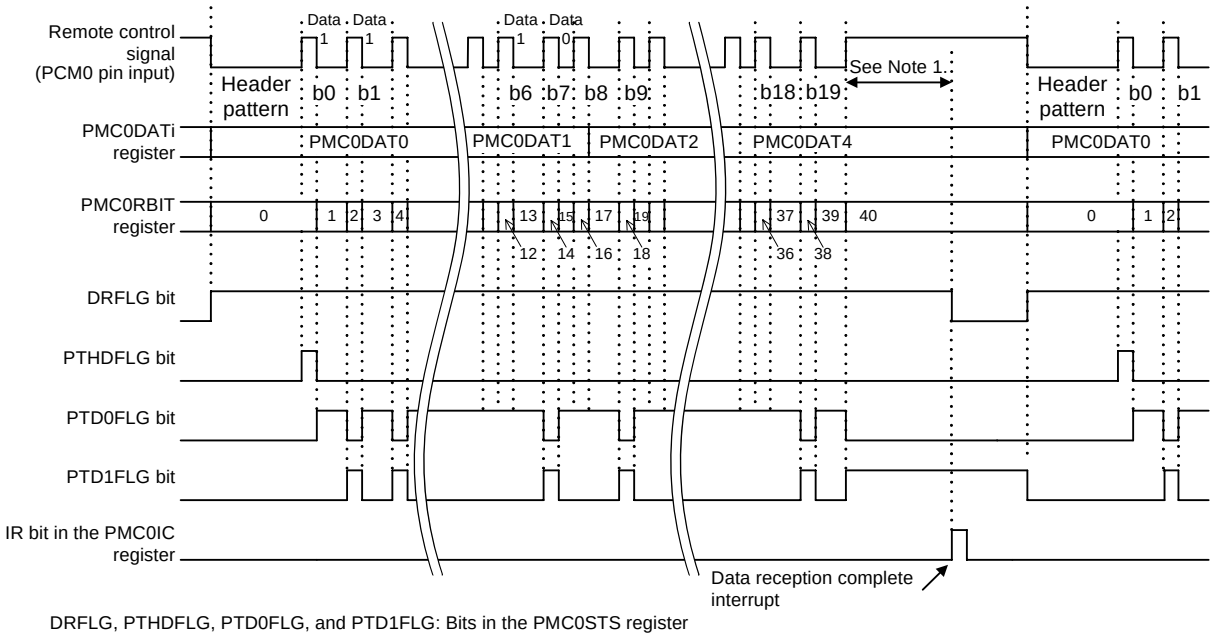


Bit Symbol	Bit Name	Function
EN	PMC0 operation enable bit	1: Operation enabled

Operation

(1) The receive operation starts at the falling edge of the header.
(2) The pulse width of the remote control signal measured at every edge is stored in PMC0DATi in order when the receive operation starts (i = 0 to 5).
(3) After receiving the 20th bit, if there is no falling edge during the maximum time set to the header, data 0, or data 1, a data reception complete interrupt is generated.
(4) Read registers PMC0DATi and PMC0RBIT in the data reception complete interrupt. The data read is encoded.

Figure 3.7 shows the condition of the status flags and the interrupt request generation timing of the PMC0 circuit in remote control reception.



DRFLG, PTHDFLG, PTD0FLG, and PTD1FLG: Bits in the PMC0STS register
i = 0 to 5

The above assumes the following:
- The SINV bit in the PMC0CON0 register is 0 (not inverted), the HDEN bit is 1 (header enabled), and bits DRINT1 to DRINT0 are 10b (interrupt request is generated when no receive error occurs and reception completed).
- Bits TYP1 to TYP0 in the PMC0CON1 register are 10b (pulse width measurement).
- The PMC0INT register is 04h (data reception complete interrupt enabled).

Note:
1. The data reception complete interrupt is generated when the counter value is bigger than register PMC0HDPMAX, PMC0D0PMAX, or PMC0D1PMAX.

Figure 3.7 PMC0 Individual Operation of the Remote Control Format with Special Header Pattern

Encoding process

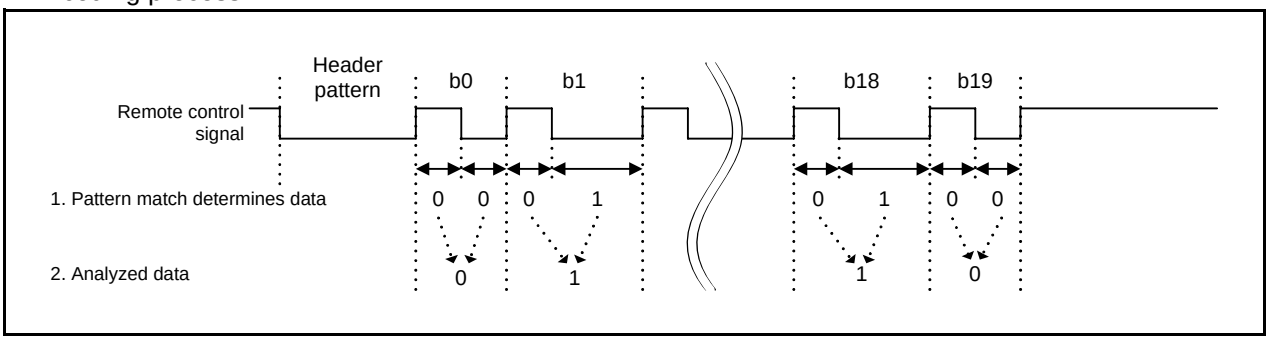


Figure 3.8 Analytical Operation Example of Format with Special Header Pattern

(1) The pulse width is measured in pattern match mode.
(2) Every 2 bits of data measured after the receive operation is completed.
When the data is 00b, it is determined to be data 0 and converted.
When the data is 01b, it is determined to be data 1 and converted.

4. Individual Operation of the PMC1 Circuit in Pattern Match Mode

4.1 Remote Control Signal Reception without Header Pattern

Figure 4.1 shows how to receive the remote control signal when not using the pattern match mode of the PMC1 circuit.

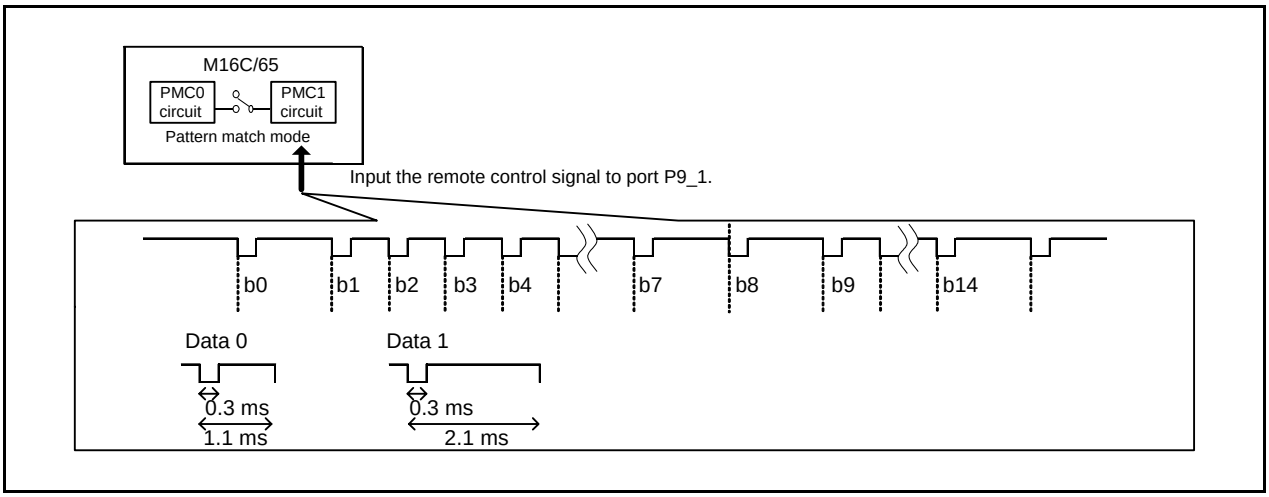


Figure 4.1 PMC1 Receive Outline of the Remote Control Format without Header Pattern

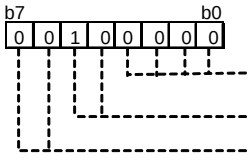
The detection pattern is designed to accept a tolerance of ±10% from the format width shown in Figure 4.1. See the following table for settings.

Table 4.1 PMC1 Circuit Settings

Item		Description
Count sources	Clock source	fC
	Division	No division
Operation mode		Pattern match mode
Pattern match mode	Detect patterns	Data 0 or data 1 match
	Interrupt request generation timing	Data 0 or data 1 match
		Completion of data reception
	Selectable functions	Input signal inversion
		Digital filter
Input port		P9_1

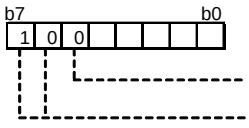
Register settings

PMC1 Function Select Register 3



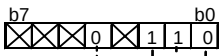
Symbol	Address	
PMC1CON3	01FBh	
Bit Symbol	Bit Name	Function
PD/CST/CFR/CRE	Mode select bit	0000: Pattern match mode
CSRC1 to CSRC0	Clock source select bit	10: fC
CDIV1 to CDIV0	Count source divisor select bit	00: No division

PMC1 Function Select Register 2



Symbol	Address	
PMC1CON2	01FAh	
Bit Symbol	Bit Name	Function
CEINT	Counter overflow interrupt enable bit	0: Disabled
PSEL1 to PSEL0	Input pin select bit	10: PMC1 pin

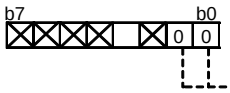
PMC1 Function Select Register 0



Symbol	Address
PMC1CON0	01F8h

Bit Symbol	Bit Name	Function
EN	PMC1 operation enable bit	0: Operation disabled
SINV	Input signal polarity invert bit	1: Inverted
FIL	Filter enable bit	1: Filter enabled
HDEN	Header pattern enable bit	0: Header disabled

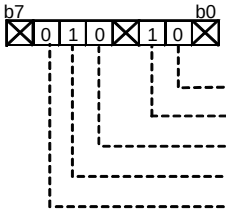
PMC1 Function Select Register 1



Symbol	Address
PMC1CON1	01F9h

Bit Symbol	Bit Name	Function
TYP1 to TYP0	Receive mode select bit	00: Period measurement (between rising edge and rising edge)

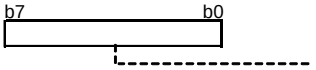
PMC1 Interrupt Source Register



Symbol	Address
PMC1INT	01FDh

Bit Symbol	Bit Name	Function
REINT	Receive error flag interrupt enable bit	0: Disabled
DRINT	Data reception complete interrupt enable bit	1: Enabled
PTHDINT	Header match flag interrupt enable bit	0: Disabled
PTDINT	Data 0/1 match flag interrupt enable bit	1: Enabled
TIMINT	Timer measure interrupt enable bit	0: Disabled

PMC1 Data 0 Pattern Set Register (MIN)

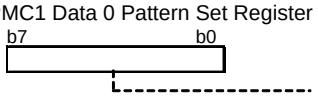


Symbol	Address
PMC1D0PMIN	D098h

Function

1.1 [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 31

PMC1 Data 0 Pattern Set Register (MAX)

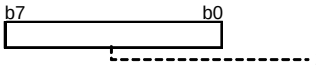


Symbol	Address
PMC1D0PMAX	D099h

Function

1.1 [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 39

PMC1 Data 1 Pattern Set Register (MIN)

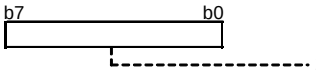


Symbol	Address
PMC1D1PMIN	D09Ah

Function

2.1 [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 61

PMC1 Data 1 Pattern Set Register (MAX)

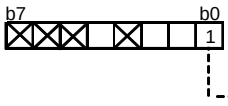


Symbol	Address
PMC1D1PMAX	D09Bh

Function

2.1 [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 75

PMC1 Function Select Register 0



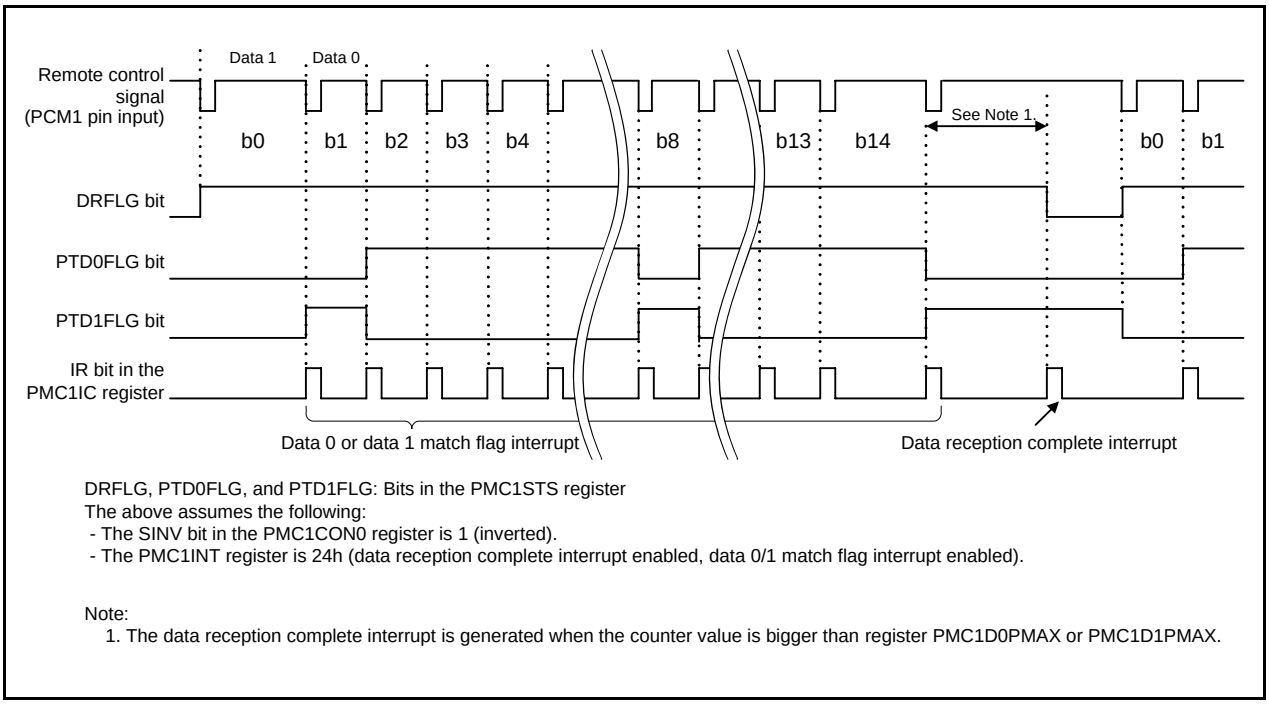
Symbol	Address
PMC1CON0	01F8h

Bit Symbol	Bit Name	Function
EN	PMC1 operation enable bit	1: Operation enabled

Operation

(1) The receive operation starts at the first falling edge.
(2) When receiving data, store the receive data bit by bit using the data 0/1 match flag interrupt in the program.
(3) After receiving the 15th bit, if a falling edge is not detected by the time the maximum time set to data 0 or data 1 has elapsed, a data reception complete interrupt is generated.
(4) The receive data is stored to an array in the data reception complete interrupt.

Figure 4.2 shows the condition of the status flags and the interrupt generation timing of the PMC1 circuit when receiving the remote control signal.



DRFLG, PTD0FLG, and PTD1FLG: Bits in the PMC1STS register
The above assumes the following:
- The SINV bit in the PMC1CON0 register is 1 (inverted).
- The PMC1INT register is 24h (data reception complete interrupt enabled, data 0/1 match flag interrupt enabled).

Note:
1. The data reception complete interrupt is generated when the counter value is bigger than register PMC1D0PMAX or PMC1D1PMAX.

Figure 4.2 PMC1 Receive Operation of the Remote Control Format without Header Pattern

4.2 Remote Control Format with Header Pattern Reception

Figure 4.3 shows the outline of receiving remote control format with header using the pattern match mode of PMC1 circuit.

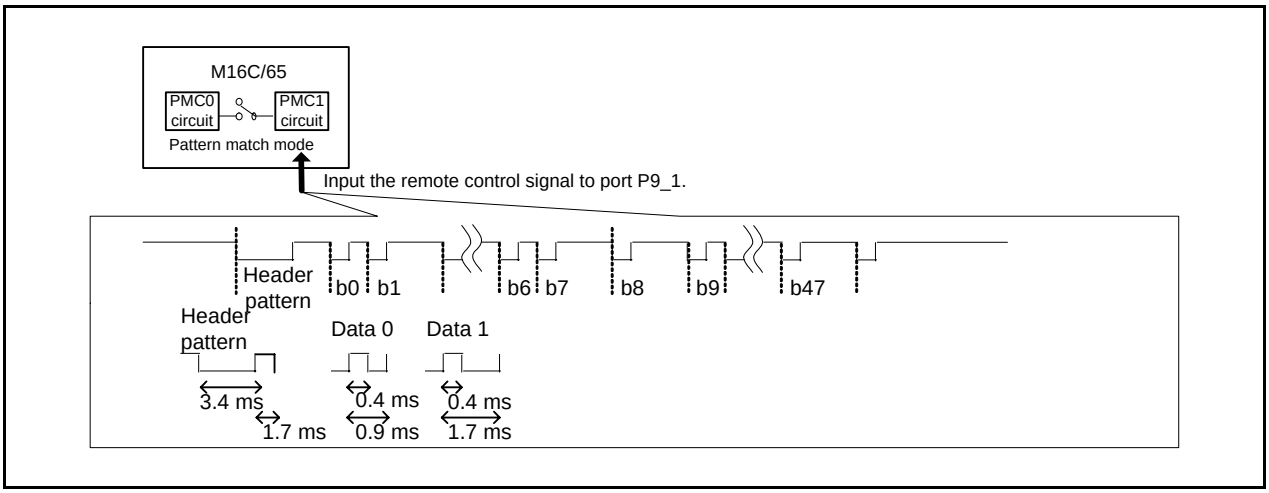


Figure 4.3 Outline of the Remote Control Format with Header Pattern

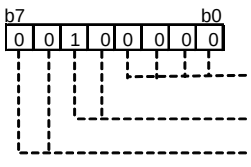
The detection pattern is designed to accept a tolerance of ±10% from the format width shown in Figure 4.3. See the following table for settings.

Table 4.2 PMC1 Circuit Settings

Item		Description
Count sources	Clock source	fC
	Division	No division
Operation mode		Pattern match mode
Pattern match mode	Detect patterns	Header
		Data 0 or data 1 match
	Interrupt request generation timing	Data 0 or data 1 match
		Completion of data reception
	Selectable functions	Input signal inversion
		Digital filter
Input port		P9_1

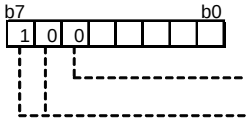
Register settings

PMC1 Function Select Register 3



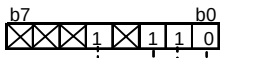
Symbol	Address	
PMC1CON3	01FBh	
Bit Symbol	Bit Name	Function
PD/CST/CFR/CRE	Mode select bit	0000: Pattern match mode
CSRC1 to CSRC0	Clock source select bit	10: fC
CDIV1 to CDIV0	Count source divisor select bit	00: No division

PMC1 Function Select Register 2



Symbol	Address	
PMC1CON2	01FAh	
Bit Symbol	Bit Name	Function
CEINT	Counter overflow interrupt enable bit	0: Disabled
PSEL1 to PSEL0	Input pin select bit	10: PMC1 pin

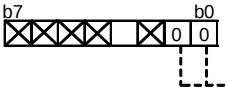
PMC1 Function Select Register 0



Symbol	Address
PMC1CON0	01F8h

Bit Symbol	Bit Name	Function
EN	PMC1 operation enable bit	0: Operation disabled
SINV	Input signal polarity invert bit	1: Inverted
FIL	Filter enable bit	1: Filter enabled
HDEN	Header pattern enable bit	1: Header enabled

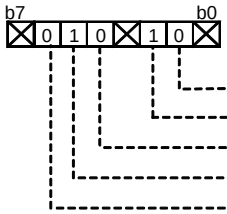
PMC1 Function Select Register 1



Symbol	Address
PMC1CON1	01F9h

Bit Symbol	Bit Name	Function
TYP1 to TYP0	Receive mode select bit	00: Period measurement (between rising edge and rising edge)

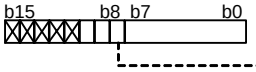
PMC1 Interrupt Source Register



Symbol	Address
PMC1INT	01FDh

Bit Symbol	Bit Name	Function
REINT	Receive error flag interrupt enable bit	0: Disabled
DRINT	Data reception complete interrupt enable bit	1: Enabled
PTHDINT	Header match flag interrupt enable bit	0: Disabled
PTDINT	Data 0/1 match flag interrupt enable bit	1: Enabled
TIMINT	Timer measure interrupt enable bit	0: Disabled

PMC1 Header Pattern Set Register (MIN)

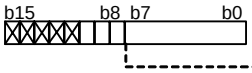


Symbol	Address
PMC1HDPMIN	D095h to D094h

Function

(3.4 + 1.7) [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 149

PMC1 Header Pattern Set Register (MAX)

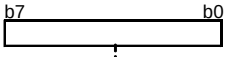


Symbol	Address
PMC1HDPMAX	D097h to D096h

Function

(3.4 + 1.7) [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 183

PMC1 Data 0 Pattern Set Register (MIN)

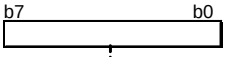


Symbol	Address
PMC1D0PMIN	D098h

Function

0.9 [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 26

PMC1 Data 0 Pattern Set Register (MAX)

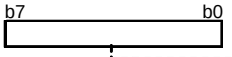


Symbol	Address
PMC1D0PMAX	D099h

Function

0.9 [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 31

PMC1 Data 1 Pattern Set Register (MIN)

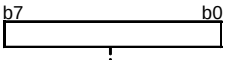


Symbol	Address
PMC1D1PMIN	D09Ah

Function

1.7 [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 49

PMC1 Data 1 Pattern Set Register (MAX)

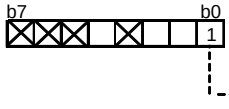


Symbol	Address
PMC1D1PMAX	D09Bh

Function

1.7 [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 60

PMC1 Function Select Register 0



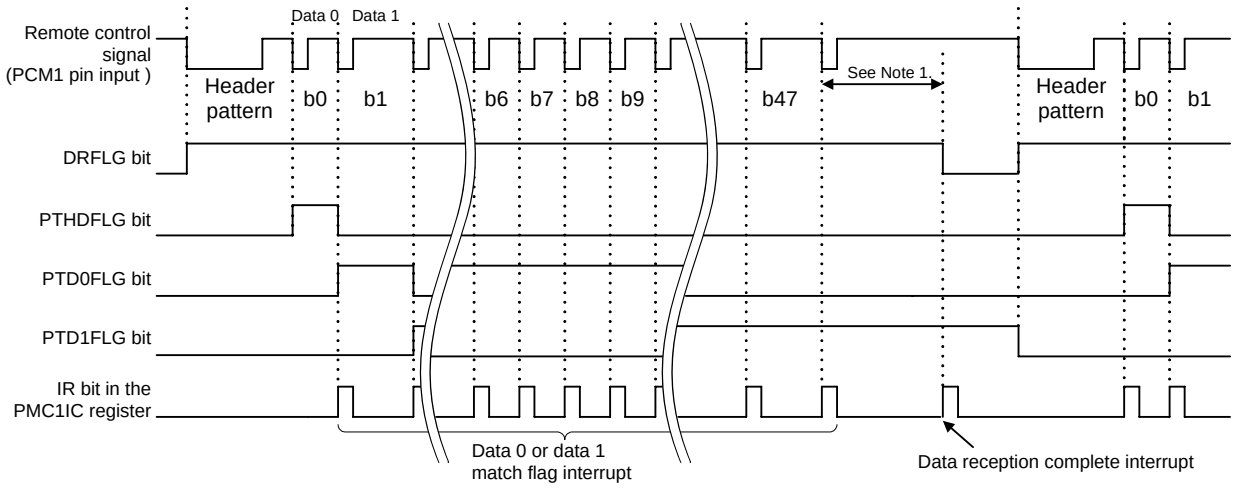
Symbol	Address
PMC1CON0	01F8h

Bit Symbol	Bit Name	Function
EN	PMC1 operation enable bit	1: Operation enabled

Operation

(1) The receive operation starts at the first falling edge of the header.
(2) Store the receive data bit by bit using data 0/1 match flag interrupt in the program when receiving data.
(3) After receiving the 48th bit, if a falling edge is not detected by the time the maximum time set to the header, data 0, or data 1 has elapsed, a data reception complete interrupt is generated.
(4) The receive data is stored to an array in the data reception complete interrupt.

Figure 4.4 shows the condition of the status flags and the interrupt generation timing of the PMC1 circuit in remote control reception.



DRFLG, PTHDFLG, PTD0FLG, and PTD1FLG: Bits in the PMC1STS register

The above assumes the following:
- The SINV bit in the PMC1CON0 register is 1 (inverted), and the HDEN bit is 1 (header enabled).
- The PMC1INT register is 24h (data reception complete interrupt enabled, data 0/1 match flag interrupt enabled).

Note:
1. The data reception complete interrupt is generated when the counter value is bigger than register PMC1HDPMAX, PMC1D0PMAX, or PMC1D1PMAX.

Figure 4.4 PMC1 Receive Operation of the Remote Control Format with Header Pattern

4.3 Bi-Phase Remote Control Format Reception

Figure 4.5 shows the outline of receiving bi-phase remote control format using the pattern match mode of PMC1 circuit.

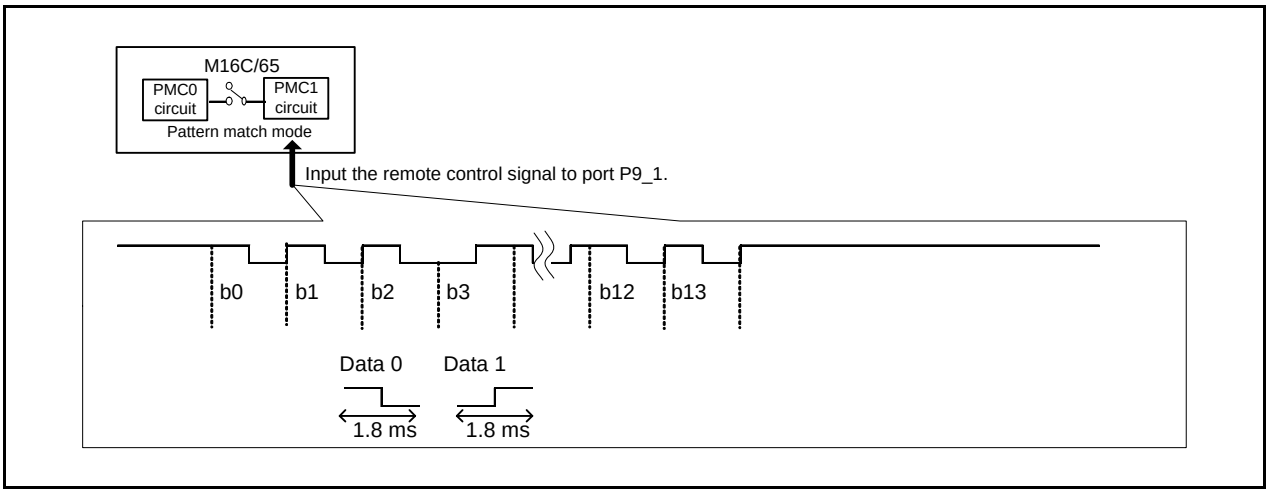


Figure 4.5 Outline of the Bi-Phase Remote Control Format

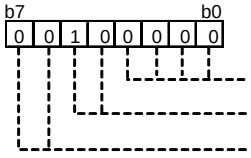
The detection pattern is designed to accept a tolerance of ±20% from the format width shown in Figure 4.5. See the following table for settings.

Table 4.3 PMC1 Circuit Settings

Item		Description
Count sources	Clock source	fC
	Division	No division
Operation mode		Pattern match mode
Pattern match mode	Detect patterns	Data 0 or data 1 match
	Interrupt request generation timing	Data 0 or data 1 match
		Completion of data reception
	Selectable functions	Input signal not inverted
		Digital filter
Input port		P9_1

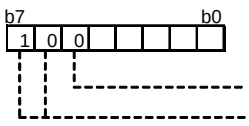
Register settings

PMC1 Function Select Register 3



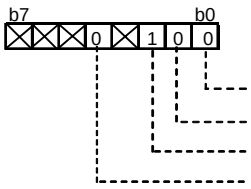
Symbol	Address	
PMC1CON3	01FBh	
Bit Symbol	Bit Name	Function
PD/CST/CFR/CRE	Mode select bit	0000: Pattern match mode
CSRC1 to CSRC0	Clock source select bit	10: fC
CDIV1 to CDIV0	Count source divisor select bit	00: No division

PMC1 Function Select Register 2



Symbol	Address	
PMC1CON2	01FAh	
Bit Symbol	Bit Name	Function
CEINT	Counter overflow interrupt enable bit	0: Disabled
PSEL1 to PSEL0	Input pin select bit	10: PMC1 pin

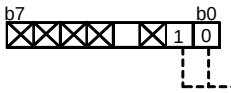
PMC1 Function Select Register 0



Symbol	Address
PMC1CON0	01F8h

Bit Symbol	Bit Name	Function
EN	PMC1 operation enable bit	0:Operation disabled
SINV	Input signal polarity invert bit	0: Not inverted
FIL	Filter enable bit	1: Filter enabled
HDEN	Header pattern enable bit	0: Header disabled

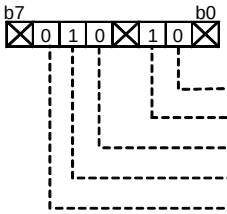
PMC1 Function Select Register 1



Symbol	Address
PMC1CON1	01F9h

Bit Symbol	Bit Name	Function
TYP1 to TYP0	Receive mode select bit	10: Pulse width measurement (between rising edge and falling edge, and falling edge and rising edge)

PMC1 Interrupt Source Register

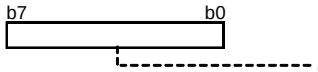


Symbol	Address
PMC1INT	01FDh

Bit Symbol	Bit Name	Function
REINT	Receive error flag interrupt enable bit	0: Disabled
DRINT	Data reception complete interrupt enable bit	1: Enabled
PTHDINT	Header match flag interrupt enable bit	0: Disabled
PTDINT	Data 0/1 match flag interrupt enable bit	1: Enabled
TIMINT	Timer measure interrupt enable bit	0: Disabled

PMC1 Data 0 Pattern Set Register (MIN)

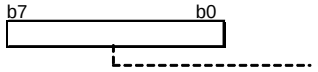
Symbol	Address
PMC1D0PMIN	D098h



0.9 [ms] × (1 - 0.2) / (1 / 32.768 [kHz]) - 1 = 23

PMC1 Data 0 Pattern Set Register (MAX)

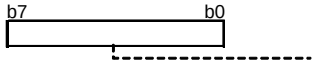
Symbol	Address
PMC1D0PMAX	D099h



0.9 [ms] × (1 + 0.2) / (1 / 32.768 [kHz]) - 1 = 36

PMC1 Data 1 Pattern Set Register (MIN)

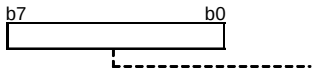
Symbol	Address
PMC1D1PMIN	D09Ah



1.7 [ms] × (1 - 0.2) / (1 / 32.768 [kHz]) - 1 = 47

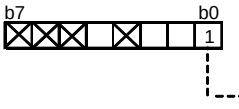
PMC1 Data 1 Pattern Set Register (MAX)

Symbol	Address
PMC1D1PMAX	D09Bh



1.7 [ms] × (1 + 0.2) / (1 / 32.768 [kHz]) - 1 = 71

PMC1 Function Select Register 0



Symbol	Address
PMC1CON0	01F8h

Bit Symbol	Bit Name	Function
EN	PMC1 operation enable bit	1: Operation enabled

Operation

(1) The receive operation starts at the falling edge of b0.
(2) Store the receive data bit by bit using the data 0/1 match flag interrupt in the program when receiving data.
(3) After receiving the 14th bit, if a falling edge is not detected by the time the maximum time set to data 0 or data 1 has elapsed, a data reception complete interrupt is generated.
(4) The receive data is stored to an array in the data reception complete interrupt.

Figure 4.6 shows the condition of the status flags and the interrupt generation timing of the PMC1 circuit in remote control reception.

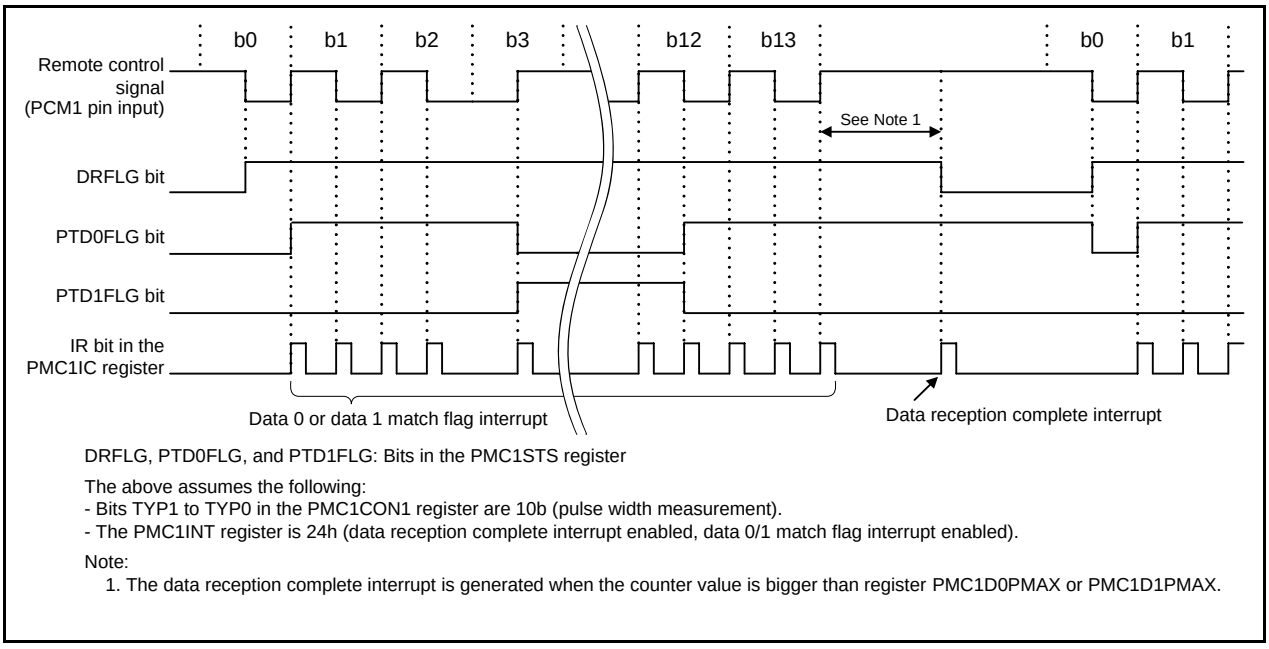


Figure 4.6 PMC1 Receive Operation of the Bi-Phase Remote Control Format

Encoding process

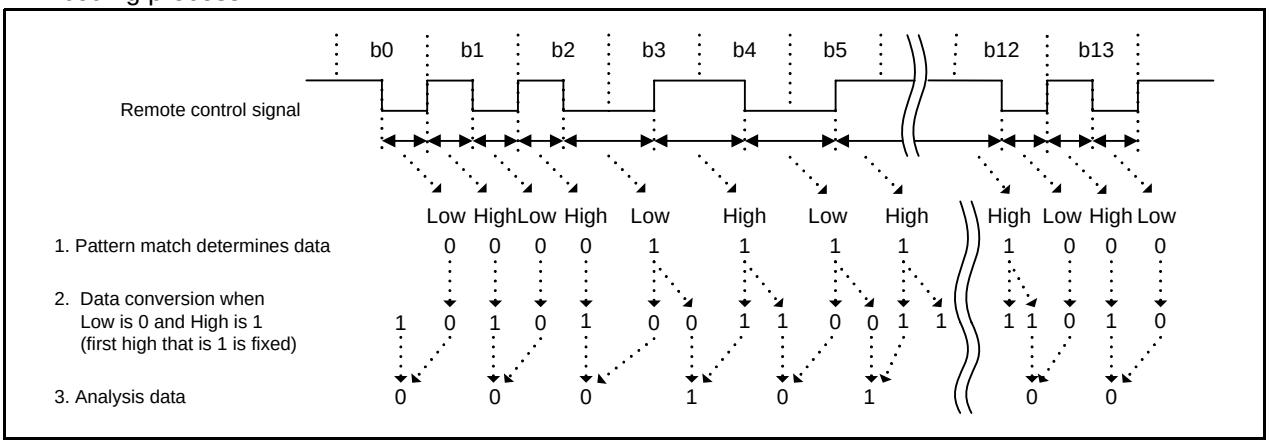


Figure 4.7 Analytical Operation Example of Bi-Phase Format

(1) The pulse width measurement is set for monitoring the signal determined data 0 or data 1 in pattern match mode.
(2) Based in Figure 6.6 PMC1 circuit receive timing, high and low periods are measured.
Convert to:
High period is long: 11b, high period is short: 1.
Low period is long: 00b, low period is short: 0.
(3) The 2 bits of data converted in step 2 converted to 1 bit in bi-phase format.

5. Combined Operation of the PMC0 and PMC1 Circuits in Pattern

5.1 Remote Control Signal Receiver with Header Pattern and Spacer

Figure 5.1 shows the outline of receiving remote control format with header and spacer using the pattern match mode of the PMC0 and PMC1 circuits.

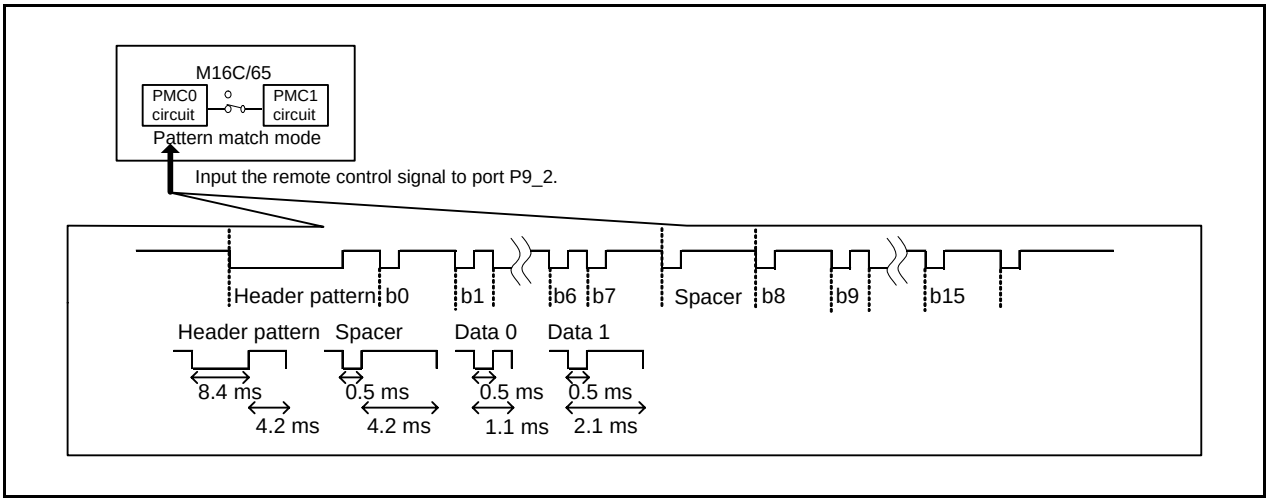


Figure 5.1 Outline of the Remote Control Signal Receiver with Header Pattern and Spacer

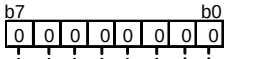
The detection pattern is designed to accept a tolerance of ±10% from the format width shown in Figure 5.1. See the following table for settings.

Table 5.1 PMC0/PMC1 Circuit Settings

Item		Description	
		PMC0 circuit	PMC1 circuit
Count sources	Clock source	fC	
	Division	No division	
Operation mode		Pattern match mode	
Pattern match mode	Detect patterns	Special data	Header
		Data 0 or data 1 match	
	Interrupt request generation timing	Completion of data reception	
	Selectable functions	Input signal inversion	
		Digital filter	
		Error flag hold	
Input port		P9_2	

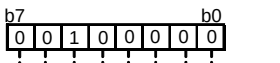
Register settings

PMC0 Function Select Register 3



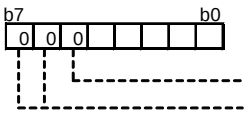
Symbol	Address	
PMC0CON3	01F3h	
Bit Symbol	Bit Name	Function
PD/CST/CFR/CRE	Mode select bit	0000: Pattern match mode
CSRC1 to CSRC0	Clock source select bit	00: Same as PMC1
CDIV1 to CDIV0	Count source divisor select bit	00: No division

PMC1 Function Select Register 3



Symbol	Address	
PMC1CON3	01FBh	
Bit Symbol	Bit Name	Function
PD/CST/CFR/CRE	Mode select bit	0000: Pattern match mode
CSRC1 to CSRC0	Clock source select bit	10: fC
CDIV1 to CDIV0	Count source divisor select bit	00: No division

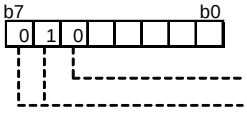
PMC0 Function Select Register 2



Symbol	Address
PMC0CON2	01F2h

Bit Symbol	Bit Name	Function
CEINT	Counter overflow interrupt enable bit	0: Disabled
PSEL1 to PSEL0	Input pin select bit	00: Same as PMC1

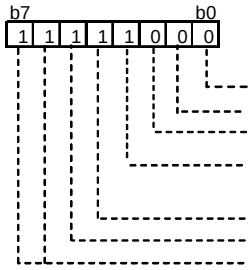
PMC1 Function Select Register 2



Symbol	Address
PMC1CON2	01FAh

Bit Symbol	Bit Name	Function
CEINT	Counter overflow interrupt enable bit	0: Disabled
PSEL1 to PSEL0	Input pin select bit	01: PMC0 pin

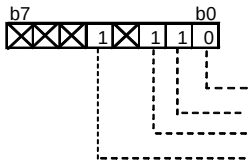
PMC0 Function Select Register 0



Symbol	Address
PMC0CON0	01F0h

Bit Symbol	Bit Name	Function
EN	PMC0 operation enable bit	0: Operation disabled
SINV	Input signal polarity invert bit	Set to 0
FIL	Filter enable bit	Set to 0
EHOLD	Error flag hold bit	Status of the REFLG bit in the PMC0STS register: 1: Held even after next data received
HDEN	Header pattern enable bit	1: Header enabled
SDEN	Special data pattern enable bit	1: Special data pattern enabled
DRINT1 to DRINT0	Receive interrupt control bit	11: Interrupt request is generated when compare match and no receive error occurs, and reception completed

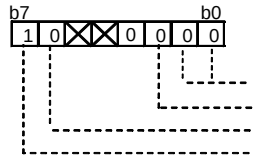
PMC1 Function Select Register 0



Symbol	Address
PMC1CON0	01F8h

Bit Symbol	Bit Name	Function
EN	PMC1 operation enable bit	0: Operation disabled
SINV	Input signal polarity invert bit	1: Inverted
FIL	Filter enable bit	1: Filter enabled
HDEN	Header pattern enable bit	1: Header enabled

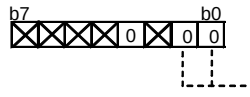
PMC0 Function Select Register 1



Symbol	Address
PMC0CON1	01F1h

Bit Symbol	Bit Name	Function
TYP1 to TYP0	Receive mode select bit	00: Period measurement (between rising edge and rising edge)
CSS	Counter start control bit	0: Counters operate individually
EXSDEN	Special pattern detect block select bit	0: PMC0
EXHDEN	Header pattern detect block select bit	1: PMC1

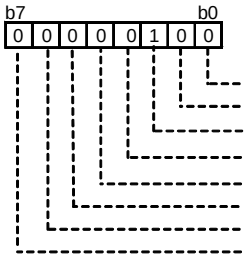
PMC1 Function Select Register 1



Symbol	Address
PMC1CON1	01F9h

Bit Symbol	Bit Name	Function
TYP1 to TYP0	Receive mode select bit	00: Period measurement (between rising edge and rising edge)

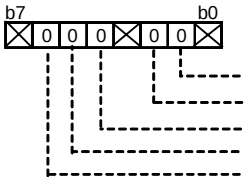
PMC0 Interrupt Source Register



Symbol	Address
PMC0INT	01F5h

Bit Symbol	Bit Name	Function
CPINT	Compare match flag interrupt enable bit	0: Disabled
REINT	Receive error flag interrupt enable bit	0: Disabled
DRINT	Data reception complete interrupt enable bit	1: Enabled
BFULINT	Receive buffer full flag interrupt enable bit	0: Disabled
PTHDINT	Header match flag interrupt enable bit	0: Disabled
PTDINT	Data 0/1 match flag interrupt enable bit	0: Disabled
TIMINT	Timer measure interrupt enable bit	0: Disabled
SDINT	Special data match flag interrupt enable bit	0: Disabled

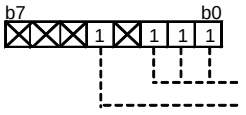
PMC1 Interrupt Source Register



Symbol	Address
PMC1INT	01FDh

Bit Symbol	Bit Name	Function
REINT	Receive error flag interrupt enable bit	0: Disabled
DRINT	Data reception complete interrupt enable bit	0: Disabled
PTHDINT	Header match flag interrupt enable bit	0: Disabled
PTDINT	Data 0/1 match flag interrupt enable bit	0: Disabled
TIMINT	Timer measure interrupt enable bit	0: Disabled

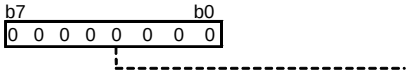
PMC0 Compare Control Register



Symbol	Address
PMC0CPC	01F6h

Bit Symbol	Bit Name	Function
CPN2 to CPN0	Compare bit specified bit	Bits 7 to 0 are compared
CPEN	Compare enable bit	1: Compare enabled

PMC0 Compare Data Register



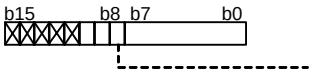
Symbol	Address
PMC0CPD	01F7h

Function

Compare with 0000 0000b

See Note 1.

PMC0 Header Pattern Set Register (MIN)

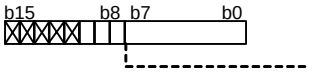


Symbol	Address
PMC0HDPMIN	D081h to D080h

Function

(0.5 + 4.2) [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 138

PMC0 Header Pattern Set Register (MAX)

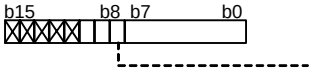


Symbol	Address
PMC0HDPMAX	D083h to D082h

Function

(0.5 + 4.2) [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 168

PMC1 Header Pattern Set Register (MIN)

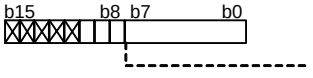


Symbol	Address
PMC1HDPMIN	D095h to D094h

Function

(8.4 + 4.2) [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 371

PMC1 Header Pattern Set Register (MAX)



Symbol	Address
PMC1HDPMAX	D097h to D096h

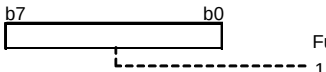
Function

(8.4 + 4.2) [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 453

Note:
1. Set all bits to 0 when the compare match function is not used.
Check the specification to set the compared value when the compare match function is used.

PMC0 Data 0 Pattern Set Register (MIN)

Symbol	Address
PMC0D0PMIN	D084h

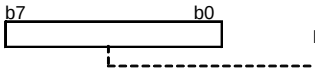


Function

1.1 [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 31

PMC0 Data 0 Pattern Set Register (MAX)

Symbol	Address
PMC0D0PMAX	D085h

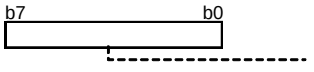


Function

1.1 [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 39

PMC0 Data 1 Pattern Set Register (MIN)

Symbol	Address
PMC0D1PMIN	D086h

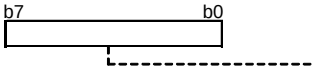


Function

2.1 [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 61

PMC0 Data 1 Pattern Set Register (MAX)

Symbol	Address
PMC0D1PMAX	D087h

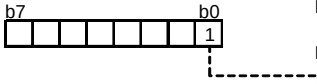


Function

2.1 [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 75

PMC0 Function Select Register 0

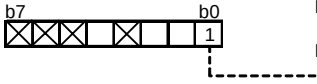
Symbol	Address
PMC0CON0	01F0h



Bit Symbol	Bit Name	Function
EN	PMC0 operation enable bit	1: Operation enabled

PMC1 Function Select Register 0

Symbol	Address
PMC1CON0	01F8h

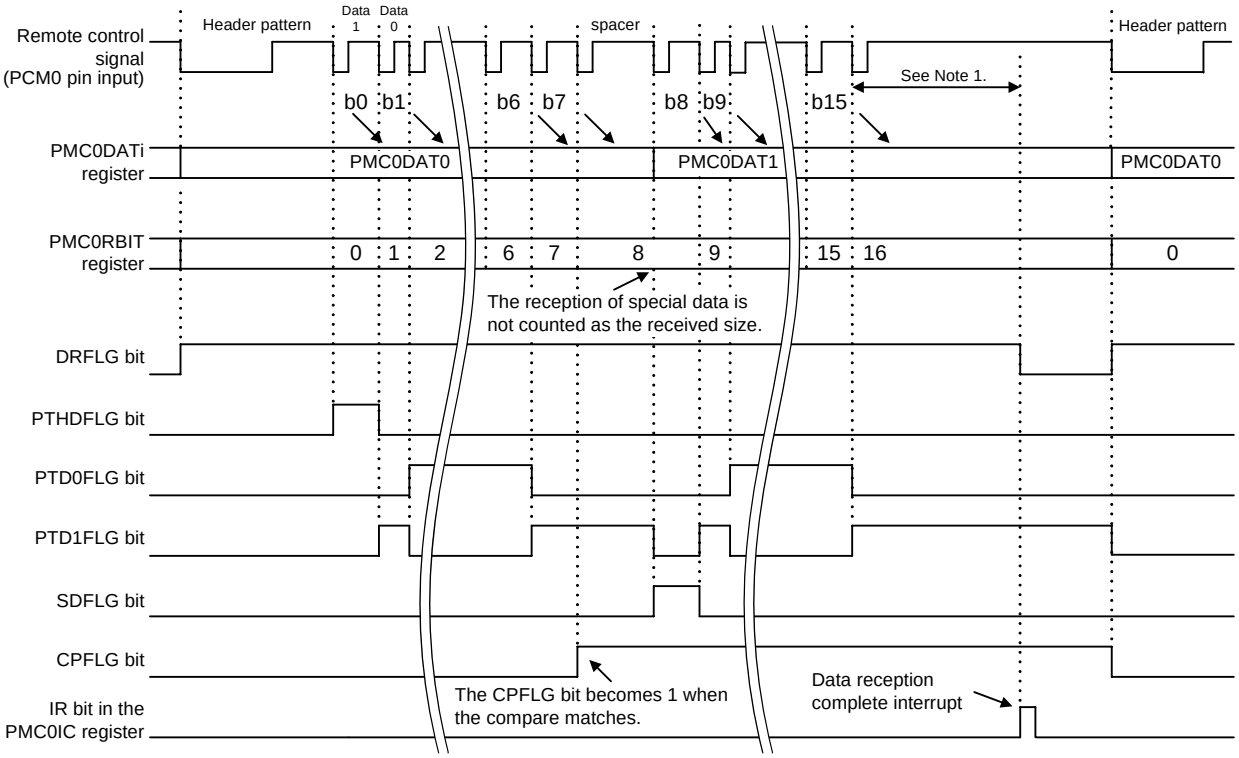


Bit Symbol	Bit Name	Function
EN	PMC1 operation enable bit	1: Operation enabled

Operation

(1) The receive operation starts at the first falling edge of the header.
(2) Store the receive data bit by bit to the PMC0DATi register when receiving data (i = 0 to 5).
(3) After receiving the 16th bit, if a falling edge is not detected by the time the maximum time set to the header, special data, data 0, or data 1 has elapsed, a data reception complete interrupt is generated.
(4) Read registers PMC0DATi and PMC0RBIT using the program in the data reception complete interrupt (i = 0 to 5).

Figure 5.2 shows the condition of the status flags and the interrupt generation timing of the PMC0 and PMC1 circuits in remote control reception.



DRFLG, PTHDFLG, PTD0FLG, PTD1FLG, SDFLG, and CPFLG: Bits in the PMC0STS register
i = 0 to 5
The above assumes the following:
- The SINV bit in the PMC0CON0 register is 1 (inverted), the SDEN bit is 1 (special data pattern enabled), and bits DRINT1 and DRINT0 are 11b (interrupt request is generated when compare match and no receive error occurs, and reception completed).
- The SINV bit in the PMC1CON0 register is 1 (inverted), and the HDEN bit is 1 (header enabled).
- The PMC0INT register is 04h (data reception complete interrupt enabled).
- The CPEN bit in the PMC0CPC register is 1 (compare enabled), and bits CPN2 to CPN0 are 111b (bits 7 to 0 are compared).

Note:
1. The data reception complete interrupt is generated when the counter value is bigger than register PMC0HDPMAX, PMC0D0PMAX, PMC0D1PMAX, or PMC1HDPMAX.

Figure 5.2 PMC0 and PMC1 Combined Receive Operation of the Remote Control Format with Header Pattern and Spacer

5.2 Remote Control Signal Receiver with Header Pattern and Repeat Code

Figure 5.3 shows the outline of the remote control format reception with header and repeat code of the PMC0 and PMC1 combined circuit operation in pattern match mode.

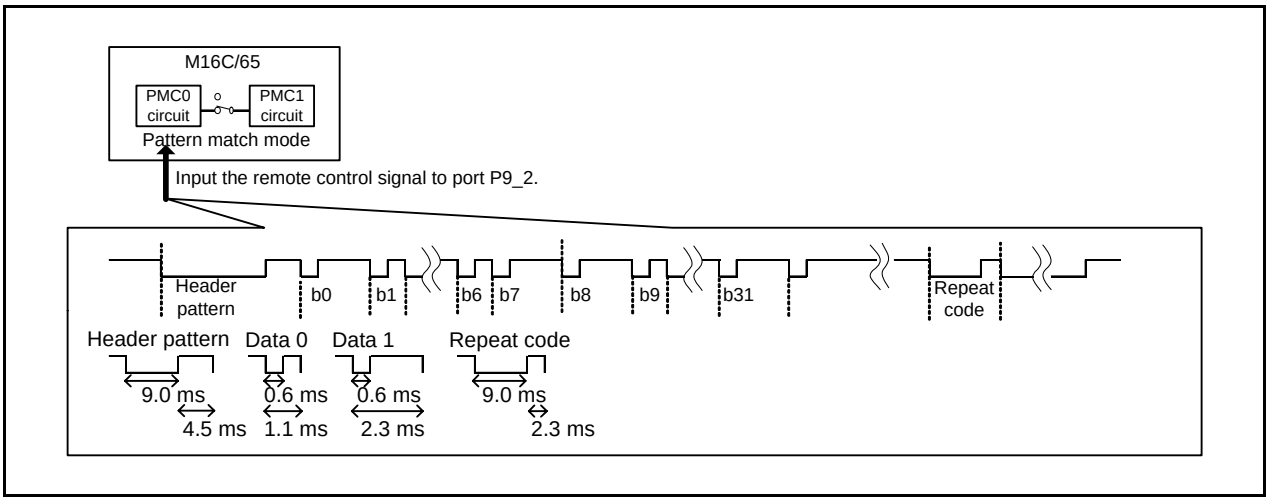


Figure 5.3 Outline of the Remote Control Signal Reception with Header Pattern and Repeat Code

The detection pattern is designed to accept a tolerance of ±10% from the format width shown in Figure 5.3. See the following table for settings.

Table 5.2 PMC0/PMC1 Circuit Settings

Item		Description	
		PMC0 circuit	PMC1 circuit
Count sources	Clock source	fC	
	Division	No division	
Operation mode		Pattern match mode	
Pattern match mode	Detect patterns	Header	Special data pattern
		Data 0 or data 1 match	
	Interrupt request generation timing	Special data match	
		Completion of data reception	
	Selectable functions	Input signal inversion	
		Digital filter	
		Error flag hold	
Input port		P9_2	

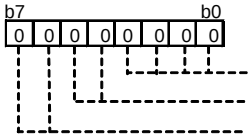
This application note confirms the time measured using timer A0 and repeat code received in the PMC0/PMC1 circuit during a fixed period.
Table 5.3 lists the Timer A0 Settings.

Table 5.3 Timer A0 Settings

Item	Description
Operation mode	One-shot timer mode
Count source	fC32
TA0 register setting value	200 - 1 (200 ms)
Interrupt priority level	Level 1

Register settings

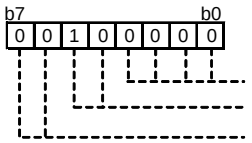
PMC0 Function Select Register 3



Symbol	Address
PMC0CON3	01F3h

Bit Symbol	Bit Name	Function
PD/CST/CFR/CRE	Mode select bit	0000: Pattern match mode
CSRC1 to CSRC0	Clock source select bit	00: Same as PMC1
CDIV1 to CDIV0	Count source divisor select bit	00: No division

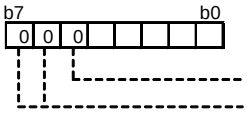
PMC1 Function Select Register 3



Symbol	Address
PMC1CON3	01FBh

Bit Symbol	Bit Name	Function
PD/CST/CFR/CRE	Mode select bit	0000: Pattern match mode
CSRC1 to CSRC0	Clock source select bit	10: fC
CDIV1 to CDIV0	Count source divisor select bit	00: No division

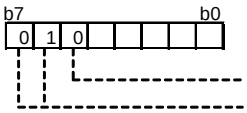
PMC0 Function Select Register 2



Symbol	Address
PMC0CON2	01F2h

Bit Symbol	Bit Name	Function
CEINT	Counter overflow interrupt enable bit	0: Disabled
PSEL1 to PSEL0	Input pin select bit	00: Same as PMC1

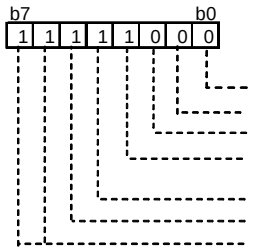
PMC1 Function Select Register 2



Symbol	Address
PMC1CON2	01FAh

Bit Symbol	Bit Name	Function
CEINT	Counter overflow interrupt enable bit	0: Disabled
PSEL1 to PSEL0	Input pin select bit	01: PMC0 pin

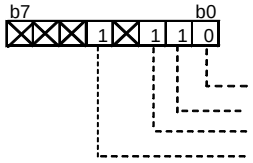
PMC0 Function Select Register 0



Symbol	Address
PMC0CON0	01F0h

Bit Symbol	Bit Name	Function
EN	PMC0 operation enable bit	0: Operation disabled
SINV	Input signal polarity invert bit	Set to 0
FIL	Filter enable bit	Set to 0
EHOLD	Error flag hold bit	Status of the REFLG bit in the PMC0STS register: 1: Held even after next data received
HDEN	Header pattern enable bit	1: Header enabled
SDEN	Special data pattern enable bit	1: Special data pattern enabled
DRINT1 to DRINT0	Receive interrupt control bit	11: Interrupt request is generated when compare match and no receive error occurs, and reception completed

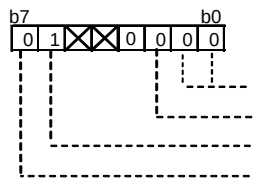
PMC1 Function Select Register 0



Symbol	Address
PMC1CON0	01F8h

Bit Symbol	Bit Name	Function
EN	PMC1 operation enable bit	0: Operation disabled
SINV	Input signal polarity invert bit	1: Inverted
FIL	Filter enable bit	1: Filter enabled
HDEN	Header pattern enable bit	1: Header enabled

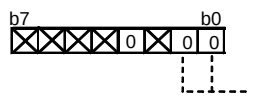
PMC0 Function Select Register 1



Symbol	Address
PMC0CON1	01F1h

Bit Symbol	Bit Name	Function
TYP1 to TYP0	Receive mode select bit	00: Period measurement (between rising edge and rising edge)
CSS	Counter start control bit	0: Counters operate individually
EXSDEN	Special pattern detect block select bit	1: PMC1
EXHDEN	Header pattern detect block select bit	0: PMC0

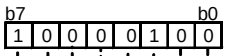
PMC0 Function Select Register 1



Symbol	Address
PMC0CON1	01F1h

Bit Symbol	Bit Name	Function
TYP1 to TYP0	Receive mode select bit	00: Period measurement (between rising edge and rising edge)

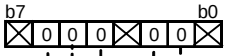
PMC0 Interrupt Source Register



Symbol	Address
PMC0INT	01F5h

Bit Symbol	Bit Name	Function
CPINT	Compare match flag interrupt enable bit	0: Disabled
REINT	Receive error flag interrupt enable bit	0: Disabled
DRINT	Data reception complete interrupt enable bit	1: Enabled
BFULINT	Receive buffer full flag interrupt enable bit	0: Disabled
PTHDINT	Header match flag interrupt enable bit	0: Disabled
PTDINT	Data 0/1 match flag interrupt enable bit	0: Disabled
TIMINT	Timer measure interrupt enable bit	0: Disabled
SDINT	Special data match flag interrupt enable bit	1: Enabled

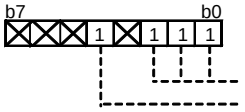
PMC1 Interrupt Source Register



Symbol	Address
PMC1INT	01FDh

Bit Symbol	Bit Name	Function
REINT	Receive error flag interrupt enable bit	0: Disabled
DRINT	Data reception complete interrupt enable bit	0: Disabled
PTHDINT	Header match flag interrupt enable bit	0: Disabled
PTDINT	Data 0/1 match flag interrupt enable bit	0: Disabled
TIMINT	Timer measure interrupt enable bit	0: Disabled

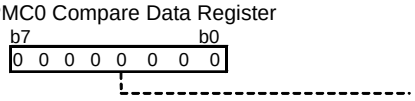
PMC0 Compare Control Register



Symbol	Address
PMC0CPC	01F6h

Bit Symbol	Bit Name	Function
CPN2 to CPN0	Compare bit specified bit	Bits 7 to 0 are compared
CPEN	Compare enable bit	1: Compare enabled

PMC0 Compare Data Register

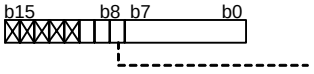


Symbol		
PMC0CPD	01F7h	

Function: Compare with 0000 0000b

See Note 1.

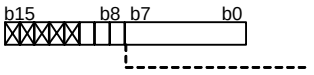
PMC0 Header Pattern Set Register (MIN)



Symbol	Address
PMC0HDPMIN	D081h to D080h

Function: (9.0 + 4.5) [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 397

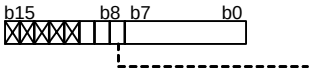
PMC0 Header Pattern Set Register (MAX)



Symbol	Address
PMC0HDPMAX	D083h to D082h

Function: (9.0 + 4.5) [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 486

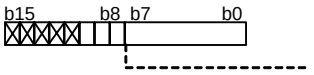
PMC1 Header Pattern Set Register (MIN)



Symbol	Address
PMC1HDPMIN	D095h to D094h

Function: (9.0+ 2.3) [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 332

PMC1 Header Pattern Set Register (MAX)



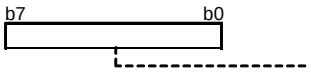
Symbol	Address
PMC1HDPMAX	D097h to D096h

Function: (9.0 + 2.3) [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 406

Note:
1. Set all bits to 0 when the compare match function is not used.
   Check the specification to set the compared value when the compare match function is used.

PMC0 Data 0 Pattern Set Register (MIN)

Symbol	Address
PMC0D0PMIN	D084h

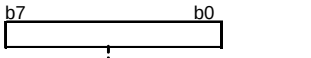


Function

1.1 [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 31

PMC0 Data 0 Pattern Set Register (MAX)

Symbol	Address
PMC0D0PMAX	D085h

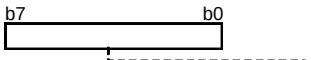


Function

1.1 [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 39

PMC0 Data 1 Pattern Set Register (MIN)

Symbol	Address
PMC0D1PMIN	D086h

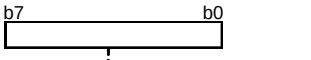


Function

2.3 [ms] × (1 - 0.1) / (1 / 32.768 [kHz]) - 1 = 67

PMC0 Data 1 Pattern Set Register (MAX)

Symbol	Address
PMC0D1PMAX	D087h

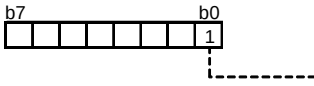


Function

2.3 [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 82

PMC0 Function Select Register 0

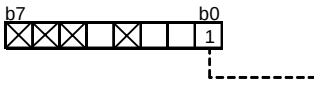
Symbol	Address
PMC0CON0	01F0h



Bit Symbol	Bit Name	Function
EN	PMC0 operation enable bit	1: Operation enabled

PMC1 Function Select Register 0

Symbol	Address
PMC1CON0	01F8h

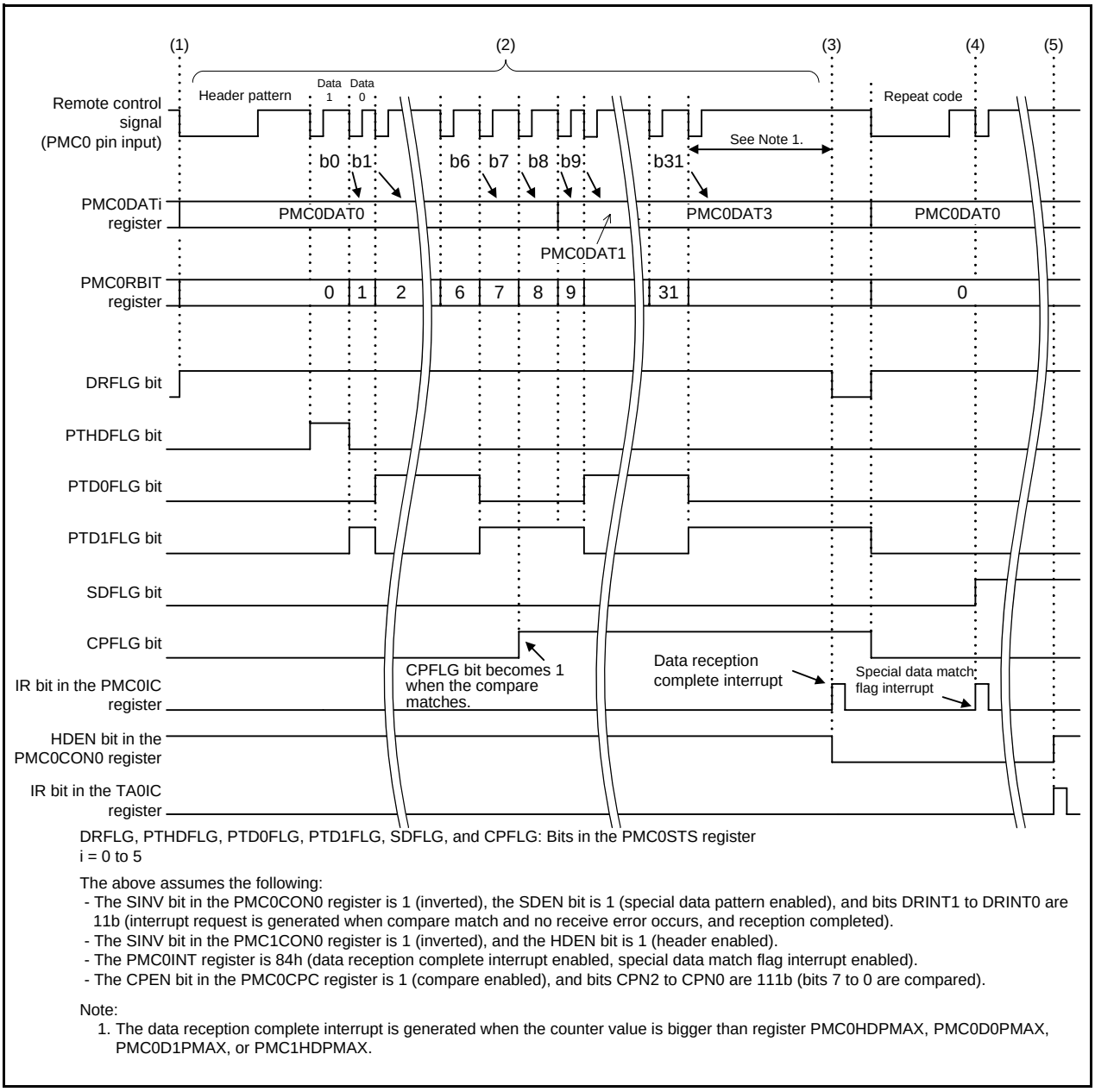


Bit Symbol	Bit Name	Function
EN	PMC1 operation enable bit	1: Operation enabled

Operation

(1) The receive operation starts at the first falling edge of the header.
(2) Store the receive data bit by bit to the PMC0DATi register when receiving data (i = 0 to 5).
(3) After receiving the 32nd bit, if a falling edge is not detected by the time the maximum time set to the header, special data, data 0, or data 1 has elapsed, a data reception complete interrupt is generated. Use a program to read registers PMC0DATi and PMC0RBIT in the data reception complete interrupt. Set the HDEN bit in the PMC0CON0 register to 0 (header disabled) to receive the repeat code. Set timer A0 to one-shot timer mode and start.
(4) The special data match flag interrupt is generated when receiving the repeat code. A trigger for timer A0 is input at the special data match flag interrupt.
(5) If the repeat code is not input, the timer A0 interrupt is generated when the timer A0 counter value becomes 0000h. Set the HDEN bit to 1 (header enabled) in the timer A0 interrupt.

Figure 5.4 shows the condition of the status flags and the interrupt generation timing of the PMC0 and PMC1 circuits when using the remote control signal receiver.



DRFLG, PTHDFLG, PTD0FLG, PTD1FLG, SDFLG, and CPFLG: Bits in the PMC0STS register
i = 0 to 5

The above assumes the following:
- The SINV bit in the PMC0CON0 register is 1 (inverted), the SDEN bit is 1 (special data pattern enabled), and bits DRINT1 to DRINT0 are 11b (interrupt request is generated when compare match and no receive error occurs, and reception completed).
- The SINV bit in the PMC1CON0 register is 1 (inverted), and the HDEN bit is 1 (header enabled).
- The PMC0INT register is 84h (data reception complete interrupt enabled, special data match flag interrupt enabled).
- The CPEN bit in the PMC0CPC register is 1 (compare enabled), and bits CPN2 to CPN0 are 111b (bits 7 to 0 are compared).

Note:
1. The data reception complete interrupt is generated when the counter value is bigger than register PMC0HDPMAX, PMC0D0PMAX, PMC0D1PMAX, or PMC1HDPMAX.

Figure 5.4 PMC0 and PMC1 Combined Receive Operation of the Remote Control Format with Header Pattern and Repeat Code

6. PMC0 Circuit Individual Operation in Pattern Match Mode using Timer Measure Interrupt

6.1 Remote Control Signal Receiver with Header Pattern and Spacer

Figure 6.1 shows the outline of the remote control format reception with header at the PMC0 circuit operation in the pattern match mode.

Every pattern in 1. "Remote Control Signal Receive Waveform" is compatible by using the register settings below.

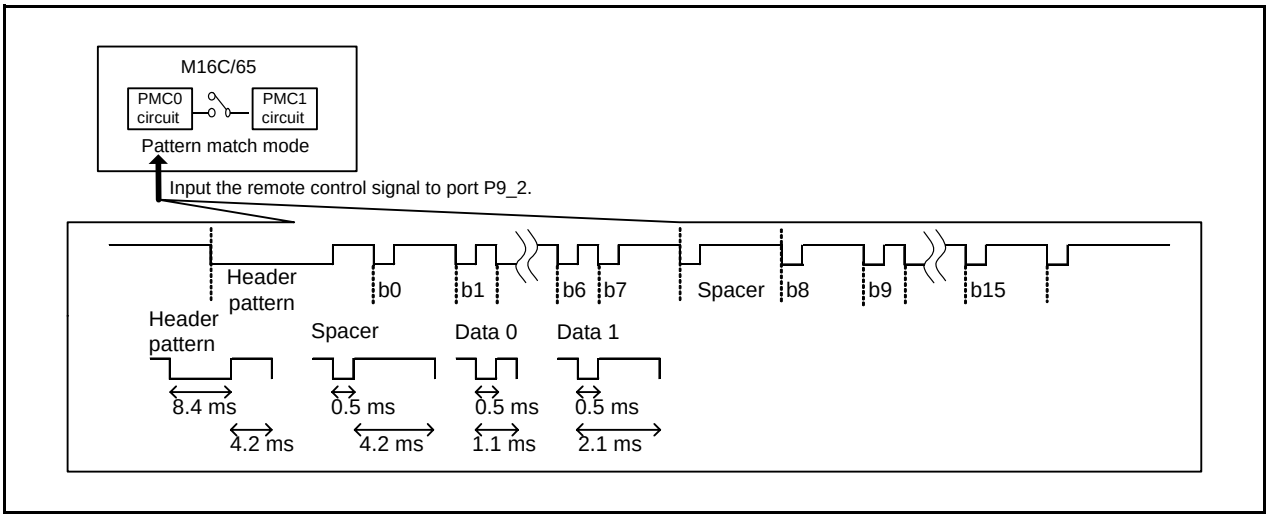


Figure 6.1 Remote Control Signal Receiver with Header Pattern and Spacer

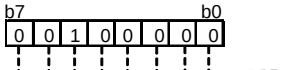
See the following table for settings.

Table 6.1 PMC0 Circuit Settings

Item		Description
Count sources	Clock source	fC
	Division	No division
Operation mode		Pattern match mode
Pattern match mode	Interrupt request generation timing	Timer measurement
		Completion of data reception
	Selectable functions	Digital filter
Input port		P9_2

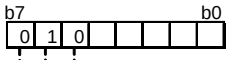
Register settings

PMC0 Function Select Register 3



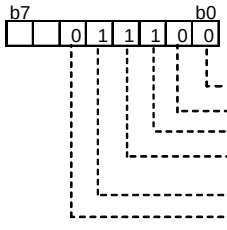
Symbol	Address	
PMC0CON3	01F3h	
Bit Symbol	**Bit Name**	**Function**
PD/CST/CFR/CRE	Mode select bit	0000: Pattern match mode
CSRC1 to CSRC0	Clock source select bit	10: fC
CDIV1 to CDIV0	Count source divisor select bit	00: No division

PMC0 Function Select Register 2



Symbol	Address	
PMC0CON2	01F2h	
Bit Symbol	**Bit Name**	**Function**
CEINT	Counter overflow interrupt enable bit	0: Disabled
PSEL1 to PSEL0	Input pin select bit	01: PMC0 pin

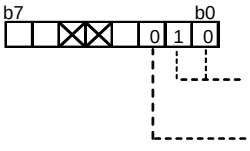
PMC0 Function Select Register 0



Symbol	Address
PMC0CON0	01F0h

Bit Symbol	Bit Name	Function
EN	PMC0 operation enable bit	0: Operation disabled
SINV	Input signal polarity invert bit	0: Not inverted
FIL	Filter enable bit	1: Filter enabled
EHOLD	Error flag hold bit	Status of the REFLG bit in the PMC0STS register: 1: Held even after next data received
HDEN	Header pattern enable bit	1: Header enabled
SDEN	Special data pattern enable bit	0: Special data pattern disabled

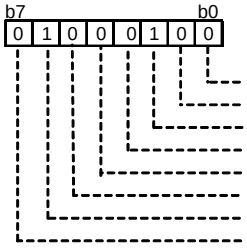
PMC0 Function Select Register 1



Symbol	Address
PMC0CON1	01F1h

Bit Symbol	Bit Name	Function
TYP1 to TYP0	Receive mode select bit	10: Pulse width measurement between rising edge and falling edge, and falling edge and rising edge)
CSS	Counter start control bit	0: Counters operate individually

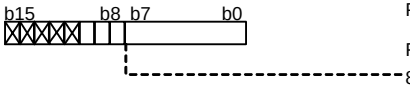
PMC0 Interrupt Source Register



Symbol	Address
PMC0INT	01F5h

Bit Symbol	Bit Name	Function
CPINT	Compare match flag interrupt enable bit	0: Disabled
REINT	Receive error flag interrupt enable bit	0: Disabled
DRINT	Data reception complete interrupt enable bit	1: Enabled
BFULINT	Receive buffer full flag interrupt enable bit	0: Disabled
PTHDINT	Header match flag interrupt enable bit	0: Disabled
PTDINT	Data 0/1 match flag interrupt enable bit	0: Disabled
TIMINT	Timer measure interrupt enable bit	1: Enabled
SDINT	Special data match flag interrupt enable bit	0: Disabled

PMC0 Header Pattern Set Register (MAX)

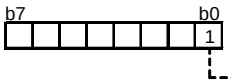


Symbol	Address
PMC0HDPMAX	D083h to D082h

Function

8.4 [ms] × (1 + 0.1) / (1 / 32.768 [kHz]) - 1 = 303

PMC0 Function Select Register 0



Symbol	Address
PMC0CON0	01F0h

Bit Symbol	Bit Name	Function
EN	PMC0 operation enable bit	1: Operation enabled

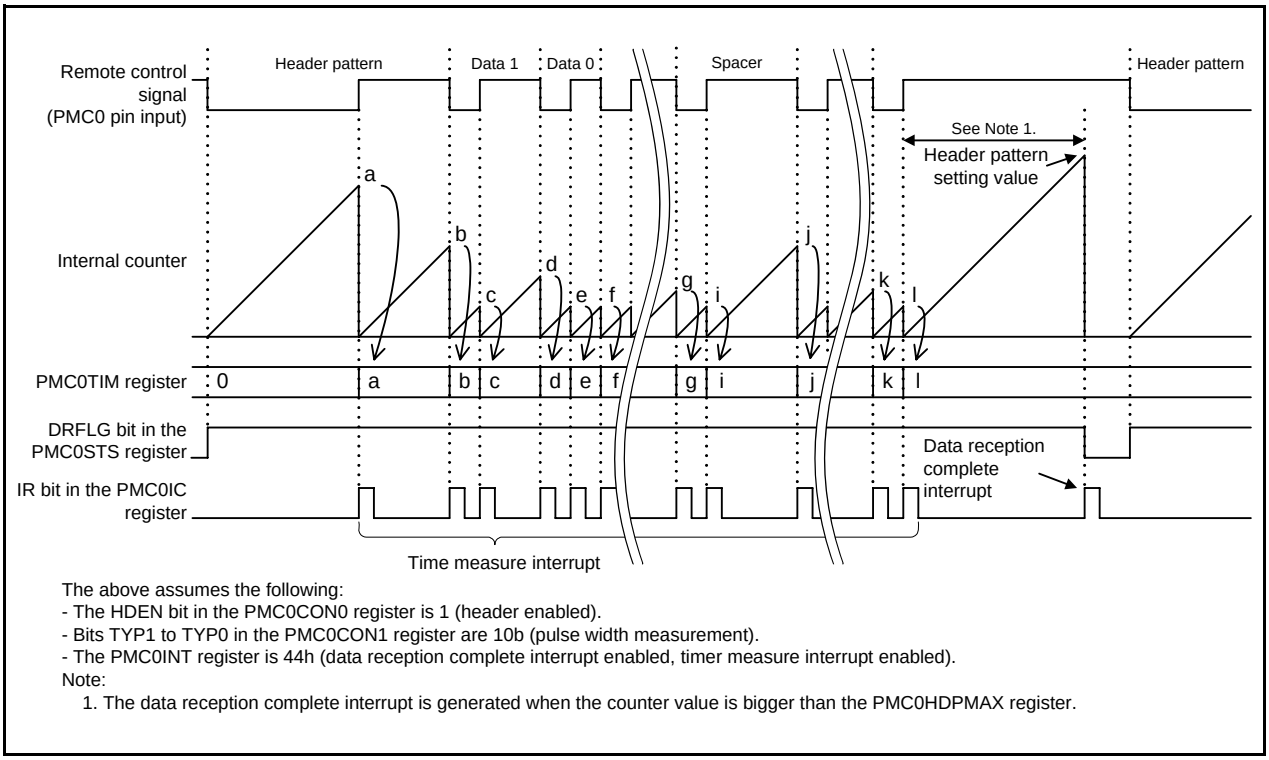


Figure 6.2 Timer Measure Mode Receive Timing in Pattern Match Mode of PMC0 Circuit

In the timer measure interrupt handler, read the PMC0TIM register to obtain each pulse width. (1) During the period that is at or above the maximum value set to the header pattern, if no edge is detected, a data reception complete interrupt is generated. When this interrupt is generated, perform the receive complete handling operation.

Note:

1. When registers PMC0BC and PMC1BC are read, an undefined value may be read.
   Do not use registers PMC0BC and PMC1BC.
   When Registers PMC0TIM and PMC1TIM are read while data changes (edge of the PMC internal input signal), an undefined value may be read. Judge the reading values of registers PMC0TIM and PMC1TIM by reading the registers at least two times.

7. Structure

Declaration	typedef union U_W_STATUS_PM {
	struct S_W_STATUS_PM {
	unsigned char ri0: 1;
	unsigned char rhdd0: 1;
	unsigned char rrpt0: 1;
	unsigned char rerr0: 1;
	unsigned char ri1: 1;
	unsigned char rhdd1: 1;
	unsigned char rrpt1: 1;
	unsigned char rerr1: 1;
	}bit;
	unsigned char all;
	}REM_STATUS_PM;	

Variable	ri0	PMC0 receive completion
	rhdd0	PMC0 header pattern detection
	rrpt0	PMC0 special data pattern match
	rerr0	PMC0 receive error
	ri1	PMC1 receive completion
	rhdd1	PMC1 header pattern detection
	rrpt1	PMC1 special data pattern match
	rerr1	PMC1 receive error
Description	Maintains the status of PMC0 and PMC1.	

8. Function Tables

Declaration	unsigned char RemInitialize(unsigned char ch,unsigned char fmt)	
Outline	Function to initialize remote control signal receiver	
Argument	Argument name	Meaning
	ch	Channel selection 0x01: PMC0 0x02: PMC1 0x03: PMC0 and PMC1
	fmt	Receive format selection 0x00: Remote control format without header pattern 0x01: Remote control format with header pattern 0x02: Bi-phase remote control format 0x03: Remote control format with header pattern and spacer 0x04: Remote control format with header pattern and repeat code 0x05: Remote control format with special data pattern 0x06: Individual Operation of the PMC0 Circuit timer measure interrupt
Variable (global)	Variable name	Value to store
	format	Selected format
	PM_RBIT	Number of received bits
Returned value	Type	Meaning
	unsigned char	INT_OK: Remote control signal receiver setting success
		INT_NG: Remote control signal receiver setting failed
Description	Sets the remote control signal receiver.	

Declaration	unsigned char GetRemStatus(void)	
Outline	Function to obtain status of remote control signal receiver	
Argument	None	
Variable (global)	Variable name	Value to store
	RemStatus.all	The status of remote control signal receiver
Returned value	Type	Meaning
	unsigned char	Status stored on the RAM
Description	Obtains the status stored on the RAM.	

Declaration	unsigned char ClearRemStatus(unsigned char ch)	
Outline	Function to initialize status of remote control signal receiver	
Argument	Argument name	Meaning
	ch	Channel selection 0x01: PMC0 0x02: PMC1
Variable (global)	Variable name	Value to store
	RemStatus.all	The status of remote control signal receiver
Returned value	None	
Description	Initializes the status stored on the RAM.	

Declaration	unsigned char GetPmc0Data(unsigned char *rx_data)	
Outline	Function to store PMC0 buffer data	
Argument	Argument name	Meaning
	*rx_data	Pointer to buffer for receive data
Variable (global)	Variable name	Value to store
	rx_data[]	To store receive data
	Pm0RecvBuf[]	Receive buffer for PMC0
Returned value	Type	Meaning
	unsigned char	0: Storage failed
		1: Storage successful
Description	Receive data in PMC0 is stored in the receive data buffer.	

Declaration	unsigned char GetPmc1Data(unsigned char *rx_data)	
Outline	Function to store PMC1 buffer data	
Argument	Argument name	Meaning
	*rx_data	Pointer to buffer for receive data
Variable (global)	Variable name	Value to store
	rx_data[]	To store receive data
	Pm1RecvBuf[]	Receive buffer for PMC1
Returned value	Type	Meaning
	unsigned char	0: Storage failed
		1: Storage successful
Description	Receive data in PMC1 is stored in the receive data buffer.	

Declaration	void PM0_PmInt(void)	
Outline	Function to receive PMC0 data	
Argument	None	
Variable (global)	Variable name	Value to store
	Pm0RecvBuf[]	Receive buffer for PMC0
	RemStatus.bit	Store the status
Returned value	None	
Description	Carries out the receive operation in PMC0.	

Declaration	void PM1_PmInt(void)	
Outline	Function to receive PMC1 data	
Argument	None	
Variable (global)	Variable name	Value to store
	Pm1RecvBuf[]	Receive buffer for PMC1
	RemStatus.bit	Store the status
	Pm1RecvBitBuf	Receive buffer every bit
	Pm1RecvBitCnt	Counter for the number of bits received in 1 byte
	Pm1RecvByteCnt	Counter for the number of bytes received
	Pm1BitCnt	Counter for the number of bits received
Returned value	None	
Description	Carries out the receive operation in PMC1.	

Declaration	void PM0_TmInt(void)	
Outline	Function to store PMC0 measured values	
Argument	None	
Variable (global)	Variable name	Value to store
	Pm0RecvTimBuf[]	Storage buffer for the PMC0 measured values
	Pm0RecvTimCnt	Counter for PMC0 measured values
Returned value	None	
Description	The results of pulse period/pulse width measurement in PMC0 are stored in the buffer.	

Declaration	void PM1_TmInt(void)	
Outline	Function to store PMC1 measured values	
Argument	None	
Variable (global)	Variable name	Value to store
	Pm1RecvTimBuf[]	Store buffer for the PMC1 measured values
	Pm1RecvTimCnt	Counter for PMC1 measured values
Returned value	None	
Description	The results of pulse period/pulse width measurement in PMC1 are stored in the buffer.	

Declaration	unsigned char RC5_Encode(unsigned char *buff)	
Outline	Function to analyze bi-phase format	
Argument	Argument name	Meaning
	*buff	Receive buffer pointer
Variable (global)	None	
Returned value	Type	Meaning
	unsigned char	0: Encoding failed
		1: Encoding successful
Description	Analyzes data received of bi-phase format. The result is stored in buff[0] and buff[1].	

Declaration	unsigned char RC6_Encode(unsigned char *buff)	
Outline	Function to analyze special header format	
Argument	Argument name	Meaning
	*buff	Receive buffer pointer
Variable (global)	None	
Returned value	Type	Meaning
	unsigned char	0: Encoding failed
		1: Encoding successful
Description	Analyzes the receiving data of special header format. The result is stored in buff[0], buff[1] and buff[2].	

Declaration	void SubClk1Wait(void)
Outline	Function to wait one sub clock cycle
Argument	None
Variable (global)	None
Returned value	None
Description	Generates wait time of one sub clock cycle.

Declaration	void _timer_a0(void)
Outline	Function to handle timer A0 interrupt
Argument	None
Variable (global)	None
Returned value	None
Description	Sets enables header. (This setting is used when receiving the remote control signal of pattern 6.)

9. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

10. Reference Documents

M16C/63 Group User's Manual: Hardware Rev.1.00
M16C/64A Group User's Manual: Hardware Rev.1.10
M16C/65 Group User's Manual: Hardware Rev.1.10
M16C/65C Group User's Manual: Hardware Rev.0.10
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
M16C Series, R8C Family C Compiler Package V.5.45
C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

11. Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry

Revision History	M16C/63, 64A, 65, and 65C Groups Remote Control Signal Receiver Setting by Format Type

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 28, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.
   - "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
   - "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
   - "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

RENESAS

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 1.0