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H8/300L

Low power implementation of SLP (LowPower)

Introduction

In today world, many embedded products are expected to be compact, portable and wearable. In other word, low power design is becoming very important.

Common questions raised during product specification stage are:

- How long does the product last?
- How much power can it consumed?
- What type of battery? Can it be Rechargeable?
- How fast shall be the response time?
- What type of interface is required? LCD? LED? I/O?
- Reliability & Quality level?
- Cost?

Developers who have selected SLP as their microcomputer (MCU) for their lower power application, has already achieved a great power saving in their product. However, if the developers pay more attention to their overall design, further reduction in power can be achieved. As the scope of the topics is very broad, the objective of this application note is to create the awareness and knowledge for low power design.

Topics involved are basic theory, SLP characteristic, SLP peripherals, battery operation, supply regulation, and external interfacing consideration.

Target Device

H8/300L Super Low Power Devices

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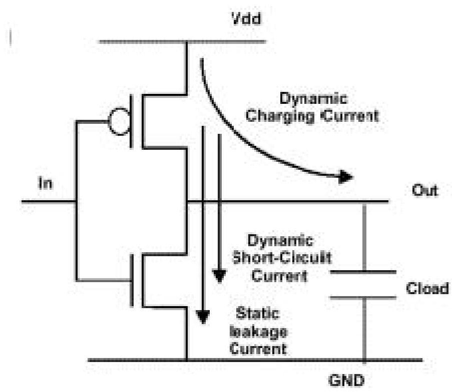
1 Theory

Generally average power consumption can be simplified as:

$$P_{aveage} = P_{short} + P_{leakage} + P_{static} + P_{dynamic}$$



In simple word,

Short-Circuit Power: power dissipated during the short switching interval whereby a short circuit current flow from power to ground

Leakage Power: power dissipated by leakage current through non-conducting transistor & reversed biased diode.

Static Power: power dissipated by current flowing from power to ground during idle time.

Dynamic Power: power dissipated during switching activities.

The dynamic power, which took up 80% of total energy lost can be explain using the fundamental equation

$$P_{dynamic} = a * C * Vcc^2 * F$$

P:	Power
a:	switching activity
C:	Load capacitance
Vcc:	Operational voltage
F:	Frequency

Therefore developers shall

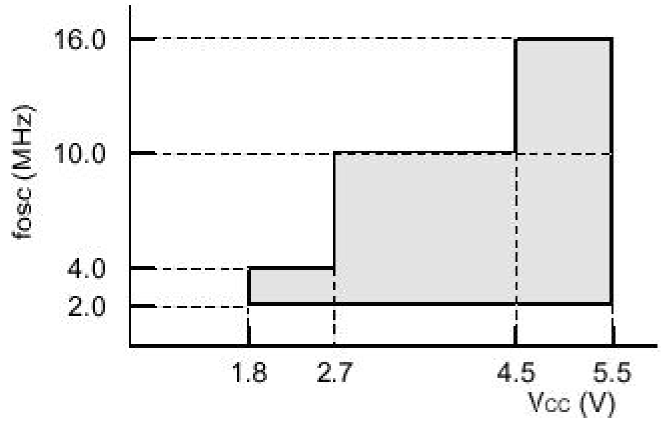
- Reduce the CPU activities/ Switch on the circuit when necessary
- Minimize the output load
- Lower the operating power supply (quadratic effect)
- Operate at the lowest possible frequency

2 SLP (Super Low Power) Characteristics

SLP devices are designed to save power. The various low power features are

2.1 Low & wide range of voltage operation (1.8-5V)

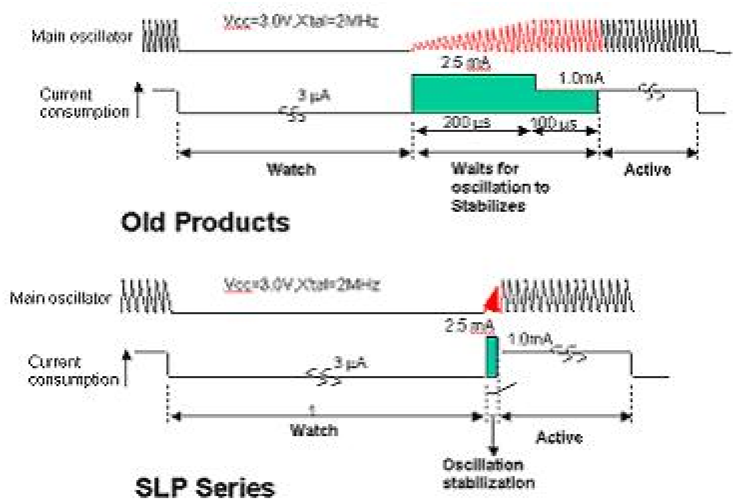
There are not many MCU that is able to support 1.8V operation. As mentioned in the last topics, a lower power supply will lower the power consumption dramatically. The wide operating range will enable the device operation to last longer when the battery voltage has been dropped. E.g if two alkaline battery is used, the system will be able to run from 3V (2x1.5V) to 1.8V(2x0.9V) [The alkaline battery’s cut-off voltage is 0.9 Volts].



2.2 Oscillation Stabilizer Timer Reduction Function (<20 µs)

During mode switching, such as watch to active mode, or exiting from standby mode, there is considerable amount of current flow during oscillation stabilization. SLP has taken steps to reduce such power losses by reducing the oscillation to be less than 20 us.

If the product has frequent mode switching activities, developers have to consider the necessity of such activity, as the average current consume may be larger than when the SLP is operating at other modes.



2.3 Seven Low Power modes

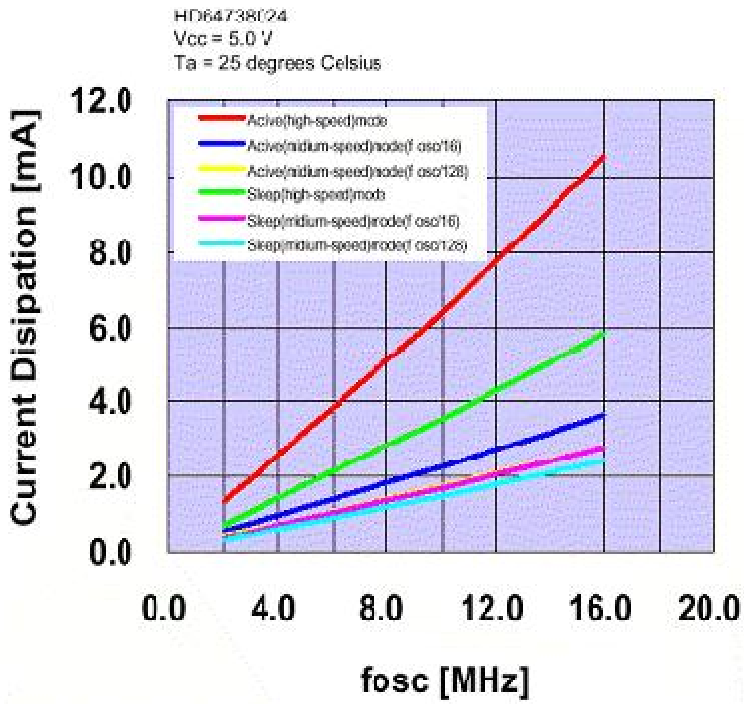
Unlike most other microcomputers, which has only 2-4 types of low power modes (e.g halt, sleep, idle...), SLP has seven low power modes which allow developers to have a better control of their system power consumption. A brief description & typical power consumption is listed as follow:

Operating Mode	Description
Active (high-speed)	The CPU and all on-chip peripheral functions are operable on the system clock in high–speed operation
Active (medium-speed)	The CPU and all on-chip peripheral functions are operable on the system clock in low–speed operation
Subactive	The CPU is operable on the subclock in low-speed operation
Sleep (high-speed)	The CPU halts. On-chip peripherals functions are operable on the system clock
Sleep (medium-speed)	The CPU halts. On chip peripherals functions operate at a frequency of 1/64, 1/32, 1/16, or 1/8 of the system clock frequency
Subsleep	The CPU halts. The time-base function of timer A, timer F, SCI3, AEC and LCD controller/driver are operable on the subclock
Watch	The CPU halts. The time-base function of timer A, timer F, AEC and LCD controller/driver are operable on the subclock
Standby	The CPU and all on-chip peripheral functions halt

The following table shows the typical power consumption at 25 °C temperature from a random sample

Operating Mode	Vcc	Frequency	Icc (typical) 25 °C	Power Consumption*
Active (high-speed)	3V	10 MHz	3.42 mA	10.26 mW
Active (medium-speed)	3V	10 MHz	1.16 mA	3.48 mW
Subactive	3V	32 KHz	19 uA	608 mW
Sleep (high-speed)	3V	10 MHz	2.74 mA	8.22 mW
Subsleep	3V	32 KHz	5.5 uA	16.5 uW
Watch	3V	32 KHz	2.2 uA	6.6 uW
Standby	3V	32 KHz	0.32 uA	0.96 uW

The following charts show the current consumption of the SLP operating at different conditions.



Note: These are indicating reading taken from a random sample.

Observation: Active [medium speed (fosc/16)] has lower current dissipation than Sleep (high speed mode).

More charts are available on-line http://www.hitachisemiconductor.com/sic/jsp/japan/eng/products/mpumcu/816bit/superlow/

2.4 Module standby mode selection

Individual on chip peripheral functions can be put into standby, by mean of disabling the clock input to the modules. This will enable better control over the peripherals usage. i.e. developer may switch any peripheral into active mode only when needed, and thus reducing any unnecessary consumption of current.

2.5 Internal step down VCC

The SLP is designed to operate at very low power!

2.6 Two clocks

There are two independent clocks (a main clock and a 32KHz clock) allowing developers to have a better control over the system design. Developers may run their system at high-speed active mode (operating at speed of main clock) to have better response, and switch to low speed active mode (main clock divided by 16, 32, 64 or 128) to conserve energy. It can further reduced the operating clock by running in sub-active mode (32KHz clock).

3 Usage SLP Peripherals

Other than the distinctive low power features, the SLP peripherals is also designed to be low-power-application friendly. For example, peripherals can still operate when the CPU is stopped. Essential peripherals are built-in, so that less external components are required.

The following table shows how do each features & peripherals react in different operating modes.

Function		Active Mode		Sleep Mode					
		High Speed	Medium Speed	High Speed	Medium Speed	Watch Mode	Subactive Mode	Subsleep Mode	Standby Mode
System Clock Oscliilator		Functions	Functions	Functions	Functions	Halted	Halted	Halted	Halted
Subclock Oscillator		Functions	Functions	Functions	Functions	Functions	Functions	Functions	Functions
Cpu Operation	Instructions	Functions	Functions	Halted	Halted	Halted	Functions	Halted	Halted
	RAM			Retained	Retained	Retained		Retained	Retained
	Registers								
	I/O Port								Retained *1
External Interrupts	IRQ0	Functions	Functions	Functions	Functions	Functions	Functions	Functions	Functions
	IRQ1					Retained*5			
	IRQAEC								Retained*5
	WKP[0-7]	Functions	Functions	Functions	Functions	Functions	Functions	Functions	Functions
Peripheral functions	Timer A	Functions	Functions	Functions	Functions	Functions*4	Functions*4	Functions*4	Retained
	Asynchronous counter					Functions*4	Functions	Functions	Functions*4
	Timer F					Functions/ Retained*7	Functions/ Retained*7	Functions/ Retained*7	Retained
	SCI3					Reset	Functions Retained*2	Functions/ Retained*2	Reset
	PWM					Retained	Retained	Retained	Retained
	ADC					Retained	Retained	Retained	Retained
	LCD					Functions/ Retained*3	Functions/ Retained*3	Functions/ Retained*3	Retained

NOTE: 1. Register contents are retained, but output is high-impedance state.

2. Functions if ∅w/2 is selected as the internal clock; Otherwise halted and retained

3. Functions if ∅w, ∅w/2 or ∅w/4 is selected as the operating clock; otherwise halted and retained.

4. Functions if trhe timekeeping time-base function is selected

5. External interrupt requests are ignored. Interrupt request register contents are not altered.

6. Incrementing is possible, but interrupt generation is not.

7. Functions if the ∅w/4 internal clock is selected; otherwise halted and retained.

3.1 LCD

3.1.1 On Chip Driver & 5V voltage booster

SLP can drive the LCD glass directly, eliminating any extra external components, such as the DC-DC converter. The voltage booster will provide the LCD glass with constant supply, even when the battery voltage is reducing. Thus the application will not have a diminishing LCD contrast level.

If a large LCD glass is used, bypass capacitors must be used to boost the drivability.

3.1.2 Backlight

Backlight can be implemented using either

i. CCFL

ii. EL backlight or

iii. White LED

White LED with the operating range of 3.5-4 Volts and 15-20 mA, will enable a better energy saving than the rest of the implementation.

3.1.3 Low power mode

During low power mode operation, LCD can continue operation if the sub-clock is selected.

3.1.4 Frame frequency

The LCD frame frequency is defined as the rate at which the backplane and segment outputs change. The frame frequency is calculated to be the LCD period/2 * number of backplanes. The range of frame frequencies is from 25 to 250Hz with the most common being between 50 and 150Hz. Higher frequencies result in higher power consumption while lower frequencies cause flicker in the images on the LCD panel

3.2 SCI

SCI is commonly used to communicate with PC for

i. Product update,

ii. Data logging,

iii. Debug purposes

Thus a RS232 driver is required to interface between the two links. However RS232 driver is not welcome in low power design. Developers can

i. Built the driver externally and plug-on when required

ii. Switch off the driver totally when it is not required. (Beware of leakage current)

iii. Use a lower the Baud rate, if speed of transfer is not a concern.

3.3 I/O Port

Matching the characteristic of each I/O port to the required operation or function is essential. Other than the usual input and output ports, SLP has the following port

3.3.1 High current output port (Port 9 & 3)

Port 9(0,1,2) can output as high as 25 mA of current, whereas port 3(1-7) and port 9(3,4,5) can output 10mA. This provides a simple interface to drive LED or other components that required high current drive. Note port 9 is a open drain output whereas port 3 is not.

3.3.2 High Voltage input port (IRQAEC)

IRQAEC is an input pin that can withstand an input that exceeds its VCC level (max of 7.3V).

3.3.3 Pull-up MOS port (Port 3,5,6)

When interfacing to external devices, developers should consider the need of pull up. If it is required, usage of resistor value must be calculated to provide just enough current drive, if otherwise extra power will be lost. The built in MOS pull up must not be enabled unnecessary, as it can provide to a maximum current of 300 uA.

3.4 IRQ/WK pins

There are two external IRQ interrupt and 8 wake up pins. These provide a very good source of obtaining external events, when SLP CPU is stop operating during the low power modes. Examples, SLP will know which of the wake-up pins had been activated, to wake it up from standby modes. This enabled the SLP to perform the necessary action.

3.5 PWM

The PWM can be used in many applications, such as DAC, tone generation, DTMF generation…

3.6 ADC

An unavoidable peripheral required to interfaces to the analogues world.

3.7 AEC

The Asynchronous Event Counter is able to latch external events even during watch and standby modes.

4 Battery operation

Portable products depend on battery for the source of energy. The operating life span of these products will be determined by the capacity of this energy source, and the energy drawn by the rest of the system. Studies had shown that the amount of energy that can be supplied by a given battery varies significantly, depending on how the energy is being drawn.

4.1 Type of Battery

The following compare some of the commonly available batteries.

	Alkaline	Nickel Cadmium (NiCd)	Nickel Metal Hydride (NiMH)	Lithium-ion
Nominal Voltage	1.5	1.25	1.25	3.6
Operating Voltage	1.25 -1.15	1.25 -1.00	1.25 – 1.00	2.5 – 3.0
End of Life	0.9	0.9	0.9	0.9
Operating Temperature	-20 – 55 C	-40 – 60 C	-20 – 60 C	-20 – 60 C
Energy Density (Wh/Kg)	150	45-80	60-120	100
Capacity	30 mAh to 45Ah	150 mAh to 4Ah	500 mAh to 5Ah	35 mAh to 4Ah
Load Current Peak Best result		20C 1C	5C 0.5C or lower	>2C 1C or lower
Advantages	High capacity, good low temp	Low cost, high discharge rate,	Twice capacity than Nicad	High energy densities and cycle life, longer life
Limitation		Low energy density, toxicity	Shorter cycle life, more expensive, inefficient high discharge rate	Unsafe, more expensive
Relative cost	Low	Medium	High	High
Type	Primary	Secondary	Secondary	Primary
Application	Portable entertainment devices, defense devices	Camera, medical devices, power tool	Mobile phone, laptop	Camera, notebook computer, cell phone

4.2 Battery usage

Few points to note while designing the system:

4.2.1 Premature voltage cut-off

The developed system should fully utilize the battery's stored energy. The system should not cut off prematurely before the end-of-discharge voltage is reached and precious battery power remains unused. e.g. The system, using the Li-ion should not cut-off at 3.3V as the Li-ion can be discharged to 3V and lower.

4.2.2 Current discharge rate

Battery can be discharge in three different load conditions;

i. Constant resistance

ii. Constant current, and

iii. Constant power.

Constant Resistance Load will cause excessive and rapid current flow as the discharge voltage fell. This caused a shorter operating life span.

Constant Current Load condition maintains a steady rate of current flow. The average current as compare to constant resistance mode will be smaller. Thus discharge time to the end voltage will also be increased.

Constant Power Load condition has the lowest average current drawn, and therefore has the longest life. During discharge, the current is lowest at the beginning of the cycle and increased as the battery voltage drops. Under this condition, the battery can be discharged below its end voltage.

5 Power Supply Regulation

Below give a quick and simple comparison of Linear and Switching Regulators

	Linear	Switching
Function	**Only step down**. Input voltage must be greater than output	**Steps up or down, or inverts.**
Efficiency	**Low to medium**, but actual battery life depends on load current and battery voltage over time. **High** if Vin-Vout difference is small.	**High,** except at very low load currents (uAmps), where switch-mode quiescent current is usually higher.
Waste Heat	**High** if the average load and/or the input/output voltage differences are high	**Low.** Components usually run cool for power levels below 10 watts.
Complexity	**Low**. Usually requires only the regulator and low value bypass capacitors.	**Medium to high.** Usually requires inductor, diode, and filter caps in addition to IC. For high power circuits, add external FETs.
Size	**Small to medium** in portable designs, but can be larger if heatsinking is needed	Larger than linear at low power, but smaller at power levels for which linear requires a heatsink.
Total Cost	**Low.**	**Medium to high**, largely due to external components.
Ripple/Noise	**Low**. No ripple, low noise. Better noise rejection.	**Medium to high,** due to ripple at switching rate

Linear regulation is a commonly adopted design due to its simplicity and cost. The main drawbacks are its efficiency and heat generation. However the actual effect of measured efficiency is quite adequate when considered over the battery's full discharge cycle. Another consideration factor is the justification of the prolonged battery life against the cost reduction.

6 Consideration for External Interfacing

A wrongly configured and selected part may cause much harm to the low power application. A general advises is to use energy saving parts and avoid the following parts:

i. Optically isolated devices

ii. Electro-mechanical relay

iii. Backlight

iv. Serial communication

The reduction of components count is a form of power saving too. However factors such as reliability, safety and cost must be put into consideration.

6.1 Low power parts

Many components have been designed for low power and its data sheet will explicitly defined its low power characteristics, such as lower operating and quiescent current, low voltage operation…etc. For example;

- 74LVCI low voltage CMOS Logic (1.65-5.5 V operation)
- 74LVC low voltage CMOS Logic (2.7-3.6V with 3.3/5 V tolerant input)
- Ultra low power CMOS SRAM
- Low power Operational Amplifier

6.2 Pull up/down resistor

The value of pull up/down resistor should be deal with too. Although the difference between the usage of a 10K and a 100K resistor in a 3.3 Volts system may be just a mere 30uA, but if comparison is made with the total system (e.g SLP consume 19uA during sub-active mode), the power lost is considered enormously.

6.3 Unused pins

It is necessary to pull up or down the input pins. Floating pins will cause the increase of switching current. A recommended value is 100K ohms resistor. For I/O ports, set the pins to be output, and set it permanently high.

The AVcc must be tied to the Vcc pin even if it is not used.

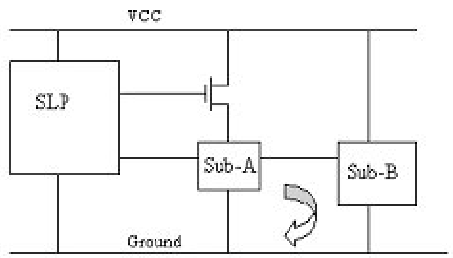
6.4 Driving of LED

LED is commonly used as a form of indicator for the human eye. Since the human eye can retain an image for about 1/60 the second. The LED can be drive periodically in order to save power. Moreover LED can be pulsed for two times its nominal current rating, at 50 % duty cycle, this will make the LED to appear brighter than driving it at nominal current rating at 100 % duty cycle (Mathematically, the average current consumed is the same)

Developers have to choose the correct type of LED for their application. Consideration must be made for the viewing angle, size, colour, brightness and more importantly the typical current consumption. A normal LED consumes about 10-30 mA of current, whereas the low current type is designed to draw only 2 mA of current.

6.5 Switching off external devices

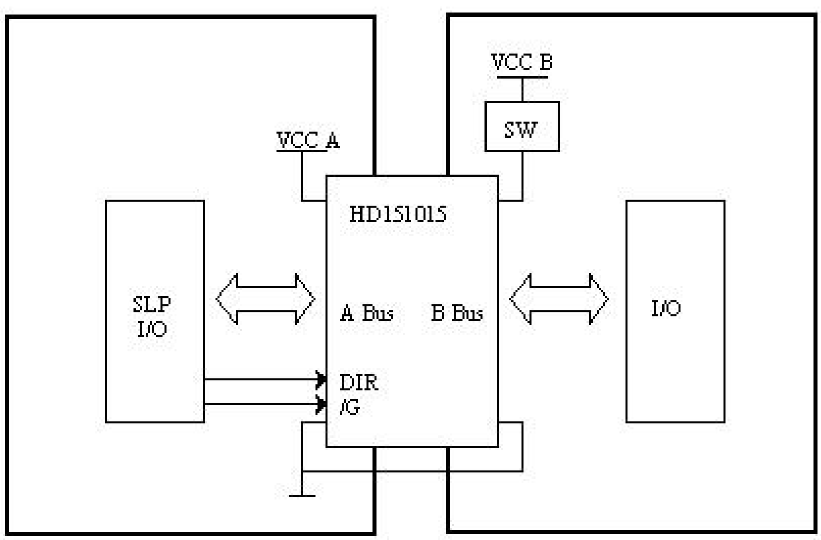
SLP may switch off its internal peripherals easily using the module standby register. However if developers are to integrate power switch to cut off power supply to other subsystem, the following factors must be consider:



When the subsystem is turned-off, will it cause loading to other sub-system?

When the battery power supply is lowered, will it cause the subsystem to malfunction earlier due to voltage dropped across the power switch?

An example using Hitachi HD151015 (9-bit level shifter/Transceiver with 3 state Output) is shown as follows:



Enable Input (G) should be 'High' when VCC B is off

6.6 Analogue Signal

Do not feed analog signal into a digital input. The analog level will cause more current flow at the digital input. An amplifier or a schmitt-trigger can be used as a conditioner.

6.7 High impedance states during standby

During standby mode, SLP output ports are in the high impedance states. Developers have to consider this case as this may cause external peripherals to goes into an unknown state. Pull up or down resistor may be necessary.

6.8 Driving state during low power operation

The designed system will operate in the lowest power mode in most of the time (perhaps 90% of its life span). Thus extra effort must be made to consider the power consume during this period of time. All components must be put into the off state or the lowest power states.

7 System power consumption & life span calculation

In order to know how long the product can last with a particular battery, the average power consumption of the system must be calculated.

For a simplified case, let assume the following

- The board contains only the SLP device.
- SLP operates on only two modes: active medium and standby.
- Two 1.5 Volts 1500mAhr alkaline batteries are used.
- The SLP will cycles itself between active medium speed and standby modes. (The initial power up stage can be ignored in the calculation.)
- The current consumption remain constant (ignoring the other factors such as temperature changes, battery voltage drops…

Mode	Current	Time Taken	% covered
Power Up	25mA		
Active High Speed	3 mA		
Active Medium (fosc/128)	1 mA	10 msec	about 10 %
Oscillation	25 mA	20 usec	about 0 %
Standby	0.32 uA	90 msec	about 90 %

Total time taken for 1 cycle = (10 msec + 20 usec + 90 msec)
= 100 msec (approximation)

Average current consume = (10 % * 1mA) + (0% * 25 mA) + (90% * 0.32uA)
= 100 uA (approximation)

No of hours the battery can last = 1500 mAhr / 100 uA
= 15 000 hrs
= 625 days
= 21 months (approximation)

Note: when more components are added into the board, the total current may not be the summation of all the components quiescent current (as shown in the data sheet). The effective loading effect of components will affect the quoted value in the data sheet.

The easier method is to measure the actual current consumed at different operating modes /states.

8 Conclusion

Topics covered in this application note raised several low power considerations. Developers are advised to explore further as each application's expectation is different. The most contradicting factor will be Cost. The implementation of each topics are not detailed in this notes, developers have to refer to each devices hardware manual for the exact setting.

The topics raised in this application note can also be applied to the other MCU. However there are more topics to be covered for higher end application. Topics such as, bus width consideration, speed partitioning of the whole system, coding consideration…

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.03	-	First edition issued

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