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# M16C/65 Group

## Long-period timers

## 1. Abstract

In this process, Timer A0 and Timer A1 are connected to make a 16-bit timer with a 16-bit prescaler. Use the following peripheral function:

- Timer mode of timer A
- Event counter mode of timer A

#### 2. Introduction

This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.



#### 3. Introduction

- (1) Set timer A0 to timer mode, and set timer A1 to event counter mode.
- (2) Perform a count on count source fITIMAB using timer A0 to count for 1 ms, and perform a count on timer A0 using timer A1 to count for 1 second.
- (3) Connect a 20MHz oscillator to XIN.
- (4) Using POFSi bit in TAPOFS register to select the output polarity of the TAiOUT pin.

## 4. Operation

- (1) Setting the count start flag to "1" causes the counter to begin counting. The counter of timer A0 performs a down count on count source flTIMAB.
- (2) If the counter of timer A0 underflows, the counter reloads the content of the reload register and continues counting. At this time, the timer A0 interrupt request bit goes to "1". The counter of timer A1 performs a down count on underflows in timer A0.
- (3) If the counter of timer A1 underflows, the counter reloads the content of the reload register and continues counting. At this time, the timer A1 interrupt request bit goes to "1".



Figure 1 shows the operation timing.

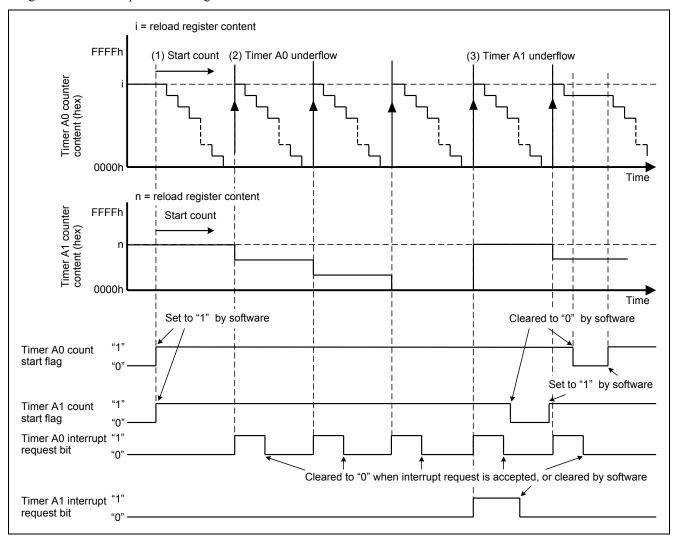


Figure 1. Operation timing of long-period timers

Figure 2 shows the connection diagram.

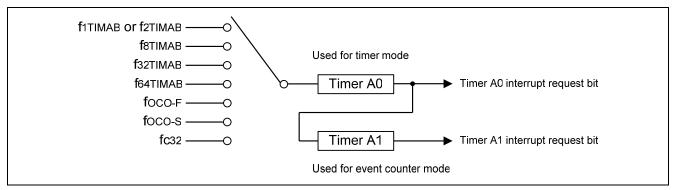


Figure 2. Connection diagram of long-period timers



## 5. Set-up procedure

Table 1 shows Timer A count source, Figure 3 shows block diagram of Timer A count source in timer mode.

**Table 1. Count Source Selection of Timer A** 

TCKDIVC0 register (Note 1)	TACSj register (Note 2)				TAiMR register		Count source	Count source period
TCDIV00	TCS3/ TCS7	TCS2/ TCS6	TCS1/ TCS5	TCS0/ TCS4	TCK1	ТСК0		f(Xin):20MHz f(Xcin):32.768kHz f(oco-F):about 20MHz f(oco-s):about 125kHz
0	0	-	-	-	0	0	f1TIMAB/ f2TIMAB (Note 3)	50ns/100ns
0	0	-	-	-	0	1	f8TIMAB	400ns
0	0	-	-	-	1	0	f32TIMAB	1600ns
0	0	-	-	-	1	1	fc32	976.56µs
0	1	0	0	0	-	-	f1TIMAB/ f2TIMAB (Note 3)	50ns/100ns
0	1	0	0	1	-	-	f8TIMAB	400ns
0	1	0	1	0	-	-	f32TIMAB	1600ns
0	1	0	1	1	-	-	f64TIMAB	3200ns
0	1	1	0	0	-	-	foco-F	about 50ns
0	1	1	0	1	-	-	foco-s	about 8µs
0	1	1	1	0	-	-	fc32	976.56µs
1	1	0	0	0	-	-	f1TIMAB/ f2TIMAB (Note 3)	about 50ns/100ns
1	1	0	0	1	-	-	f8TIMAB	about 400ns
1	1	0	1	0	-	-	f32TIMAB	about 1600ns
1	1	0	1	1	-	-	f64TIMAB	about 3200ns

Note 1: TCDIV00 bit is clock select prior to timer AB division bit. Set the TCDIV00 bit before setting other registers associated with timer A. After changing the TCDIV00 bit, set other registers associated with timer A again.

Note 2: TCS3~TCS0 bits of TACS0 register correspond to Timer A0 count source selection, TCS7~TCS4 bits of TACS0 register correspond to Timer A1 count source selection, TCS3~TCS0 bits of TACS1 register correspond to Timer A2 count source selection, TCS7~TCS4 bits of TACS1 register correspond to Timer A3 count source selection, and TCS3~TCS0 bits of TACS2 register correspond to Timer A4 count source selection. Note 3: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0", the selected clock source is f2TIMAB.

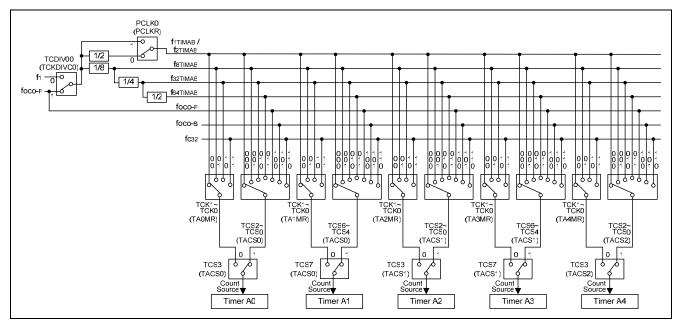
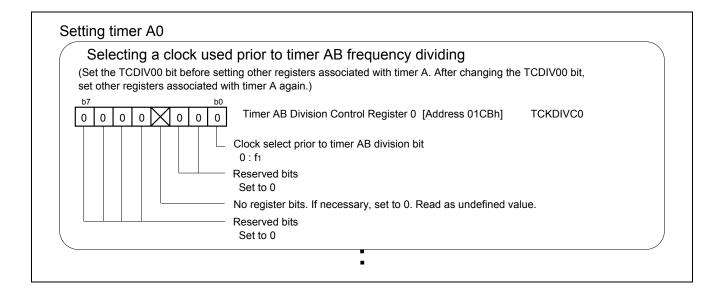
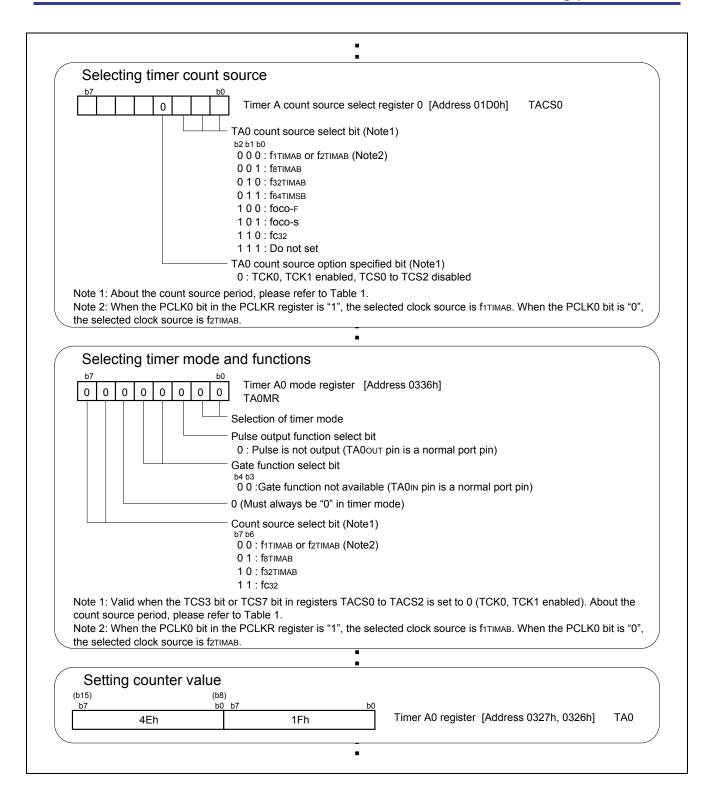


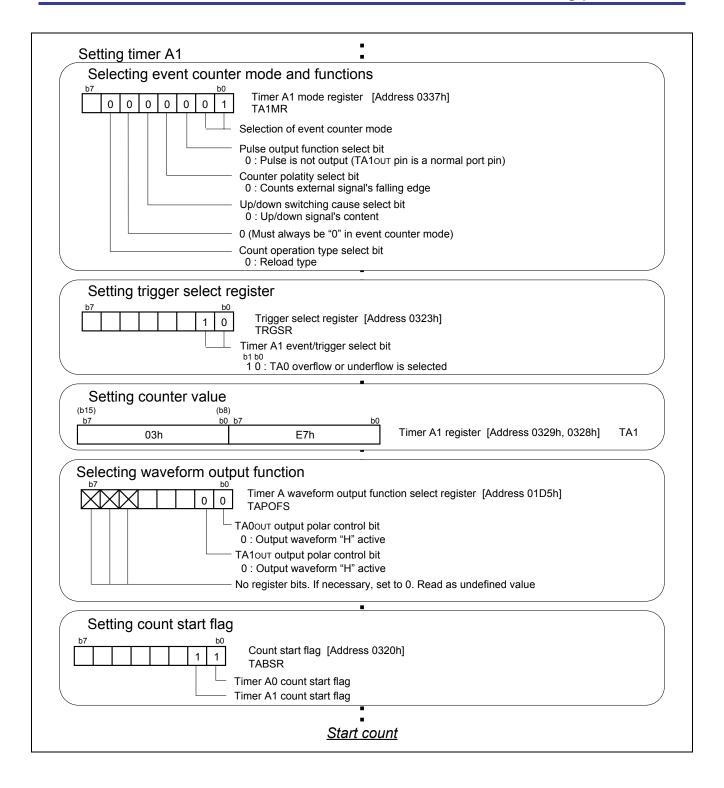
Figure 3. Count source of Timer A













## 6. Reference

Hardware manual

M16C/65 Group Hardware Manual

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## Revision

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