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Renesas Electronics Corporation

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H8SX Series

Long-Cycle Pulse Output

Introduction

As well as having an architecture that is upward-compatible with each CPU of the H8/300, H8/300H, and H8S series, so as to inherit a full complement of peripheral functions, the H8SX microcomputer series has a maximum operating frequency of 50 MHz and uses a 32-bit H8SX core CPU as well as an on-chip multiplier/divider to improve performance.

This H8SX series Application Note provides information you may be need during software and hardware design. This is a basic edition that provides operation examples that each use a single H8SX series on-chip peripheral function.

Although the operation of each program, circuit, and other aspects covered by this application note has been checked, make sure that you conduct your own operation checks before actually using the H8SX series.

Contents

1. Overview

Two channels of the 16-bit timer pulse unit (TPU) of the H8SX series output long-cycle pulses. Two cascaded 16-bit timer channels can act as a 32-bit counter to output long-cycle pulses.

2. Configuration

The following example cascades channel 2 and 1 of the 16-bit timer pulse unit (TPU) to enable their use as a 32-bit timer counter. Then it outputs pulses of any duty cycle from the output compare output pin (TIOCA1) of channel 1. When the peripheral module clock (Pϕ) is 25 MHz and the count clock is Pϕ/1, you can set any output pulse cycle between 5.24 msec and 171.79 sec in units of 2.62 msec. You can set the duty with a resolution of 1/65535.

In the following explanation, channel 2 of the 16-bit timer pulse unit is called TPU2 while channel 1 is called TPU1.

The following combinations of channels can be cascaded: TPU2 and TPU1 or TPU5 and TPU4. For this operation, the TPU2/TPU1 combination is used. The timer counter (TCNT_2) of TPU2 indicates the 16 low-order bits of the 32-bit counter while the timer counter (TCNT_1) of TPU1 indicates the 16 high-order bits of the 32-bit counter.

Figure 1 is a block diagram of long-cycle pulse output.

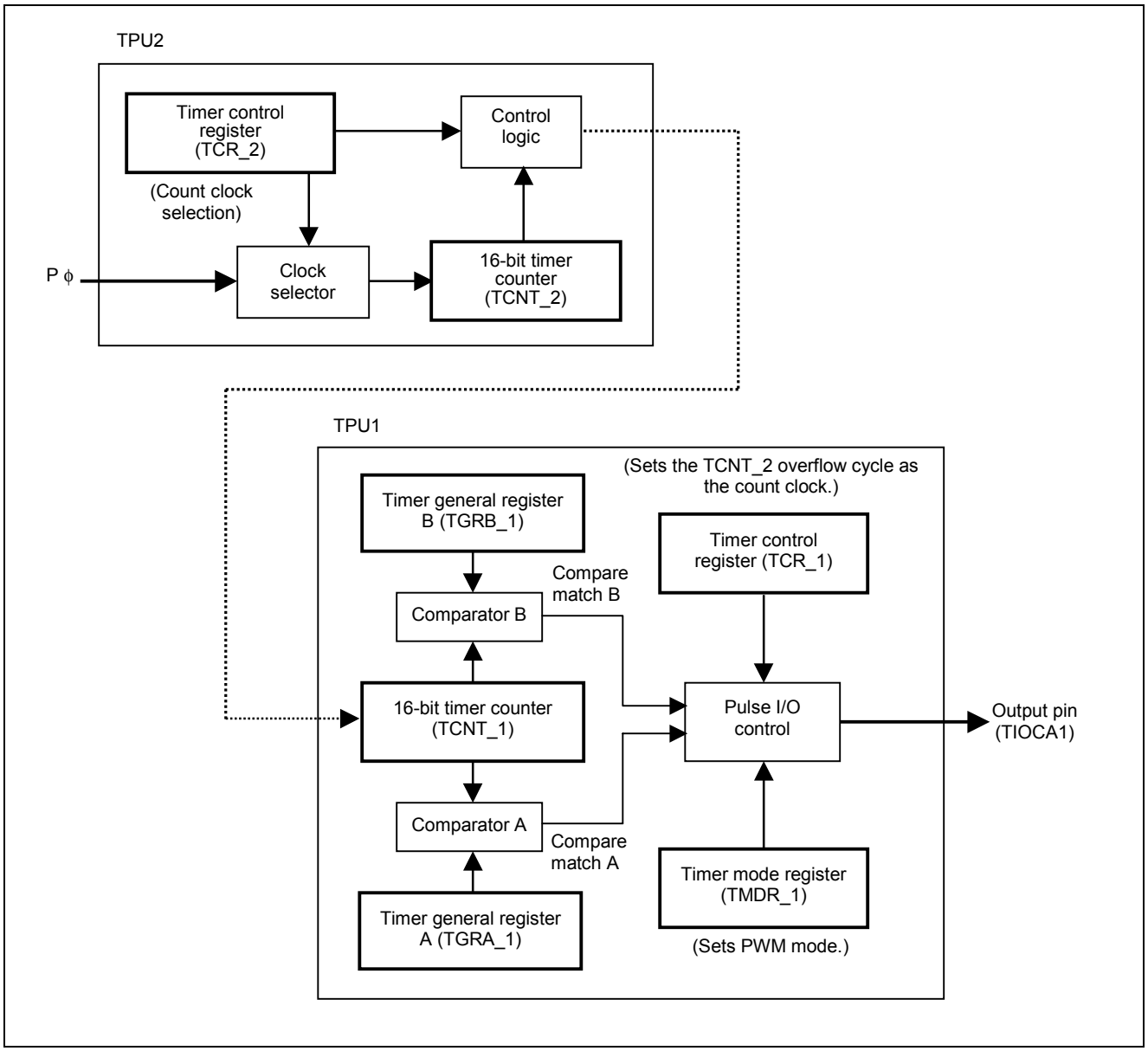


Figure 1 Block Diagram of Long-Cycle Pulse Output

3. Sample Program

3.1 Function

This sample program outputs pulses with the low and high pulse widths according to the timer values. You can calculate the timer value for a pulse width by using the following equation:

pulse-width = timer-value × TPU1-count-clock

In this configuration, the TPU1 count clock is the overflow cycle of TCNT_2. Therefore, the TPU2 count clock × (2**16) is applied.

In this example, assume that the TPU2 count clock is peripheral module (Pϕ)/1. When Pϕ is 25 MHz, the TPU2 count clock is 40.00 nsec and the TPU1 count clock is 2.62 msec. Figure 2 shows an example of operation.

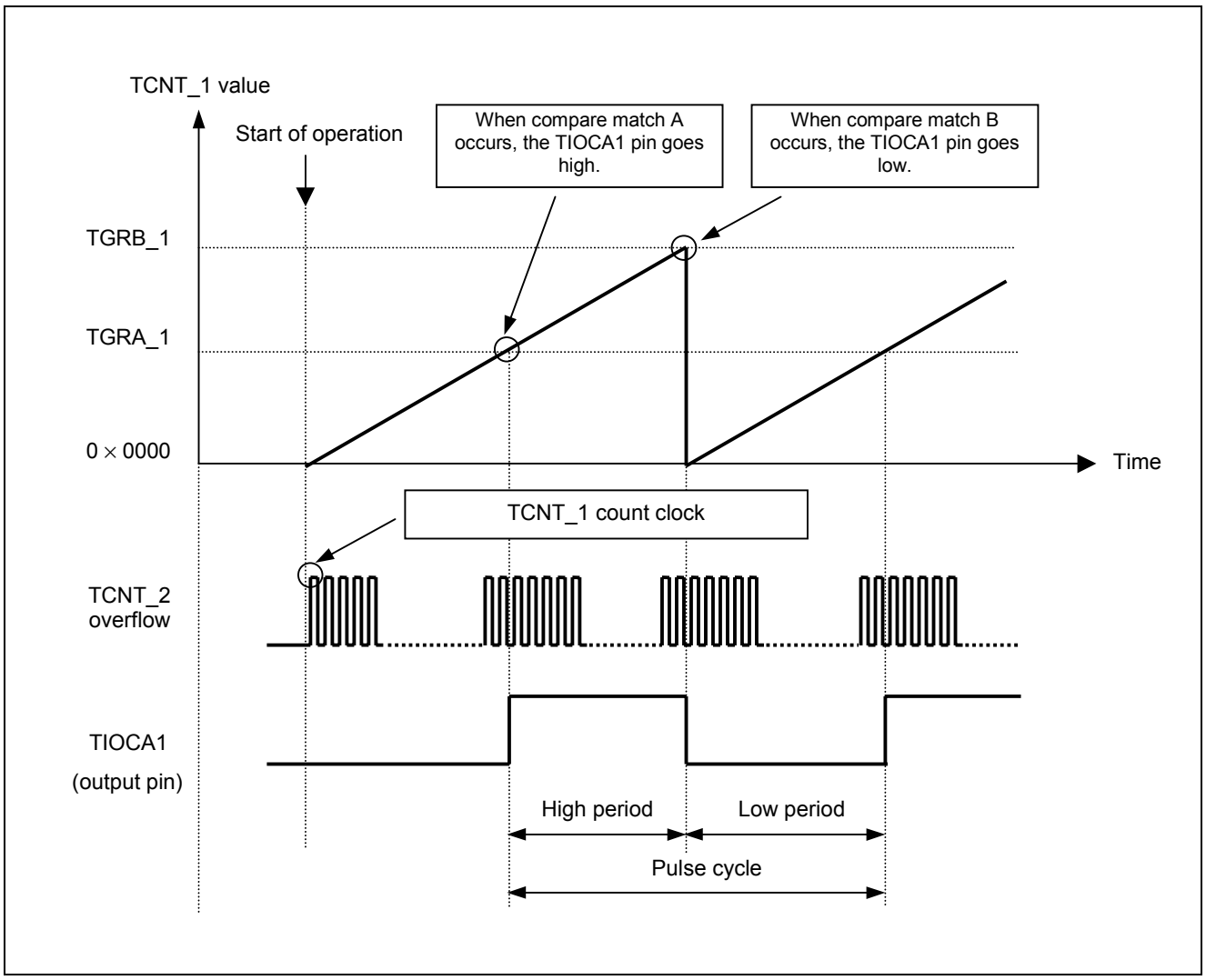


Figure 2 Example of Pulse Output Operation

Table 1 lists the function allocations of the 16-bit timer pulse unit (TPU) being used.

Table 1 Function Allocations of TPU

Type		Name	Function
Common	Register	MSTPCRA	Cancels the TPU module stop mode.
		TSTR	Specifies whether to start or stop the timer count of TPU channels 1 and 2.
TPU 2	Register	TMDR_1	Sets the TPU 1 operating mode (PWM mode 1).
		TCR_1	Sets the TCNT_1 count clock and counter clear factor.
		TIOR_1	Sets the output level when compare match A or B occurs.
		TGRA_1	Sets the counter value of compare match A.
		TGRB_1	Sets the counter value of compare match B.
	Output pin	TIOCA1	Compare match A and B output pin.

3.2 Function Specifications

The function that sets long-cycle pulse output is given as a sample program. The function specifications are listed below.

```
void  lpulse_set ( unsigned short  low_ count, unsigned short  cyc_count )
```

Argument	Description
low_count	Specifies the value of the 16 bits of the timer value for the low pulse width. The valid data range is between 0 × 0001 and 0 × FFFE. low_count must be smaller than cyc_count. If 0 × 0000 is specified, or if low_count is greater than or equal to cyc_count, normal operation is not performed. The count clock is fixed to Pϕ/1.
cyc_count	Specifies the value of the 16 bits of the timer value for the pulse cycle. The valid data range is between 0 × 0002 and 0 × FFFF. cyc_count must be greater than low_count. If 0 × 0000 is specified, or if cyc_count is smaller than or equal to low_count, normal operation is not performed. The count clock is fixed to Pϕ/1.

Return value	Description
None	—

Example)

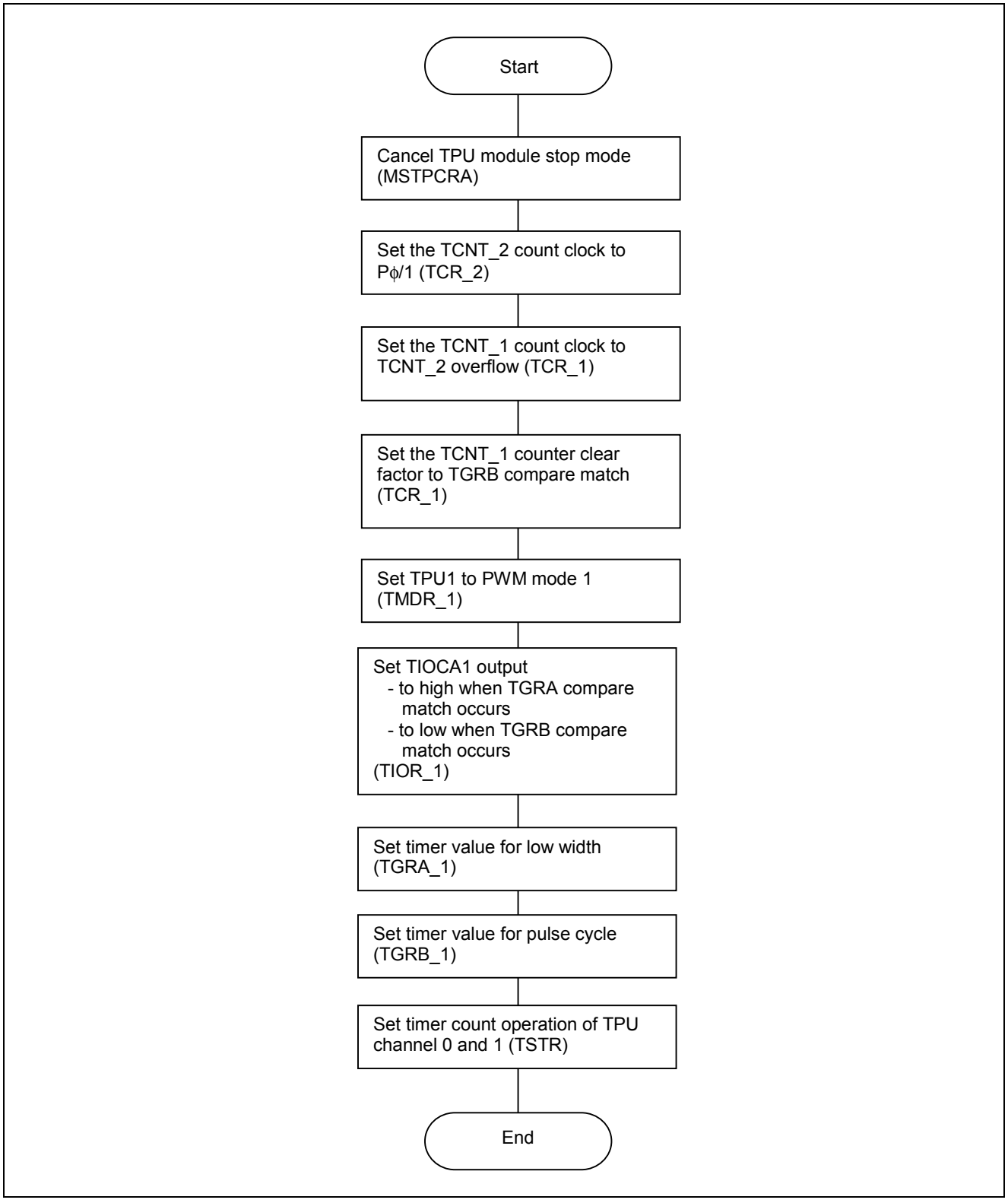
```
#define CYCLE_TIME  546                 // Pulse cycle:  546 msec
#define LOW_TIME    364                 // Low width:  364 msec
#define P_CLOCK      25                 // Pϕ (MHz)
                                                                    //
External function reference declaration
extern void  lpulse_set ( unsigned short, unsigned short * );
void  main( void )                      //  Main routine
{
unsigned long  low_count;               // Timer value for the low width
unsigned long  cyc_count;               // Timer value for the pulse cycle
   low_count = ((unsigned long)LOW_TIME    * P_CLOCK*1000)>>16;
   cyc_count = ((unsigned long)CYCLE_TIME* P_CLOCK*1000)>>16;
                     // Sets the pulse output.
   lpulse_set( (unsigned short)low_count, (unsigned short)cyc_count);

. .

}
```

3.3 Flowchart

The processing flow is shown below.



3.4 Program Listing

A listing of the source program is given below. In this source program, Renesas's standard definition (file automatically generated by High-performance Embedded Workshop: iodefine.h) that defines I/O register structure. To specify your own definition, change the I/O register structure in the sample program.

```
/************************************************************/
/* include file                                             */
/************************************************************/
#include <machine.h>
#include "iodefine.h"

/************************************************************/
/* function prototype                                       */
/************************************************************/
void pulse_set( unsigned short );

/************************************************************/
/* function definition                                      */
/************************************************************/
void  lpulse_set( unsigned short low_count,
                  unsigned short cyc_count )
{
    P_MSTPCRA.BIT.MSTPA0 = 0;    // reset module-standby for TPU
    P_TPU2.TCR.BIT.TPSC  = 0;    // set TPU2 countup clock source
    P_TPU1.TCR.BIT.TPSC  = 7;    // set TPU1 countup clock source
    P_TPU1.TCR.BIT.CCLR  = 2;    // set TPU1 counter clear cause
    P_TPU1.TMDR.BIT.MD   = 2;    // set TPU1 PWM-mode-1
    P_TPU1.TIOR.BIT.IOB  = 5;    // set TPU1 compare-match-B
    P_TPU1.TIOR.BIT.IOA  = 2;    // set TPU1 compare-match-A
                                 // set TPU1 compare value
    P_TPU1.TGRB          = (unsigned int)cyc_count;
    P_TPU1.TGRA          = (unsigned int)low_count;
    P_TPU.TSTR.BIT.CST1  = 1;    // start TPU1
    P_TPU.TSTR.BIT.CST2  = 1;    // start TPU2
}
```

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sept.19.03	—	First edition issued

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