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April 1st, 2010
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H8/38602R Group

IRQ Pin Settings

Introduction

This application note describes how to set the IRQ pin functions ($\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$). The P92/SSO (/$\overline{\text{IRQ0}}$) pin is selected for the $\overline{\text{IRQ0}}$ pin function, and the P11/AEVL/FTCI (/$\overline{\text{IRQ1}}$) pin is selected for the $\overline{\text{IRQ1}}$ pin function. IRQ0 interrupt processing toggles the LED connected to P82 on and off. IRQ1 interrupt processing toggles the LED connected to P83 on and off.

Target Device

H8/38602R

Contents

1. Specifications

- The IRQ pin functions ($\overline{IRQ0}$ and $\overline{IRQ1}$) are set.
- The $\overline{IRQ0}$ pin function is assigned to the PB0/AN0/$\overline{IRQ0}$ pin, P92/SSO (/$\overline{IRQ0}$) pin, and P30/SCK3/VCref (/$\overline{IRQ0}$) pin. The $\overline{IRQ1}$ pin function is assigned to the PB1/AN1/$\overline{IRQ1}$ pin, P11/AEVL/FTCI (/$\overline{IRQ1}$) pin, and P93/SSI (/$\overline{IRQ1}$) pin.
- The P92/SSO (/$\overline{IRQ0}$) pin is selected for the $\overline{IRQ0}$ pin function, and the P11/AEVL/FTCI (/$\overline{IRQ1}$) pin is selected for the $\overline{IRQ1}$ pin function.
- IRQ0 interrupt processing toggles LED1 connected to P82 on and off, and IRQ1 interrupt processing toggles LED2 connected to P83 on and off.
- The input edge sensing of both the $\overline{IRQ0}$ and $\overline{IRQ1}$ signals is falling edge.
- Output of the IRQ0 switch and the IRQ1 switch prevents jitter that occurs when a switch is pressed through the D-type flip-flop, and is input to the $\overline{IRQ0}$ and $\overline{IRQ1}$ pins.
- Figure 1 shows a block diagram of setting of the IRQ pins.

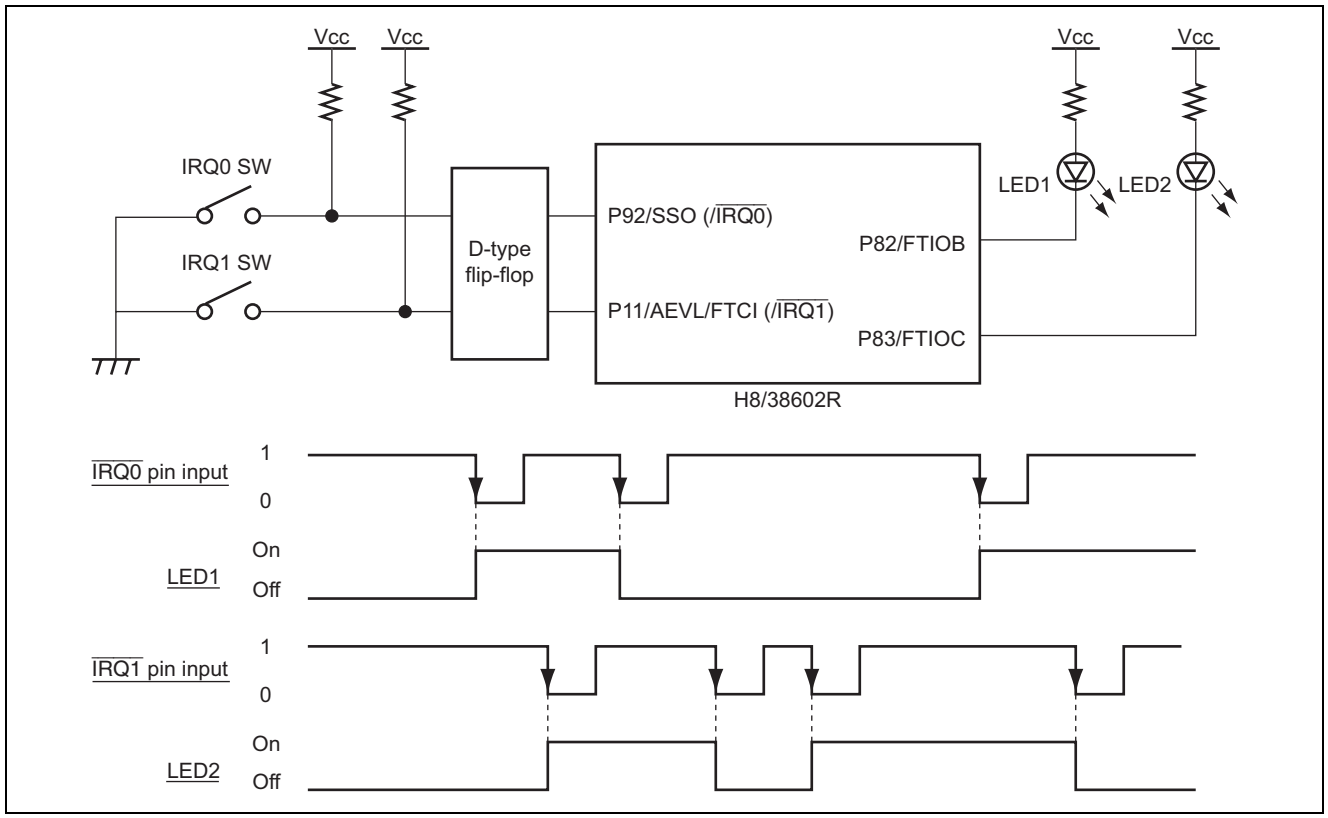


Figure 1 Setting of the IRQ Pins

2. Description of Functions Used

2.1 Functions Used

This sample task uses the IRQ interrupts for switch input to toggle the LEDs. The P92/SSO (/$\overline{\text{IRQ0}}$) pin is selected for the IRQ0 pin function, and the P11/AEVL/FTCI (/$\overline{\text{IRQ1}}$) pin is selected for the IRQ1 pin function. The LEDs are connected to the P82/FTIOB and P83/FTIOC pins, respectively. The following is a functional explanation.

(1) Exception handling: External interrupt function

Four external interrupts are provided: NMI, IRQAEC, IRQ1, and IRQ0.

Requests for IRQ1 and IRQ0 interrupts are made with an input signal to the $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ0}}$ pins. In addition, rising or falling edge sensing of the IRQ1 and IRQ0 interrupts can be specified with the IEG1 and IEG0 bits of the Interrupt Edge Select Register (IEGR). When the specified edge is input on the $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ0}}$ pins with the pin functions selected by the Port Function Control Register (PFCR) or Port Mode Register B (PMRB), the corresponding bit of the Interrupt Flag Register 1 (IRR1) is set to 1 and an interrupt request is issued.

Clearing the IEN1 and IEN0 bits of Interrupt Enable Register 1 (IENR1) to 0 disables accepting of an interrupt request. Setting the I bit of the Condition Code Register (CCR) to 1 masks all interrupts except an NMI interrupt.

- Interrupt Edge Select Register (IEGR)
  IEGR selects the edge direction that causes interrupt requests at the $\overline{\text{NMI}}$, $\overline{\text{ADTRG}}$, $\overline{\text{IRQ1}}$, and $\overline{\text{IRQ0}}$ pins to be issued.
- Interrupt Enable Register 1 (IENR1)
  IENR1 enables RTC, IRQAEC, IRQ1, and IRQ0 interrupt requests.
- Interrupt Flag Register 1 (IRR1)
  IRR1 is a status register for IRQAEC, IRQ1, and IRQ0 interrupt requests.
- Port Function Control Register (PFCR)
  PFCR changes the functions of the SSU pins and also assigns the $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ input pins to other ports.

Note on switching the functions of external interrupt pins:

If pin functions are switched by writing to PFCR and PMRB registers which control the external interrupt pins ($\overline{\text{IRQ1}}$ and $\overline{\text{IRQ0}}$), the interrupt request flag is set to 1 when the pin functions are switched even though a valid interrupt has not been input to the pins. Therefore, before using interrupts, clear the interrupt request flag to 0. Figure 2 shows the procedure for manipulating PFCR and PMRB registers and clearing the interrupt request flag.

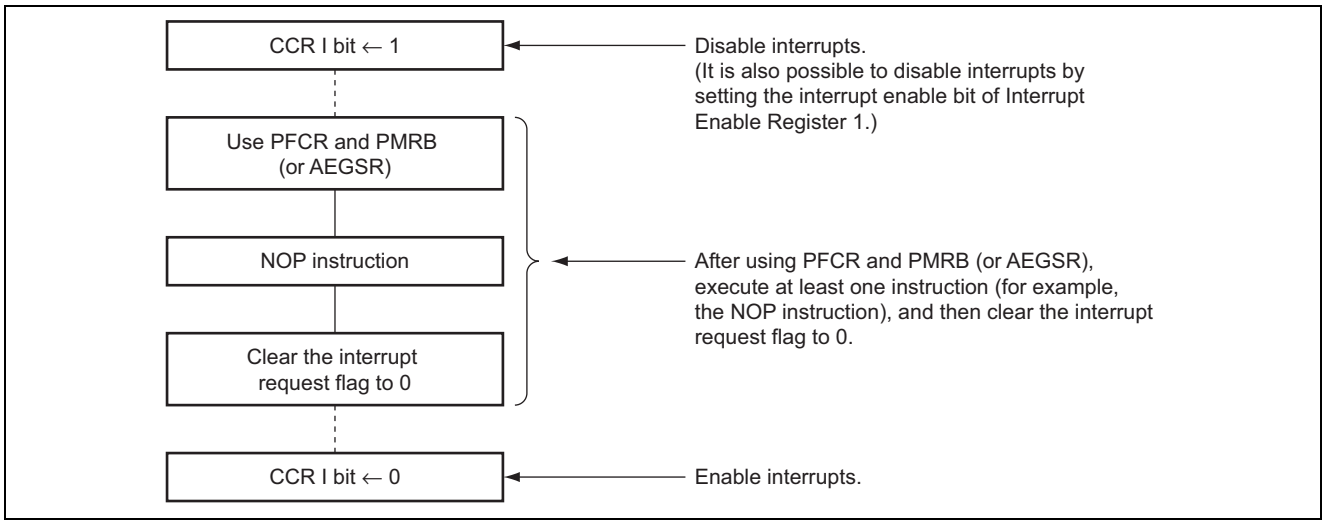


Figure 2 Procedure for Manipulating PFCR and PMRB (or AEGSR) and Clearing the Interrupt Request Flag

On switching pin functions, disable all interrupts before using the PFCR and PMRB (or AEGSR) registers. After these registers are used, at least one instruction (for example, the NOP instruction) must be executed, and then the interrupt request flag, which was set to 1, must be cleared to 0. If an instruction to clear the interrupt request flag to 0 is executed without an intervening instruction after PFCR and PMRB (or AEGSR) registers have been used, the interrupt request flag will not be cleared.

Another method that avoids setting of the interrupt request flag when pin functions are switched is controlling the signals to be at a high level.

(2) Watchdog timer function

The H8/38602R includes a watchdog timer that becomes active when a reset is canceled. The Timer Counter WD (TCWD) is incremented, and if it overflows, the H8/38602R is internally reset. Since this sample task does not use the watchdog timer function, this timer is stopped.

- Timer Control/Status Register WD1 (TCSRWD1)
  TCSRWD1 controls writing to TCSRWD1 and TCWD. TCSRWD1 also controls operation of the watchdog timer and indicates the operating status. TCSRWD1 must be rewritten by using the MOV instruction. Bit manipulation instructions cannot be used to change the setting.

(3) I/O port function

In this sample task, the LEDs are each connected to the P82/FTIOB and the P83/FTIOC pins of port 8 to control switching of the LED on and off. When the outputs of the P82 pin and P83 pin are high, the LEDs are turned off. When the outputs are low, the LED is turned on. The P82 and the P83 pins include an input pull-up MOS that can be controlled by a program. When the corresponding bit of the Port Pull-Up Control Register 8 (PUCR8) is set to 1 while the corresponding bit of the Port Control Register 8 (PCR8) is cleared to 0, the input pull-up MOS is turned on. At a reset, the input pull-up MOS is turned off. In this sample task, the input pull-up MOS of the P82 pin and the P83 pin is set to off.

- Port Data Register 8 (PDR8)
  PDR8 is a register for storing data of port 8.
- Port Control Register 8 (PCR8)
  PCR8 controls input/output of port 8 for each bit.
- Port Pull-Up Control Register 8 (PUCR8)
  PUCR8 controls the input pull-up MOS of port 8 for each bit.

2.2 Function Assignment

Function assignments in this sample task are listed in table 1. As shown in table 1, IRQ pin settings are performed by assigning functions to the functional elements.

Table 1 Assignment of Functions

Element	Description
IEGR	Sets the edge that issues an interrupt request on the $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ pins to the falling edge.
IENR1	Enables IRQ0 and IRQ1 interrupt requests.
IRR1	IRQ0 and IRQ1 interrupt request flags
PFCR	Assigns the $\overline{\text{IRQ0}}$ pin function to P92 and the $\overline{\text{IRQ1}}$ pin function to P11.
TCSRWD1	Stops the watchdog timer.
PDR8	Sets data to be output from P82 and P83.
PCR8	Sets the P82 and P83 pins as output pins.
PUCR8	Switches the input pull-up MOS of the P82 and P83 pins off.

3. Principles of Operation

This sample task uses the IRQ interrupts for switch input to toggle the LEDs. The P92/SSO (/$\overline{\text{IRQ0}}$) pin is selected for the IRQ0 pin function, and the P11/AEVL/FTCI (/$\overline{\text{IRQ1}}$) pin is selected for the IRQ1 pin function. The LEDs are connected to the P82/FTIOB and the P83/FTIOC pins. Figure 3 illustrates setting of the IRQ pins.

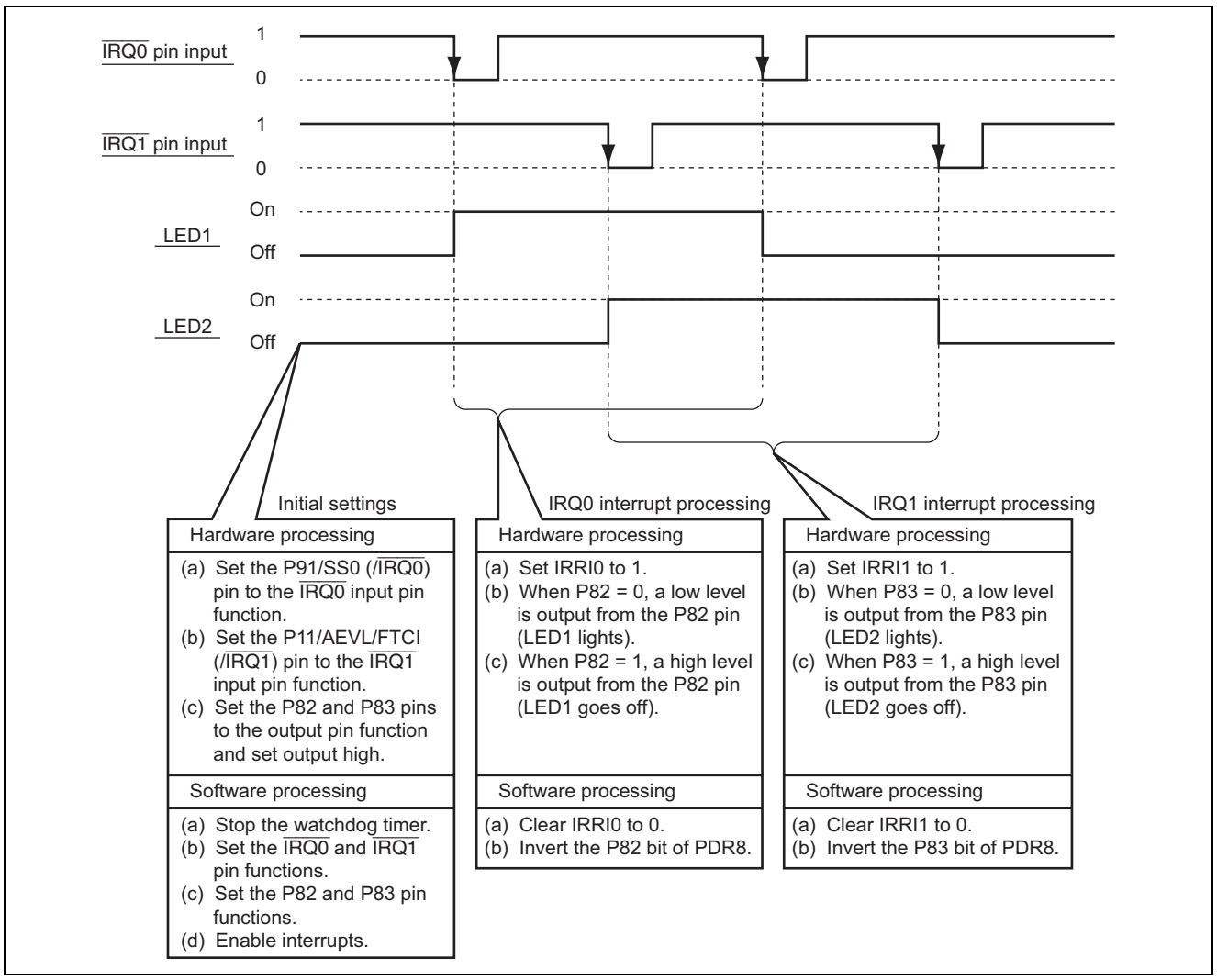


Figure 3 Principles of Operation

4. Description of Software

4.1 Description of Modules

The modules of this sample task is described in table 2.

Table 2 Modules

Function Name	Description
main	Stops the watchdog timer, performs initial setting of the $\overline{\text{IRQ0}}$ and the $\overline{\text{IRQ1}}$ pins, sets the P82 and P83 output pins, and enables interrupts.
int_irq0	Performs IRQ0 interrupt processing and inverts the P82 pin output.
int_irq1	Performs IRQ1 interrupt processing and inverts the P83 pin output.

4.2 Description of Arguments

This sample task does not use arguments.

4.3 Internal Registers

The internal registers used in this sample task are described below.

- Interrupt Edge Select Register (IEGR) Address: H'FFF2

Bit	Bit Name	Setting Value	R/W	Function
1	IEG1	0	R/W	IRQ1 Edge Select 0: Detects the falling edge of the $\overline{\text{IRQ1}}$ pin input. 1: Detects the rising edge of the $\overline{\text{IRQ1}}$ pin input.
0	IEG0	0	R/W	IRQ0 Edge Select 0: Detects the falling edge of the $\overline{\text{IRQ0}}$ pin input. 1: Detects the rising edge of the $\overline{\text{IRQ0}}$ pin input.

- Interrupt Enable Register 1 (IENR1) Address: H'FFF3

Bit	Bit Name	Setting Value	R/W	Function
1	IEN1	1	R/W	IRQ1 Interrupt Enable When this bit is set to 1, IRQ1 interrupt requests are enabled.
0	IEN0	1	R/W	IRQ0 Interrupt Enable When this bit is set to 1, IRQ0 interrupt requests are enabled.

- Interrupt Flag Register 1 (IRR1) Address: H'FFF6

Bit	Bit Name	Setting Value	R/W	Function
1	IRRI1	0	R/(W)*	IRQ1 Interrupt Request Flag [Setting condition] When the $\overline{\text{IRQ1}}$ pin is set to interrupt input and the specified edge is detected. [Clearing condition] When 0 is written to this bit.
0	IRRI0	0	R/(W)*	IRQ0 Interrupt Request Flag [Setting condition] When the $\overline{\text{IRQ0}}$ pin is set to interrupt input and the specified edge is detected. [Clearing condition] When 0 is written to this bit.

Note: * Only 0 can be written to clear the flag.

- Port Function Control Register (PFCR) Address: H'F085

Bit	Bit Name	Setting Value	R/W	Function
3	IRQ1S1	1	R/W	IRQ1 Select 1, 0
2	IRQ1S0	0	R/W	00: $\overline{\text{IRQ1}}$ is input from PB1. 01: $\overline{\text{IRQ1}}$ is input from P93. 10: $\overline{\text{IRQ1}}$ is input from P11. 11: Setting prohibited.
1	IRQ0S1	0	R/W	IRQ0 Select 1, 0
0	IRQ0S0	1	R/W	00: $\overline{\text{IRQ0}}$ is input from PB0. 01: $\overline{\text{IRQ0}}$ is input from P92. 10: $\overline{\text{IRQ0}}$ is input from P30. 11: Setting prohibited.

- Timer Control/Status Register WD1 (TCSRWD1) Address: H'FFB1

Bit	Bit Name	Setting Value	R/W	Function
7	B6WI	1	R/W	Bit 6 Write Disable Writing to the TCWE bit is enabled only when 0 is written to the B6WI bit. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable Writing to the TCWD is enabled when the TCWE bit is set to 1. When writing to this bit, 0 must be written to the B6WI bit.
5	B4WI	1	R/W	Bit 4 Write Disable Writing to the TCSRWE bit is enabled only when 0 is written to the B4WI bit. The B4WI bit is always read as 1.
4	TCSRWE	0	R/W	Timer Control/Status Register WD1 Write Enable Writing to the WDON and WRST bits is enabled when the TCSRWE bit is set to 1. When writing to this bit, 0 must be written to the B4WI bit.
3	B2WI	1	R/W	Bit 2 Write Disable Writing to the WDON is enabled only when 0 is written to the B2WI bit. This bit is always read as 1.
2	WDON	0	R/W	Watchdog Timer On The TCWD starts counting up when the WDON bit is set to 1 and stops counting when the WDON bit is cleared to 0. [Clearing condition] • If 0 is written to both B2WI and WDON bits while the TCSRWE bit is 1. [Setting condition] • If 0 is written to the B2WI bit and 1 to the WDON bit while the TCSRWE bit is 1.
1	B0WI	1	R/W	Bit 0 Write Disable Writing to the WRST bit is enabled only when 0 is written to the B0WI bit. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Clearing condition] • Reset by the $\overline{\text{RES}}$ signal • If 0 is written to both the B0WI and WRST bits while the TCSRWE bit is 1. [Setting condition] • When the TCWD overflows and an internal reset signal is generated.

- Port Data Register 8 (PDR8) Address: H'FFDB

Bit	Bit Name	Setting Value	R/W	Function
3	P83	1	R/W	If port 8 is read when the corresponding bit of the PCR8 register is 1, the value of PDR8 is read. The pin state therefore has no effect on reading. If port 8 is read when PCR8 is 0, the pin state is read.
2	P82	1	R/W	

- Port Control Register 8 (PCR8) Address: H'FFEB

Bit	Bit Name	Setting Value	R/W	Function
3	PCR83	1	W	Setting a PCR8 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR8 and PDR8 registers are valid when the corresponding pin is set as a general I/O pin. This register is a write-only register. If read, an undefined value will be read from each bit.
2	PCR82	1	W	

- Port Pull-Up Control Register 8 (PUCR8) Address: H'F086

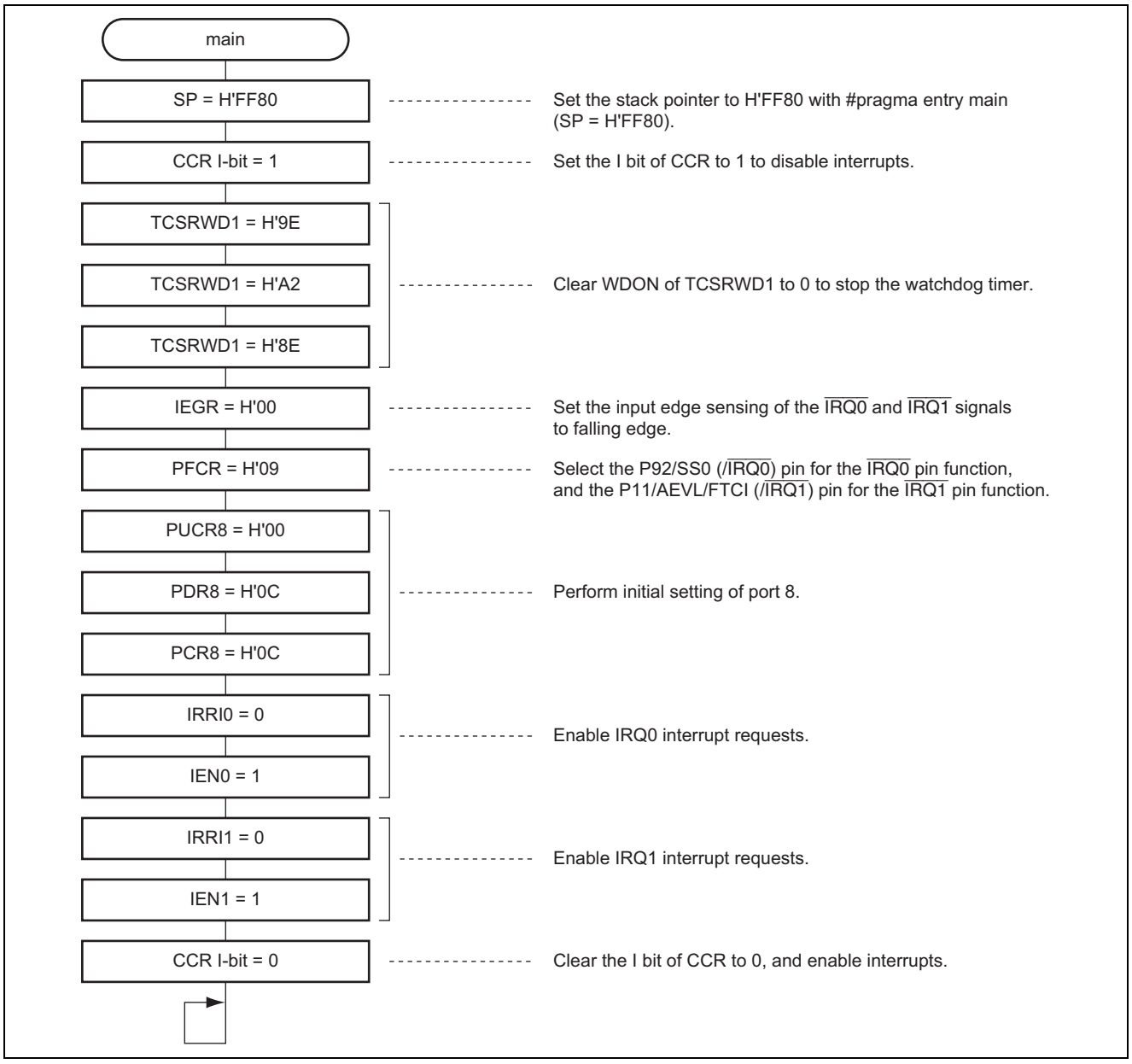
Bit	Bit Name	Setting Value	R/W	Function
3	PUCR83	0	R/W	With a PCR8 bit cleared to 0, setting the corresponding PUCR8 bit to 1 turns on the input pull-up MOS for the corresponding pin, while clearing the bit to 0 turns off the pull-up MOS.
2	PUCR82	0	R/W	

4.4 RAM Usage

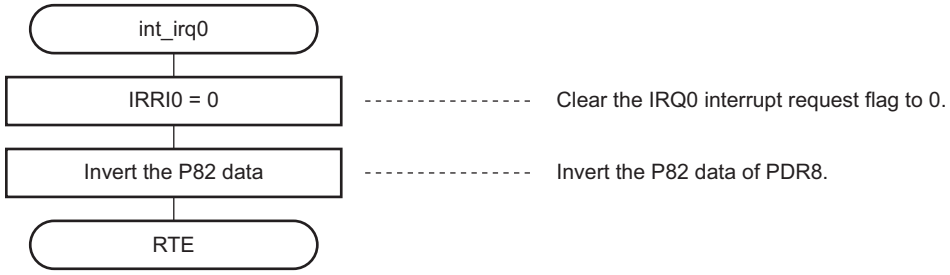
This sample task does not use internal RAM.

5. Flowcharts

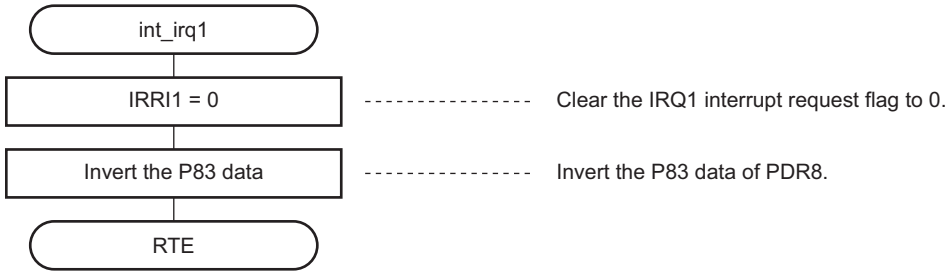
5.1 main



5.2 int_irq0



5.3 int_irq1



5.4 Link Address Specification

Section Name	Address
CVECT	H'0000
P	H'0100

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Sep.13.05	—	First edition issued

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