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Renesas Electronics Corporation

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H8/300H Tiny Series

Interrupt-Period Setup Using Auto-Reload Timer Function

Introduction

Generate a Timer B1 interrupt every 160 µs using the auto reload timer function of Timer B1.

Target Device

H8/300H Tiny Series H8/3687

Contents

1. Specification

1. Generate a Timer B1 interrupt every 160 µs using the auto reload timer function of Timer B1.
2. Timer B1 interrupt events are counted during the interrupt sequence, and each time a count of 250 is reached the LED is either illuminated or extinguished.

2. Description of Functions Used

1. In this task example, a Timer B1 interrupt can be generated every 160 µs by using the auto reload timer function of Timer B1.
   A. Figure 1 shows the block diagram of the Timer B1 auto reload function which is described as follows:
      - The system clock (ϕ) is a 10 MHz and is used as the reference clock that drives the CPU and peripheral functions.
      - Prescaler S (PSS) is a 13-bit counter to which the system clock ϕ is applied and is incremented by one on each clock cycle.
      - Timer Mode Register B1 (TMB1) is an 8-bit read/write register used to select the auto reload function and select the input clock.
      - Timer Counter B1 (TCB1) is an 8-bit readable up counter that is incremented by means of the applied internal clock and/or external events. The applied input clock can be selected from a total of eight types of clock derived from the system clock divided by 8192, 2048, 512, 256, 64, 16 and 4, and by an external clock. In this task example, a clock, derived by dividing the system clock by 64, is selected as the input clock applied to TCB1.
      - Timer Control Register B1 (TLB1) is an 8-bit write-only register used to set the reload value for TCB1. In this task example, setting TLB1 to H'E7 ensures that TCB1 will overflow in 160 µs.
      - Timer B1 Interrupt Request Flag (IRRTB1) is set to 1 by a TCB1 overflow event. If, provided that IRRTB1 has been set to 1, Timer B1 Interrupt Enable (IENTB1) of the Interrupt Enable Register (IENR1) is set to 1, and the I bit of the Condition Code register (CCR) is cleared to 0, the Timer B1 interrupt sequence will start on reception of the Timer B1 interrupt.

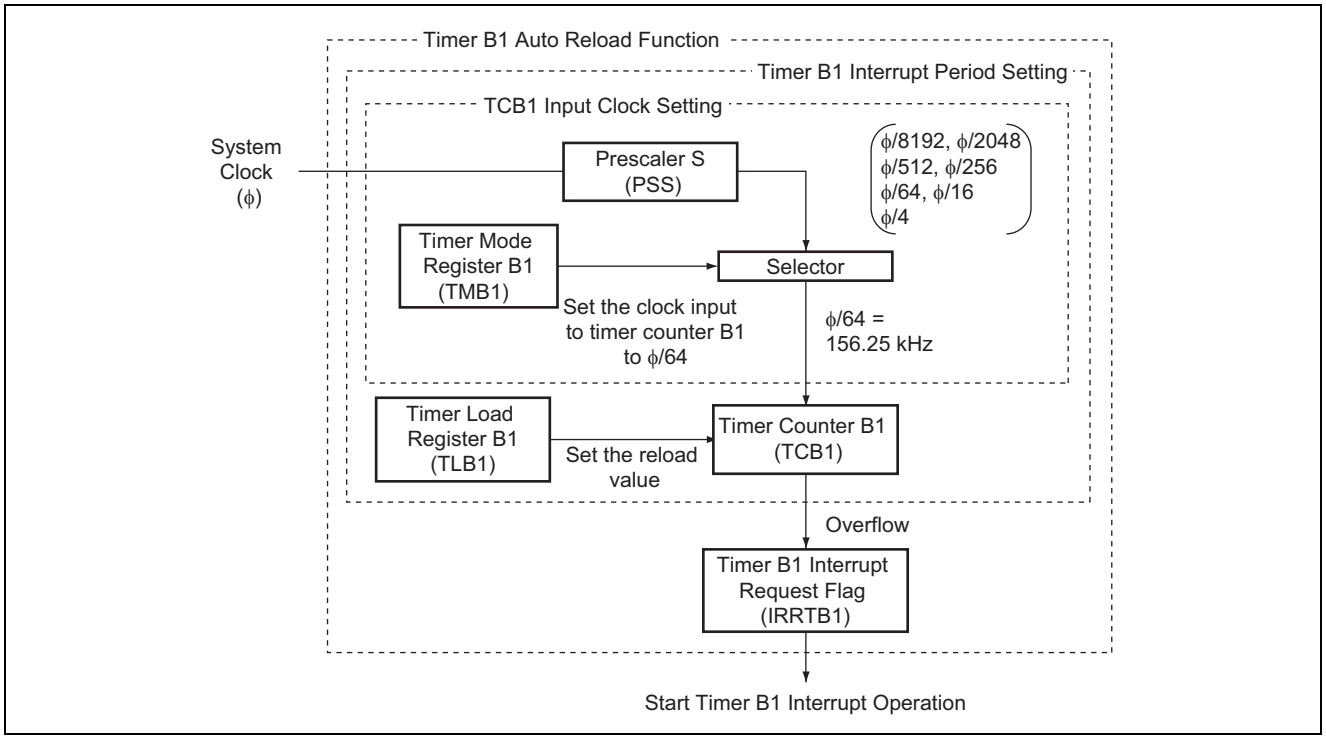


Figure 1 Timer B1 Auto Reload Function Block Diagram

B. The following is brief description of how to set the interrupt period using the Timer B1 auto reload function.
   - The interrupt period using the Timer B1 auto-reload function is set by the following expression:

     Timer B1 Interrupt Period (s) = (TCB1 input clock period (s)) × (256 – (reload setting value))

   - The Timer B1 interrupt period is set by respectively setting the TCB1 input clock period, as defined by the aforementioned expression, in TMB1 and the reload setting value in TLB1.

2. Table 1 lists the function assignments applicable to this task example. The interrupt period is set using the Timer B1 auto reload function.

Table 1 Function Assignment

Function	Function Assignment
PSS	This is a 13-bit counter to which the system clock is applied
TCB1	This is an 8-bit counter to which the system clock divided by 64 is input
TMB1	This register sets the clock input to timer counter B1 to ϕ/64
TLB1	This sets the reload value for TCB1
IRRTB1	This flag reflects the presence of the Timer B1 interrupt request
PCR7	This sets the P73 output pin function
PDR7	This stores the P73 output pin data
P73	This is the LED output

3. Operational Description

Figure 2 shows the principle of operation by way of waveform diagrams. As shown in figure 2, setting the interrupt period by means of the Timer B1 auto reload function is facilitated by both hardware and software.

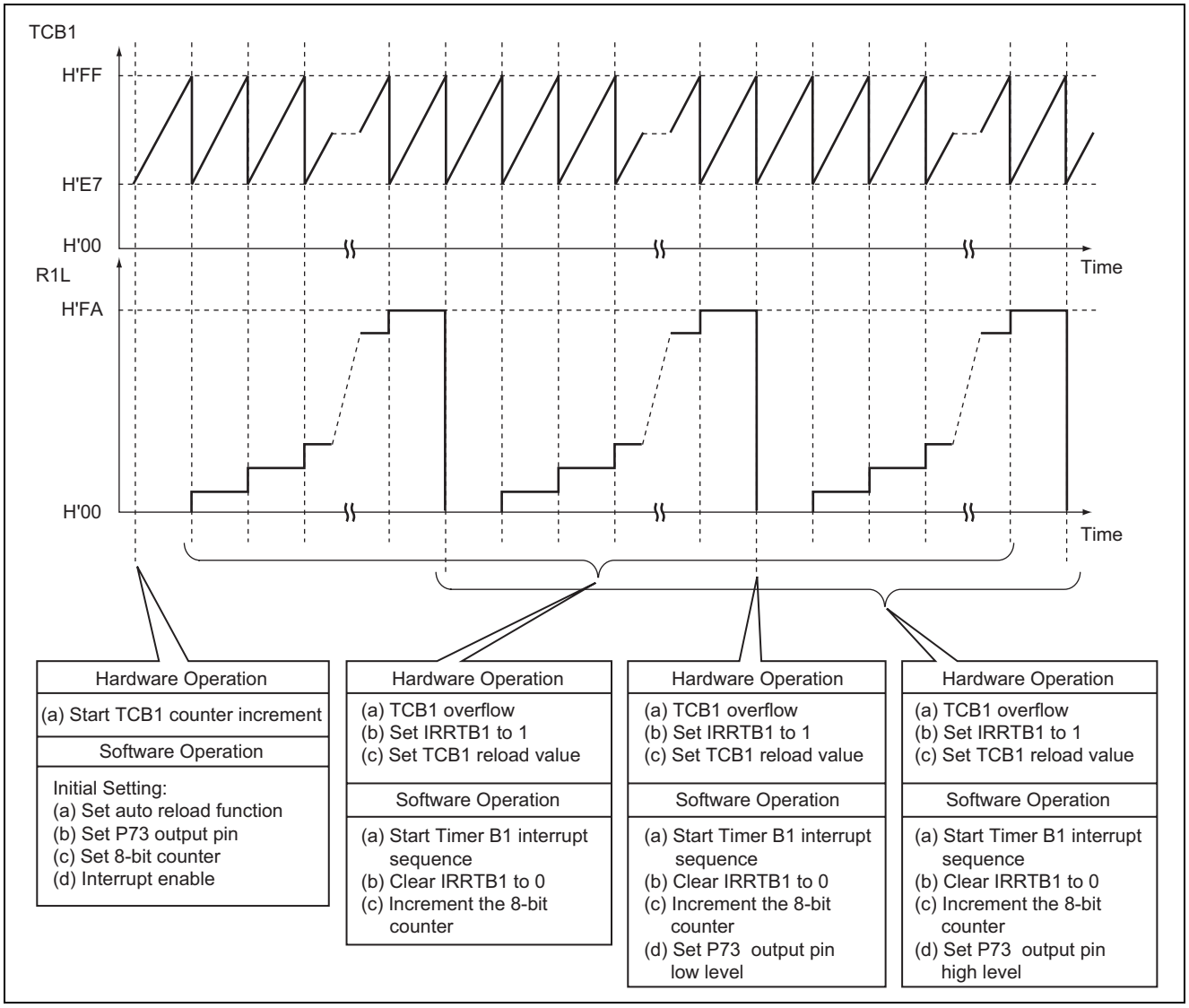


Figure 2 Operating Principle of Interrupt Period Setup by the Timer B1 Auto Reload Function

4. Software Description

4.1 Module Description

The modules applicable to this task example are listed in table 2.

Table 2 Module Description

Module Name	Label Name	Function
Main Routine	main	Initializes the stack pointer, sets the auto-reload function, facilitates port 73 setup, sets the 8-bit counter, enables the interrupts, and controls on/off illumination of the LED.
Count Up	TB1INT	Increments the 8-bit counter and sets CTEDF to 1 when the 8-bit counter counts up to H'FA.

4.2 Argument Description

There are no arguments used in this task example.

4.3 Description of Applicable Internal Registers

Table 3 lists the internal registers used in this task example.

Table 3 Description of Applicable Internal Registers

Register Name		Functional Description	Address	Setting
IRR2	IRRTB1	Interrupt Request Register 1 (Timer B1 Interrupt Request Flag): When IRRTB1 is 0, a Timer B1 interrupt is not requested When IRRTB1 is 1, a Timer B1 interrupt is requested	H'FFF7 Bit 5	0
IENR2	IENTB1	Interrupt Enable Register 1 (Timer B1 Interrupt Enable): When IENTB1 is 1, the Timer B1 interrupt is enabled	H'FFF5 Bit 5	1
TMB1		Timer Mode Register B1: When TMB1 is H'FC, the Timer B1 function is set as the auto reload function and the clock, derived from the system clock divided by 64, is set as the TCB1 input clock	H'FFB2	H'FC
TCB1		Timer Counter B1: This is an 8-bit up counter to which the input clock, derived from the system clock divided by 64, is applied	H'FFB3	H'00
TLB1		Timer Load Register B1: When TLB1 is H'E7, TCB1 starts to count from H'E7, and when the register overflows, TCB1 is reloaded with the value H'E7	H'FFB3	H'E7
PDR7	P73	Port Data Register 7 (Port Data Register 73): When P73 is set to 0, the output level of pin P73 is low When P73 is set to 1, the output level of pin P73 is high	H'FFDA Bit 3	0
PCR7	PCR73	Port Control Register 7 (Port control Register 73): When PCR73 is set to 1, pin P73 is set as an output pin.	H'FFEA Bit 3	1

4.4 Description of RAM Used

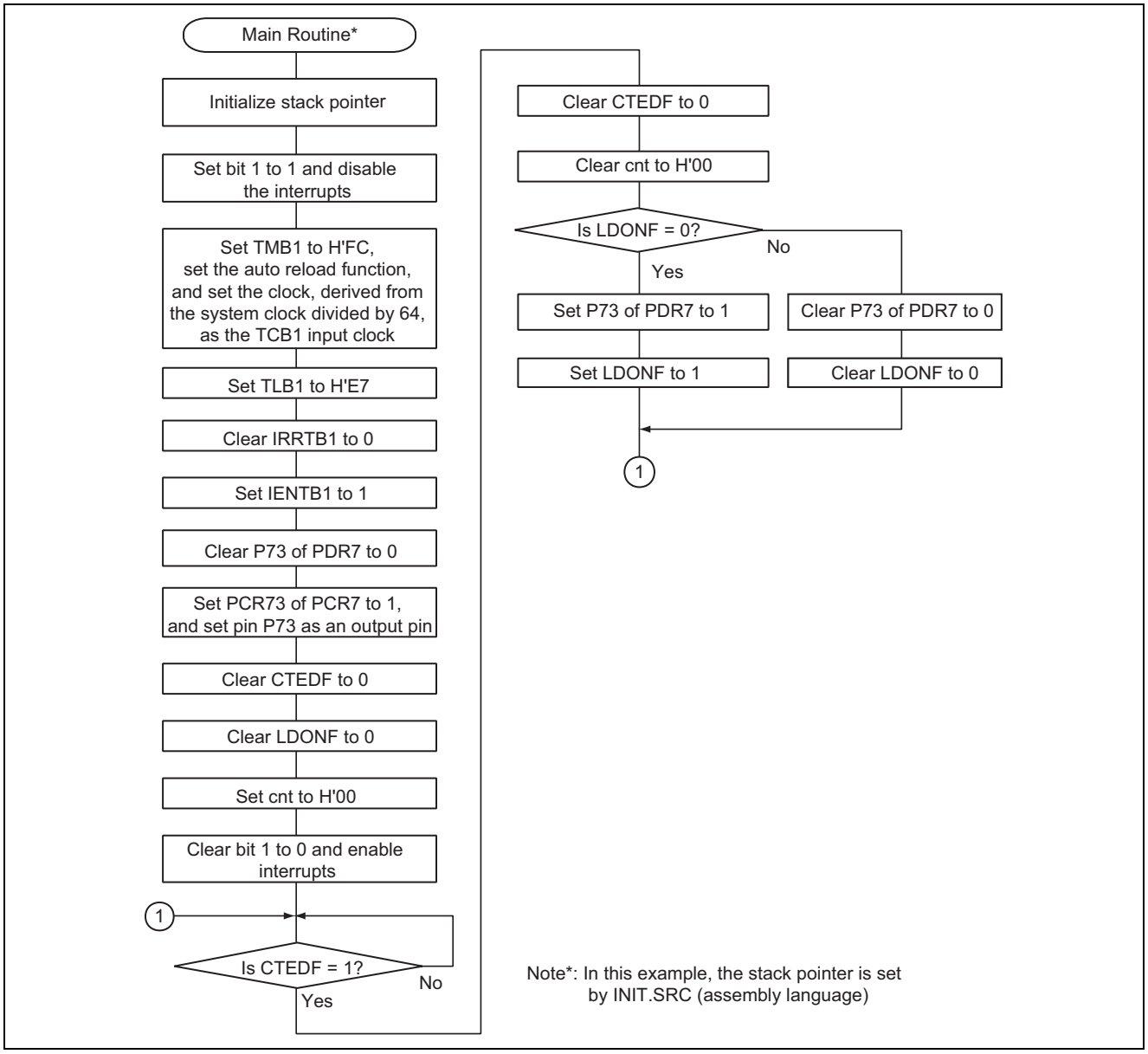
Table 4 lists and describes the RAM used in this task example.

Table 4 Description of Applicable RAM

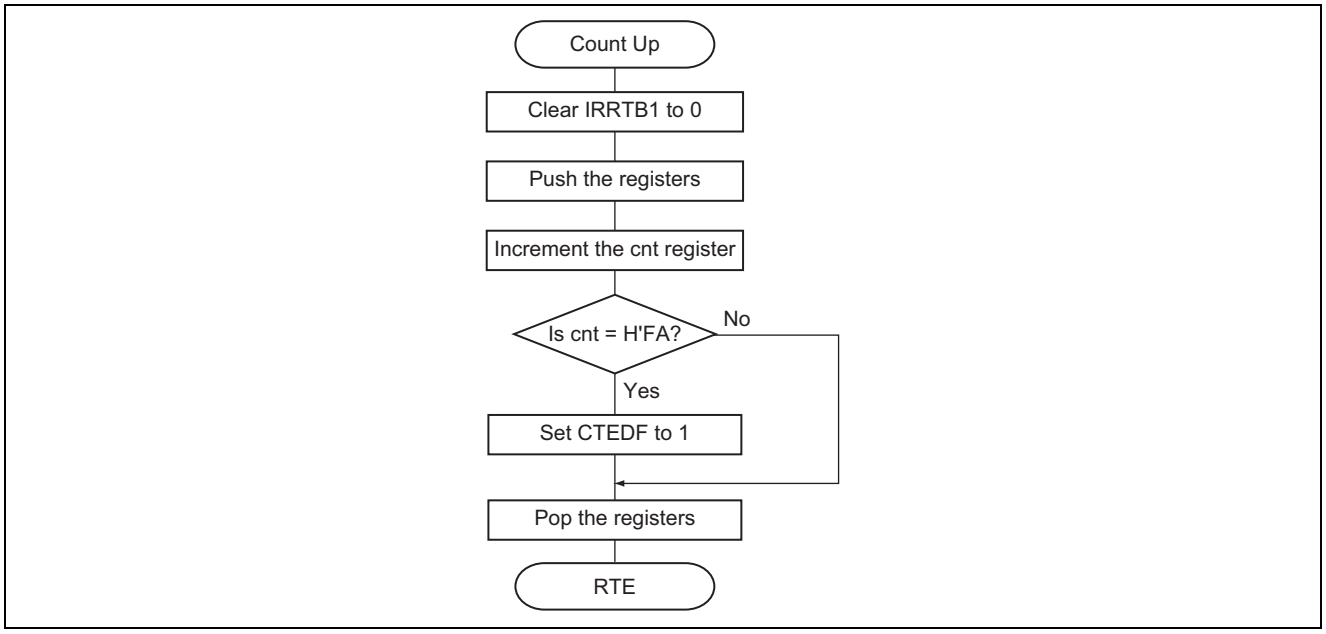
Label Name		Function	Address	Used in
USRF	CTEDF	Flag that determines whether the count value in the 8-bit counter is H'FA	H'FB80 Bit 0	Main routine Count up
	LDONF	Flag that determines the on/off status of the LED	H'FB80 Bit 1	Main routine
cnt		An 8-bit counter	H'FB81	Count up

5. Flowcharts

1. Main Routine



2. Timer B1 Interrupt Service Routine



5.1 Link Address Designation

Section Name	Address
CV1	H'0000
P	H'0100
V	H'FB80

6. Program Listing

INIT.SRC (Program List)

```
    .EXPORT   _INIT
    .IMPORT   _main
;
    .SECTION  P,CODE
_INIT:
    MOV.W     #H'FF80,R7
    LDC.B     #B'10000000,CCR
    JMP       @_main
;
    .END
```

```
/************************************************************/
/*                                                          */
/*  H8/300HN Series -H8/3687-                               */
/*  Application Note                                        */
/*                                                          */
/*'Interrupt Period Setting by Auto Reload Timer Function'*/
/*                                                          */
/*  Function                                                */
/*  :Timer B1 Auto Reload                                   */
/*                                                          */
/*  External Clock : 10MHz                                  */
/*  Internal Clock : 10MHz                                  */
/*  Sub Clock      : 32.768kHz                              */
/*                                                          */
/************************************************************/

#include <C:\ch38\include\machine.h>

/************************************************************/
/*  Symbol Defnition                                        */
/************************************************************/

struct BIT {
    unsigned char    b7:1;     /* bit7 */
    unsigned char    b6:1;     /* bit6 */
    unsigned char    b5:1;     /* bit5 */
    unsigned char    b4:1;     /* bit4 */
    unsigned char    b3:1;     /* bit3 */
    unsigned char    b2:1;     /* bit2 */
    unsigned char    b1:1;     /* bit1 */
    unsigned char    b0:1;     /* bit0 */
};
```

```
#define  TMB  *(volatile unsigned char *)0xF760          /* Timer Mode Register B1         */
#define  TCB1 *(volatile unsigned char *)0xF761          /* Timer Counter B1               */
#define  TLB1 *(volatile unsigned char *)0xF761          /* Timer Load Register            */

#define  IEGR1_BIT    (*(struct BIT *)0xFFF2)            /*Interrupt Edge Select Register 1*/
#define  IEG3 IEGR1_BIT.b3                               /* IRQ3 Edge Select               */
#define  IEG2 IEGR1_BIT.b2                               /* IRQ2 Edge Select               */
#define  IEG1 IEGR1_BIT.b1                               /* IRQ1 Edge Select               */
#define  IEG  IEGR1_BIT.b0                               /* IRQ0 Edge Select               */
#define  IENR1    *(volatile unsigned char *)0xFFF4      /* Interrupt Enable Register 1    */
#define  IENR1_BIT    (*(struct BIT *)0xFFF4             /* Interrupt Enable Register 1    */
#define  IEN3 IENR1_BIT.b3                               /* IRQ3 Interrupt Enable          */
#define  IEN2 IENR1_BIT.b2                               /* IRQ2 Interrupt Enable          */
#define  IEN1 IENR1_BIT.b1                               /* IRQ1 Interrupt Enable          */
#define  IEN0 IENR1_BIT.b0                               /* IRQ0 Interrupt Enable          */
#define  IENR2    *(volatile unsigned char *)0xFFF5      /* Interrupt Enable Register 1    */
#define  IENR2_BIT    (*(struct BIT *)0xFFF5)            /* Interrupt Enable Register 1    */
#define  IENTB1   IENR2_BIT.b5                           /* IRQ3 Interrupt Enable          */
#define  IRR1 *(volatile unsigned char *)0xFFF6          /* Interrupt Flag Register 1      */
#define  IRR1_BIT (*(struct BIT *)0xFFF6)                /* Interrupt Flag Register 1      */
#define  IRRI3    IRR1_BIT.b3                            /* IRQ3 Interrupt Request Flag    */
#define  IRRI2    IRR1_BIT.b2                            /* IRQ2 Interrupt Request Flag    */
#define  IRRI1    IRR1_BIT.b1                            /* IRQ1 Interrupt Request Flag    */
#define  IRRI0    IRR1_BIT.b0                            /* IRQ0 Interrupt Request Flag    */
#define  IRR2 *(volatile unsigned char *)0xFFF7          /* Interrupt Flag Register 2      */
#define  IRR2_BIT (*(struct BIT *)0xFFF7)                /* Interrupt Flag Register 2      */
#define  IRRTB1   IRR2_BIT.b5                            /* TMB1 Interrupt Request Flag    */
#define  PDR7 *(volatile unsigned char *)0xFFDA          /* Port7 Data Register            */
#define  PDR7_BIT (*(struct BIT *)0xFFDA)                /* Port7 Data Register            */
#define  P7B3 PDR7_BIT.b3                                /* Port Data Register 73          */
#define  PCR7_BIT (*(struct BIT *)0xFFDA)                /* Port7 Control Register         */
#define  PCR73    PDR7_BIT.b3                            /* Port73 Control Register        */

#pragma  interrupt    (TB1INT)
```

```
/*********************************************************/
/*  Function Definitions                                 */
/*********************************************************/
extern   void INIT ( void );                              /* SP Set                       */
void     main     ( void );
void     TB1INT   ( void );

/*********************************************************/
/*  RAM define                                           */
/*********************************************************/
unsigned char    USRF;                                    /* User Flag Erea               */
unsigned char    USRF_1;                                  /* User Flag Erea               */
unsigned char    cnt;                                     /* Counter                      */

extern void _INITSCT();

/*********************************************************/
/*  Vector Address       */
/*********************************************************/
#pragma  section  V1                                      /* VECTOR SECTOIN SET           */
void     (*const VEC_TBL1[])(void) = {                    /* 0x00 - 0x0f                  */
    INIT                                                  /* 00 Reset                     */
};

#pragma  section  V2                                      /* VECTOR SECTOIN SET           */
void (*const VEC_TBL2[])(void) = {
    TB1INT                                                /* 29 Timer B1 Interrupt        */
};
#pragma  section                                          /* P                            */
```

```
/*********************************************************/
/*  Main Program                                         */
/*********************************************************/
void main ( void )
{
    _INITSCT();

    set_imask_ccr(1);                  /* Interrupt Disable                          */

    TMB1 = 0xFC;                       /* Initialize Timer B1 Function & Input Clock */
    TLB1 = 0xE7;                       /* Initialize TCB1 reload Value               */
    IRRTB1 = 0;                        /* Interrupt Flag Initialize                  */
    IENTB1 = 1;                        /* Interrupt Enable Flag Set                  */

    P7B3 = 0;
    PCR73 = 1;                         /* Initialize P73 Output Terminal Function    */

    USRF = 0x00;                       /* Initialize User Flag Erea                  */
    USRF_1 = 0x00;                     /* Initialize User Flag Erea                  */
    cnt = 0x00;                        /* Initialize 8 bit counter                   */

    set_imask_ccr(0);                  /* Interrupt Enable                           */

    while(1)
    {

        while(USRF == 0x01)            /* CTEDF = "1"?                               */
        {
              USRF = 0x00;             /* Clear CTEDF                                */

              cnt = 0x00;              /* Initialize 8 bit counter                   */

        if (USRF_1 == 0x00)            /* LDONF = "1"?                               */
        {
               P7B3 = 1;               /* Turn on LED                                */
               USRF_1 = 0x01;          /* Set LDONF                                  */
           }
          else
           {
               P7B3 = 0;               /* Turn off LED                               */
               USRF_1 = 0x00;          /* Clear LDONF                                */
           }
       }
    }
}
```

```
/*********************************************************/
/*  TimerB1 Interrupt                                    */
/*********************************************************/
void TB1INT( void )
{
    IRRTB1 = 0;                         /* Clear IRRTB1                              */
    cnt = cnt+1;                        /* Increment 8 bit Counter                   */

    if(cnt == 0xFA)                     /* 8 bit Counter = H'FA                      */
     {
      USRF = 0x01;                      /* Set CTEDF                                 */
     }
}
```

Revision Record

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Feb.26.03	—	First edition issued
2.00	Jul.22.05	—	Second edition issued

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