R32C/100 Series

Intelligent I/O SR Waveform Output Mode

REJ05B1227-0100
Rev.1.00
May 06, 2010

# 1. Abstract

This document describes the set/reset (SR) waveform output of a variable period and duty using the waveform generation function of intelligent I/O groups 0 to 2.

# 2. Introduction

The application example described in this document applies to the following microcomputer (MCU):
Microcomputer: R32C/118 Group

This program can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the R32C/118 Group. Check the hardware manual for any additions or modifications to functions. Careful evaluation is recommended before using this application note.

# 3. Overview

The intelligent I/O consists of three groups, each with one free-running 16-bit base timer and eight 16-bit registers for time measurement or waveform generation. Table 3.1 lists the Intelligent I/O Functions and Channels.

**Table 3.1 Intelligent I/O Functions and Channels**

| Function | Group 0 | Group 1 | Group 2 |
|---|---|---|---|
| Base timer | One channel | One channel | One channel |
| Time management | Eight channels | Eight channels | Not available |
| Waveform generation | Eight channels | Eight channels | Eight channels |

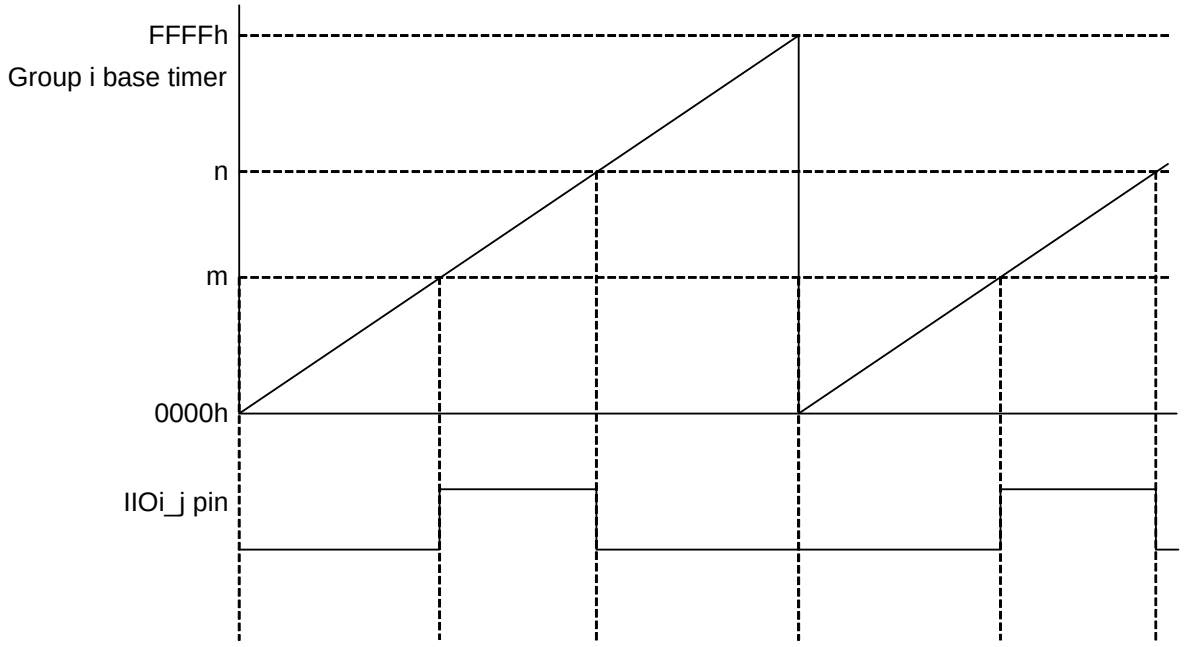
The waveform generation function of the intelligent I/O has four operating modes and two selectable functions, as listed in Table 3.2.

**Table 3.2 Intelligent I/O Waveform Generation Specifications**

| Function | | Group 0 | Group 1 | Group 2 |
|---|---|---|---|---|
| Operating modes | Single-phase waveform output mode | Eight channels | Eight channels | Eight channels |
| | Inverted waveform output mode | Eight channels | Eight channels | Eight channels |
| | SR waveform output mode | Eight channels | Eight channels | Eight channels |
| | Bit modulation PWM mode | Not available | Not available | Eight channels |
| Selectable functions | RTP mode | Not available | Not available | Eight channels |
| | Parallel RTP mode | Not available | Not available | Eight channels |

In the SR waveform mode described in this document, when the values for the group i base timer (GiBT) and the waveform generation register (GiPOj) for channel j match, the output level at the corresponding pin (IIOi_j) becomes high, and when the base timer (GiBT) and channel k match or the base timer reaches 0000h, the output level at the corresponding pin (IIOi_j) becomes low (i = 0 to 2; j = 0, 2, 4, 6; k = 1, 3, 5, 7). Figure 3.1 shows an example of SR waveform output mode operation.

The SR waveform output mode always uses channels in pairs, i.e. channels 0 and 1, channels 2 and 3, channels 4 and 5, and channels 6 and 7.
Note that in the waveform generation function for the intelligent I/O, the default output value and inverted output can be selected for each channel.




i = 0 to 2
j = 0, 2, 4, 6
m: GiPOj register value
n: GiPOj + 1 register value

Note:
1. Waveform when the INV bit in the GiPOCRj register is set to 0 (do not invert the output level) and the IVL bit is set to 0 (output low as default value).

**Figure 3.1 Operation Example in SR Waveform Output Mode**

# 4. Application Example

## 4.1 Description

In this application note, the SR waveform output cycle is enabled on channel 0, and the timing at which the output level becomes high and low are set on channel j and channel k, respectively (j = 2, 4, 6; k = 3, 5, 7). Also, an SR waveform is output from the IIOi_j pin corresponding to channel j for group i (i = 0 to 2).
Figure 4.1 shows the SR waveform output.

In the SR waveform output mode, PWM and duty cycles can be varied, and the duty cycle start position (set width) and end position (reset width) can be set freely.

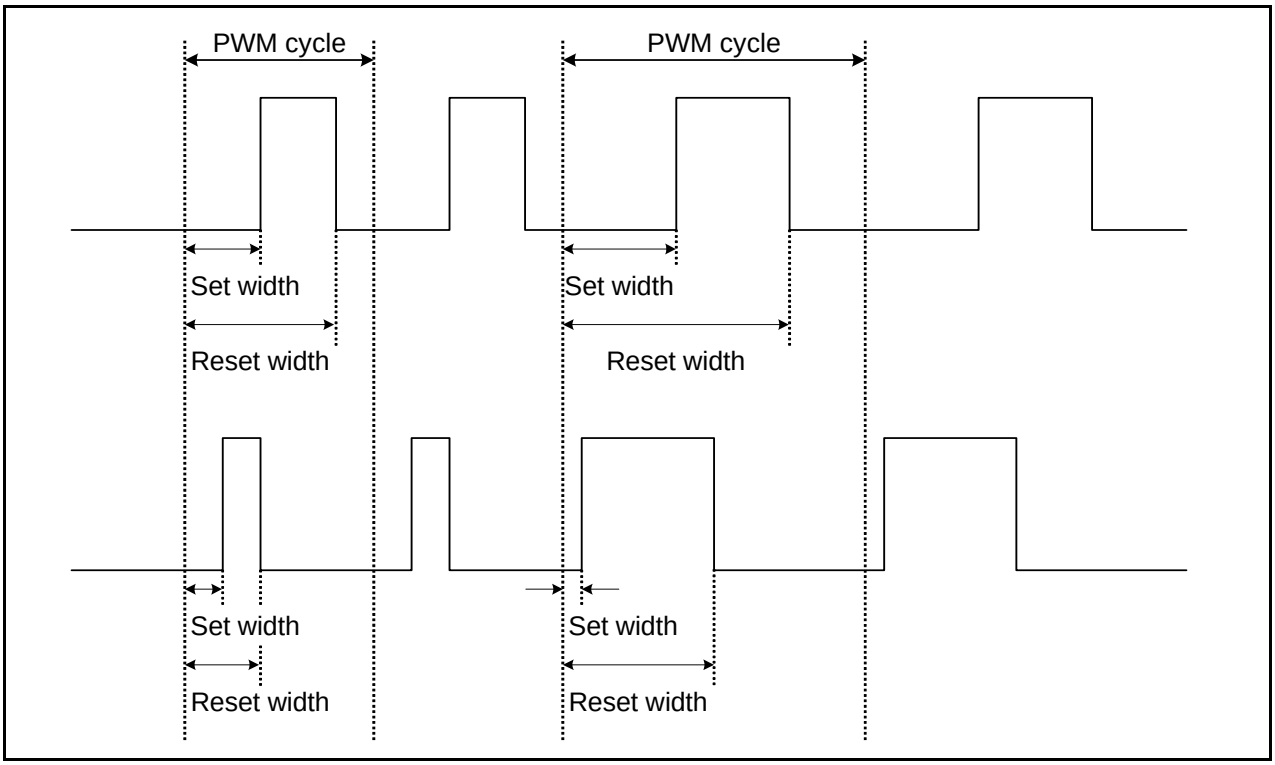



**Figure 4.1 SR Waveform Output Example**

(1) Setting the PWM cycle

Channel 0 is used in the single-phase waveform output mode of the waveform generation function. The base timer is reset by a match between the GiPO0 register and the base timer value (i = 0 to 2). When the setting value in the GiPO0 register is n, the PWM cycle is as follows.

$$\frac{n+2}{fBTi}$$ where fBTi is base timer operating clock

(2) Setting the set and the reset width

Channel j is used in the SR waveform output mode of the waveform generation function. When the setting value of registers GiPOj and GiPOk are m and n, respectively, the set and the reset width are as follows (j = 0, 2, 4, 6; k = j + 1).

Set width: $\frac{m}{fBTi}$ Reset width: $\frac{n}{fBTi}$

(3) Changing the PWM cycle and the set and reset widths

The PWM cycle and the set and reset widths are changed using a channel 0 waveform generation interrupt by rewriting registers GiPO0, GiPOj and GiPOk in the interrupt handler.

## 4.2 Setting Outline

An outline flowchart of intelligent I/O settings for SR waveform output is shown in the Figure 4.2.

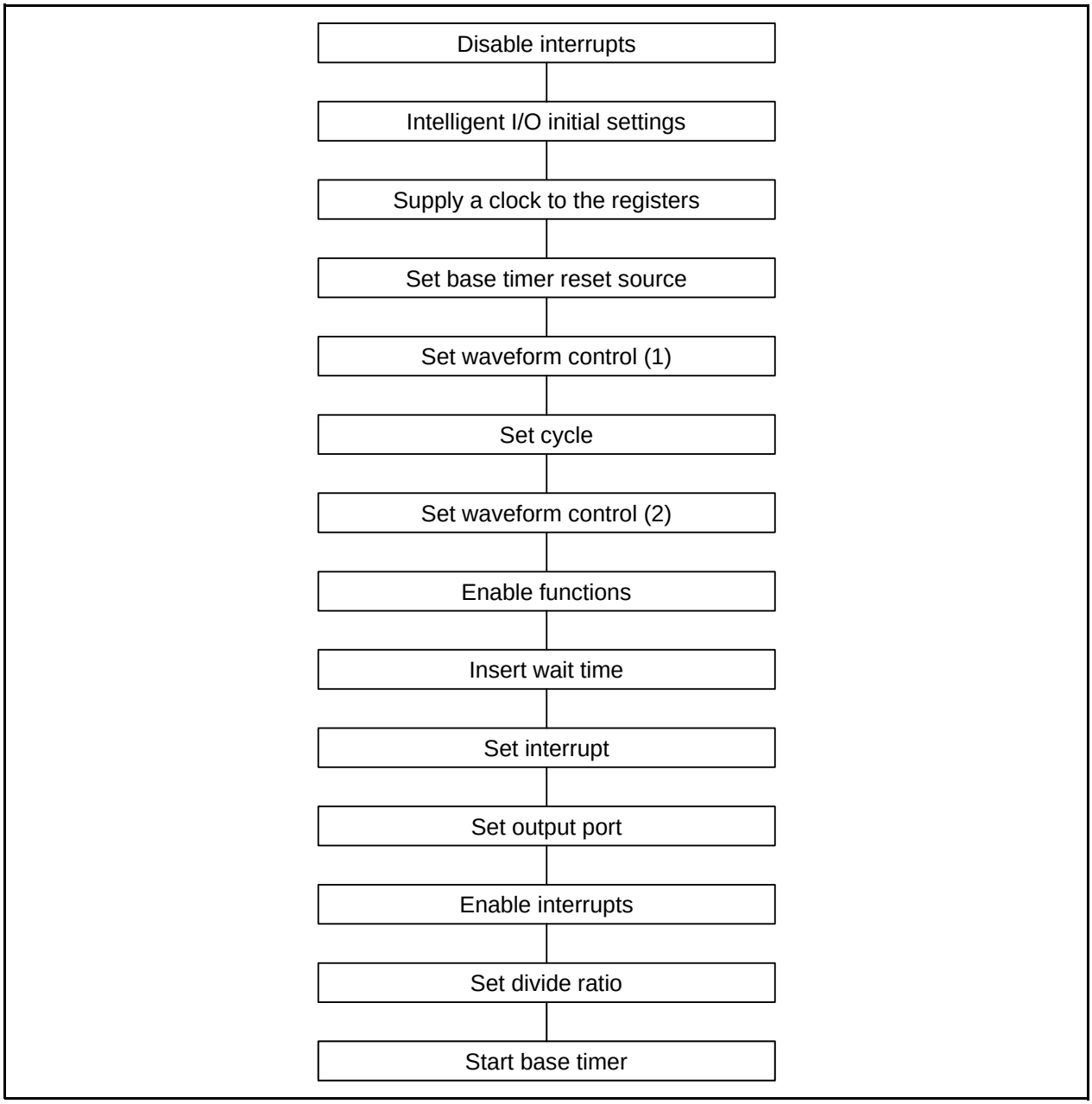


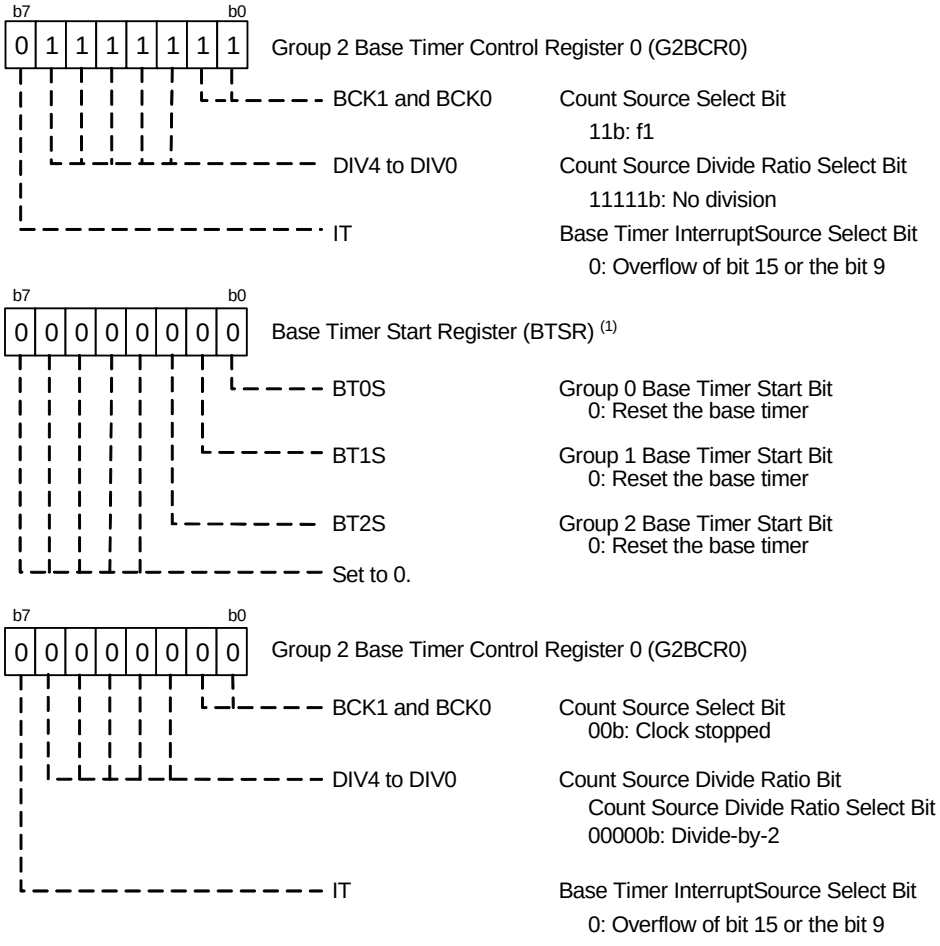

**Figure 4.2 Outline of Intelligent I/O Settings (SR Waveform Output)**

## 4.3 Detailed Settings

Disable interrupts.

Set the I flag to 0, or set bits ILVL2 to ILVL0 in the IIOkIC register that have been assigned the interrupt requests from the intelligent I/O, to 000b (k = 0 to 11).

Intelligent I/O initial settings




Note:

1. The initial settings of bits and registers for the intelligent I/O are required as follows:
   (1) Set the G2BCR0 register to provide the clock to the group 2 base timer.
   (2) Set all bits BT0S to BT2S to 0 (base timer is reset).
   (3) Set other registers associated with the intelligent I/O.
   The BTiS bit allows the base timers of two or all groups to start counting simultaneously (i = 0 to 2).
   To start counting individually, the BTiS bit should be set to 0 and the BTS bit in the GiBCR1 register should be set.

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Supply a clock to the registers.

| b7 | | | | | | | b0 |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Group i Base Timer Control Register 0 (GiBCR0) (i = 0 to 2)(1)

| | | |
|---|---|---|
| BCK1 and BCK0 | Count Source Select Bit | 11b: f1 |
| DIV4 to DIV0 | Count Source Divide Ratio Select Bit | 11111b: No division |
| IT | Base Timer InterruptSource Select Bit | 0: Overflow of bit 15 or the bit 9 |

Note:
1. To enable each register immediately after it is set, set these bits to 1111111b.

Set the base timer reset source.

| b7 | | | | | | | b0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

Group i Base Timer Control Register 1 (GiBCR1) (i = 0 to 2)

| | | |
|---|---|---|
| RST0 | Base Timer Reset Select Bit 0 | 0: No reset |
| RST1 | Base Timer Reset Source Select Bit 1 | 1: Match with the GiPO0 register (1) |
| RST2 | Base Timer Reset Source Select Bit 2 | 0: No reset |
| Set to 0. | | |
| BTS | Base Timer Start Bit (2) | 0: Reset the base timer |
| UD1 and UD0 | Increment/Decrement Counting Control Bit | 00b: Increment counting mode |
| Set to 0. | | |

Note:
1. The base timer is reset after two fBTi clock cycles if the base timer value has matched the GiPO0 register setting. When the RST1 bit is set to 1, the value of the GiPOj register to be used for the waveform generation should be smaller than that of the GiPO0 register (j = 1 to 7).
2. After setting the intelligent I/O related registers, set this bit to 1.

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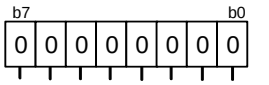
Set the waveform control (1).




Group i Waveform Generation Register j (GiPOCRj) (i = 0 to 2; j = 0 to 7)

MOD2 to MOD0 — Operation Mode Select Bit
000b: Single-phase waveform output mode

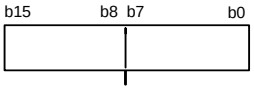
Set to 0.

RLD — GiPOj Register Value Reload Timing Select Bit
0: Reload the value on a write access(1)

Set to 0.

Note:
1. This bit is enabled immediately after writing to the GiPOj register.

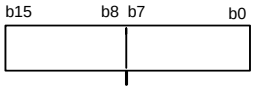
Set the cycle.




Group i Waveform Generation Register 0 (GiPO0) (i = 0 to 2)

Set the PWM cycle starting point. When the set value is n, the PWM cycle is:

$$\frac{1}{f_{BTi}} \times (n+2)$$




Group i Waveform Generation Register j (GiPOj, GiPOk) (i = 0 to 2; j = 2, 4, 6; k = j +1)

Set a start point of set and reset widths.
When setting the value to m, the set and reset widths are:

$$\frac{1}{f_{BTi}} \times m$$

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Set the waveform control (2).

b7 b0

| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|

Group i Waveform Generation Control Register 0 (GiPOCR0) (i = 0 to 2)

- MOD2 to MOD0 — Operation Mode Select Bit
  - 000b: Single-phase waveform output mode
- Set to 0
- RLD — GiPOj Register Value Reload Timing Select Bit
  - 1: Reload the value into the GiPOj register when the base timer is reset
- Set to 0
- INV — Output Level Inversion Select Bit (1)
  - 0: Do not invert the output level

b7 b0

| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
|---|---|---|---|---|---|---|---|

Group i Waveform Generation Control Register 0 (GiPOCRj) (i = 0 to 2; j = 2 to 7)

- MOD2 to MOD0 — Operating Mode Select Bit (2)
  - 000b: SR waveform output mode
- Set to 0
- IVL — Default Output Value Select Bit (3)
  - 0: Output low as default value
- RLD — GiPOj Register Value Reload Timing Select Bit
  - 1: Reload the value into the GiPOj register when the base timer is reset
- Set to 0
- INV — Output Level Inversion Select Bit (1)
  - 0: Do not invert the output level

Notes:
1. The output level inversion is the final step in the waveform generation process. When the INV bit is set to 1 (output level is inverted), high is output by setting the IVL bit to 0 (output low as default value), and vice versa.
2. The value written to the next channel after an even channel setting is ignored. Set to 000b.
3. The setting value is output by a write to the IVL bit if the FSCj bit in the GiFS register is set to 0 (waveform generation selected) and the IFEj bit in the GiFE register is set to 1 (function for channel j enabled).

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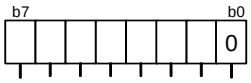
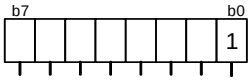
Enable functions.




Group i Function Select Register (GiFS) (i = 0, 1)

FSC0 Channel 0 Time Measurement/Waveform Generation Select Bit
0: Select the waveform generation

FSCj Channel j Time Measurement/Waveform Generation Select Bit (j = 1 to 7)
0: Select the waveform generation
1: Select the time measurement




Group i Function Enable Register (GiFE) (i = 0 to 2)

IFE0 Channel 0 Function Enable Bit
1: Enable the function for channel 0

IFEj Channel j Function Enable Bit (j = 1 to 7) (1)
0: Disable the function for channel j
1: Enable the function for channel j

Notes:
1. Set unused channels to 0.

Insert wait time
Wait at least 2 fBTi clock cycles.

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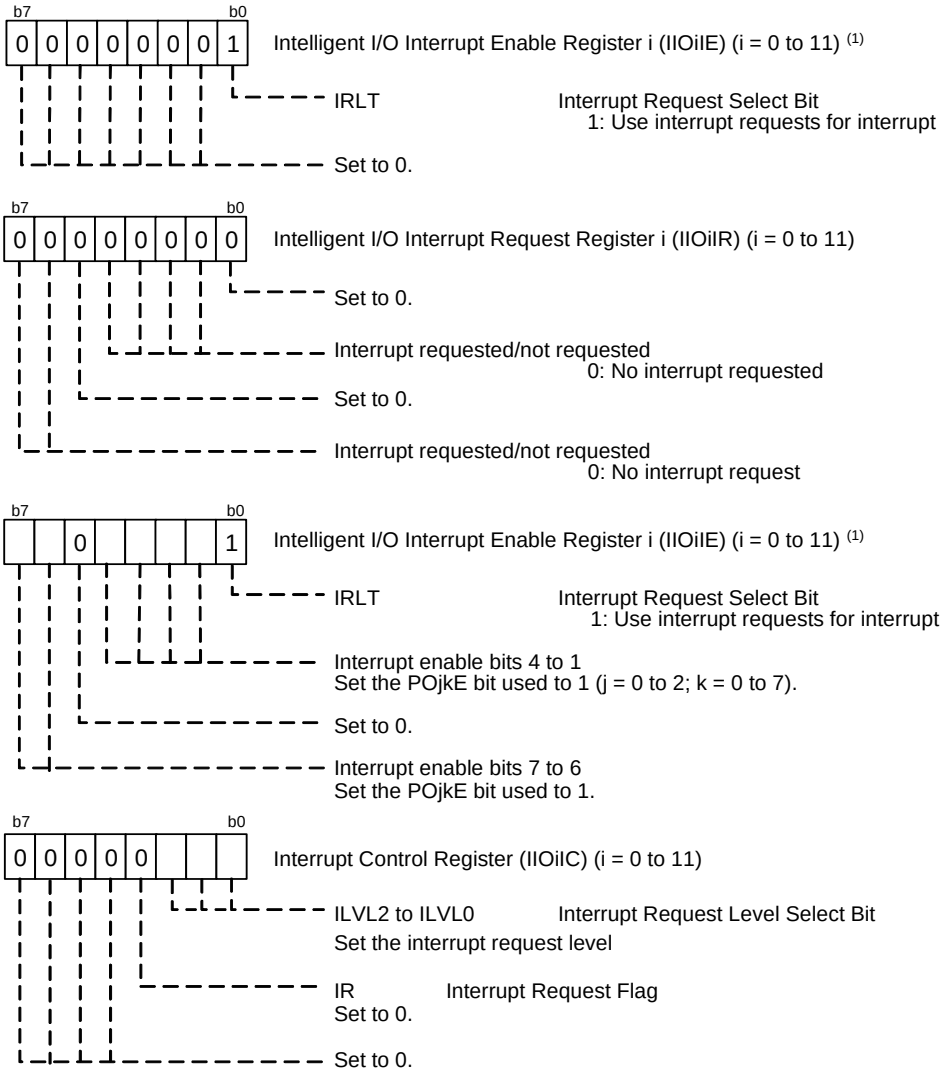
Setting interrupts.




Notes:
1. Do not set the IRLT bit and bits 1 to 7 to 1 at the same time.

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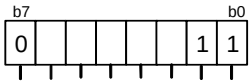
Set the output port.

For the port used for outputting in the intelligent I/O, set the corresponding bit of the PDi register (i = 0 to 13) to 1. Then select the function with P1_0S to P1_7S, P4_3S, P6_4S, P7_0S to P7_1S, P7_3S to P7_7S, P8_1S, P9_2S, P11_0S to P11_3S, P13_0S to P13_7S, and P15_0S to P15_7S.

Enable interrupts

Set the I flag to 1 to enable interrupts.

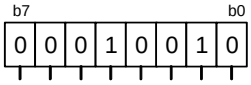
Set the divide ratio.




Group i Base Timer Control Register 0 (GiBCR0) (i = 0 to 2)

| | |
|---|---|
| BCK1 and BCK0 | Count Source Select Bit<br>11b: f1 |
| DIV4 to DIV0 | Count Source Divide Ratio Select Bit<br>Set the desired divide ratio. |
| Set to 0. | |

Start the base timer.




Group i Base Timer Control Register 1 (GiBCR1) (i = 0 to 2)

| | |
|---|---|
| RST0 | Base Timer Reset Source Select Bit 0<br>0: No reset |
| RST1 | Base Timer Reset Source Select Bit 1<br>1: Match with the GiPO0 register |
| RST2 | Base Timer Reset Source Select Bit 2<br>0: No reset |
| Set to 0. | |
| BTS | Base Timer Start Bit (1, 2)<br>0: Reset the base timer |
| UD1 and UD0 | Increment/Decrement Counting Control Bit<br>00b: Increment counting mode |
| Set to 0. | |

Notes:
1. To start the base timers in groups 0 and 1 individually, the BTS bit should be set to 1 after setting the BTkS bit in the BTSR register to 0 (base timer is reset) (k = 0 to 2).
2. To start the base timers of two or all groups simultaneously, the BTSR register should be used. The BTS bit should be set to 0.

## 4.4 Precautions to Take when Using Interrupts

In the intelligent I/O interrupt handler, make sure to set the IIOkIR register that corresponds to the interrupt concerned to 00h (initialized) (k = 0 to 11). Unless this register setting is made, even if an interrupt request from the intelligent I/O is generated, the IR bit in the IIOkIC register will not be set to 1 (interrupt not generated).
Also, read the GiBT register to confirm that the base timer is reset, before setting the GiPO0 and GiPOj registers (i = 0 to 2; j = 0 to 7). Refer to Figure 4.3 for details.

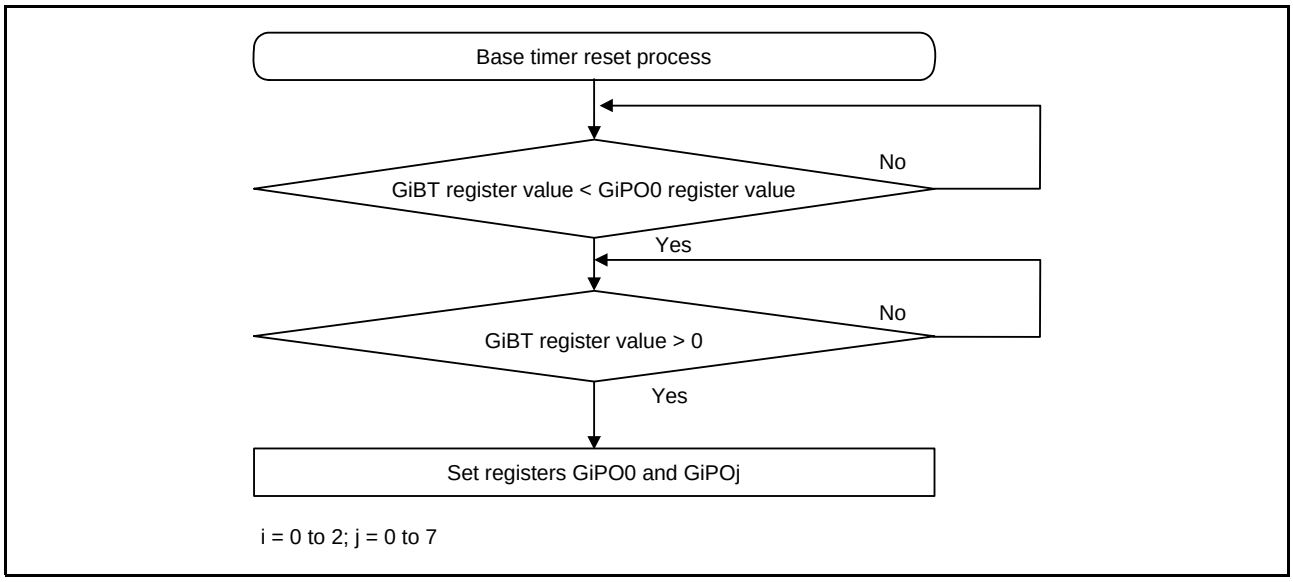



**Figure 4.3 Base Timer Reset Processing Procedure**

# 5. Sample Programs

Sample programs can be downloaded from the Renesas Electronics website.

## 5.1 Description of the Sample Program

The sample program uses intelligent I/O group 0 to output SR waveform from the IIO0_4 (P1_4) pin.
Each time an intelligent I/O interrupt is generated, a waveform with a different PWM cycle and different low level width is output. IIO0_0 (P1_0) outputs a single-phase waveform.

### 5.1.1 Clock Conditions and Output Waveforms

The set clock frequencies in the sample program are listed in Table 5.1

**Table 5.1 Set Clock Frequencies**

| Clock Name | Frequency |
|---|---|
| Main clock (XIN) | 16 MHz |
| PLL clock | 100 MHz |
| Base clock | 50 MHz |
| CPU clock | 50 MHz |
| Peripheral bus clock | 25 MHz |
| Peripheral clock source | 25 MHz |

The IIO pins used in the sample program and their corresponding output ports are listed in Table 5.2

**Table 5.2 Sample Program and Corresponding Output Ports**

| IIO Pin | Output Port |
|---|---|
| IIO0_0 | P1_0 |
| IIO0_4 | P1_4 |
| IIO0_5 | |

Figure 5.1 shows the Output Waveform Produced by the Sample Program.

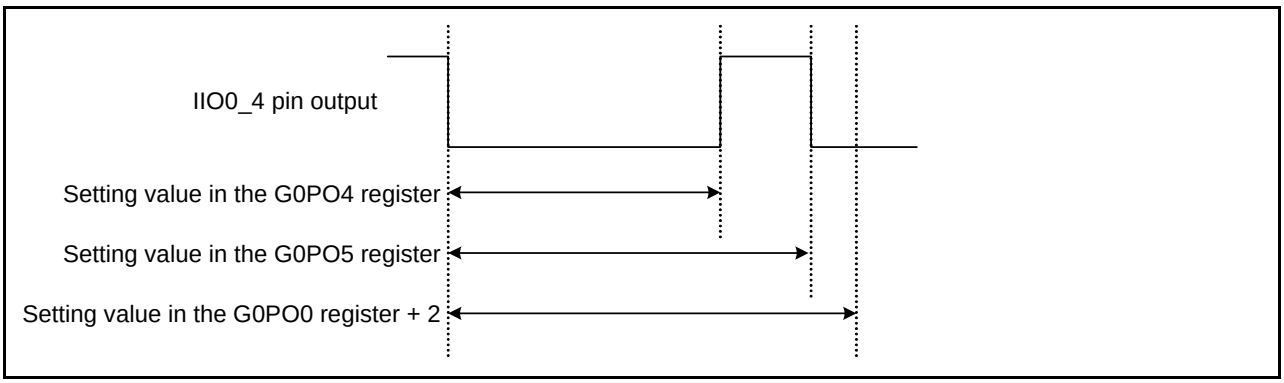



**Figure 5.1 Output Waveform Produced by the Sample Program**

Table 5.1 lists the Waveform Generation Registers of Intelligent I/O and Their Set Patterns Used in the Sample Program. Figure 5.1 shows the Output Waveform Produced by the Sample Program. The numbers in parentheses in Table 5.1 denote the length of time based on the clock condition in Table 3.2.

**Table 5.1 Waveform Generation Registers of Intelligent I/O and Their Set Patterns Used in the Sample Program**

| | Pattern 1 | Pattern 2 | Pattern 3 | Pattern 4 | Pattern 5 |
|---|---|---|---|---|---|
| G0PO0 | 1000 (40.08 μs) | 1400 (56.08 μs) | 1800 (72.08 μs) | 2200 (88.08 μs) | 2600 (104.08 μs) |
| G0PO4 | 250 (10 μs) | 350 (14 μs) | 450 (18 μs) | 550 (22 μs) | 650 (26 μs) |
| G0PO5 | 750 (30 μs) | 1050 (42 μs) | 1350 (54 μs) | 1650 (66 μs) | 1950 (78 μs) |

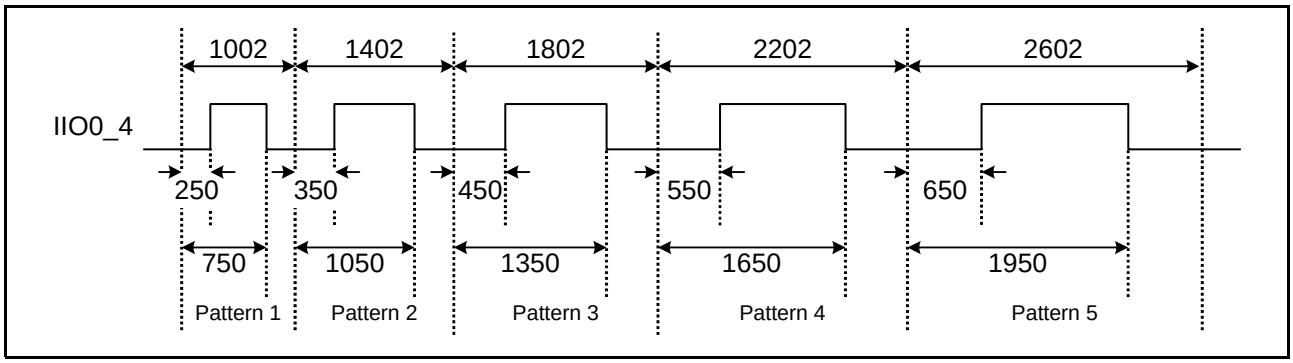



**Figure 5.2 IIO Pins and Output Patterns Used in the Sample Program**

Figure 5.3 shows the PR Waveform Output Timing.

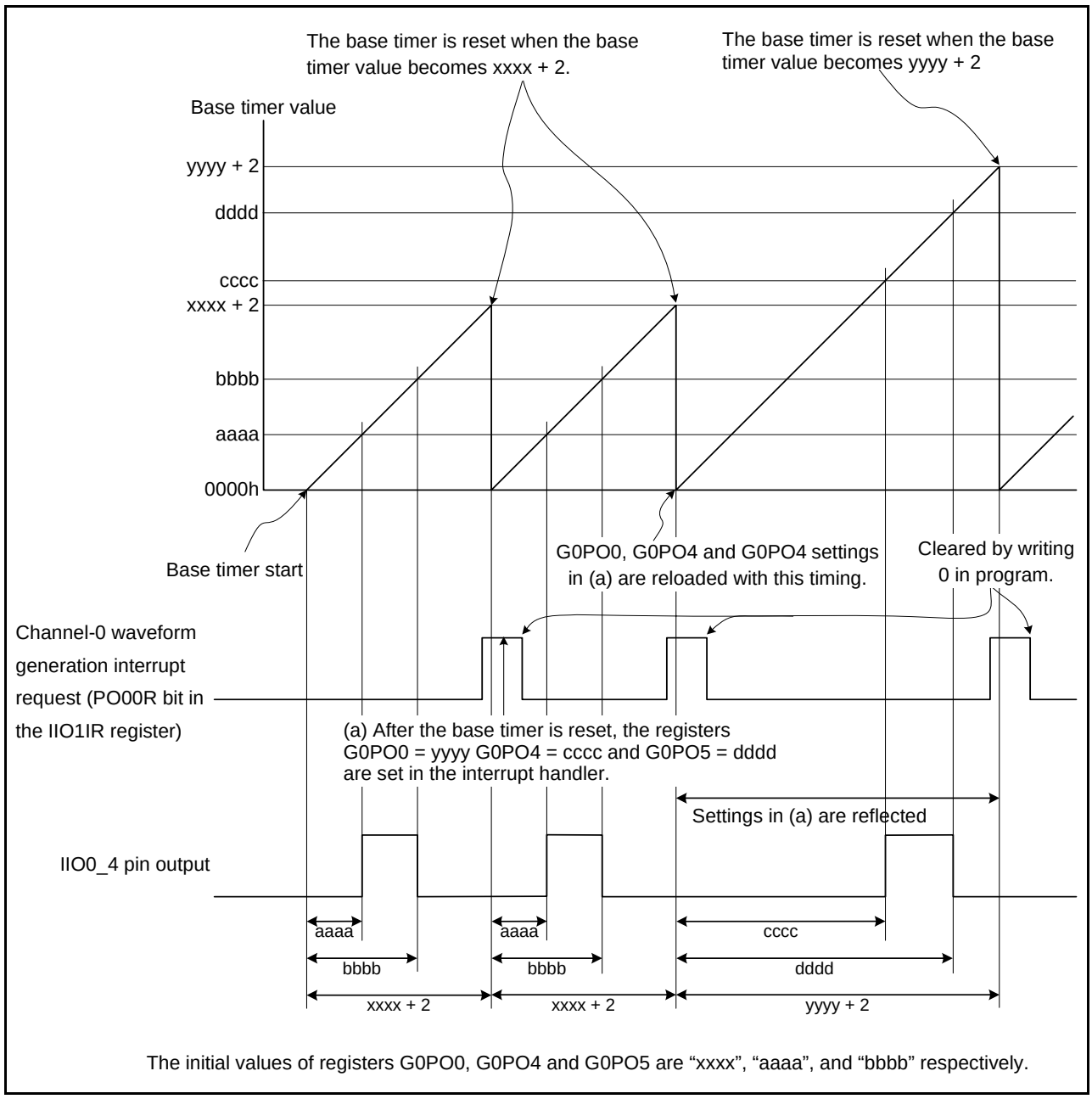



**Figure 5.3 PR Waveform Output Timing**

## 5.2 Program Flowchart

The sample program is comprised of the main function and the intelligent I/O interrupt function.
Figure 5.4 shows the Program Flowchart of Main Function. Figure 5.5 shows the Flowchart of Intelligent I/O Interrupt Function. Note that the numbers (1) through (22) in the diagram correspond to the flowchart numbers of the sample program.

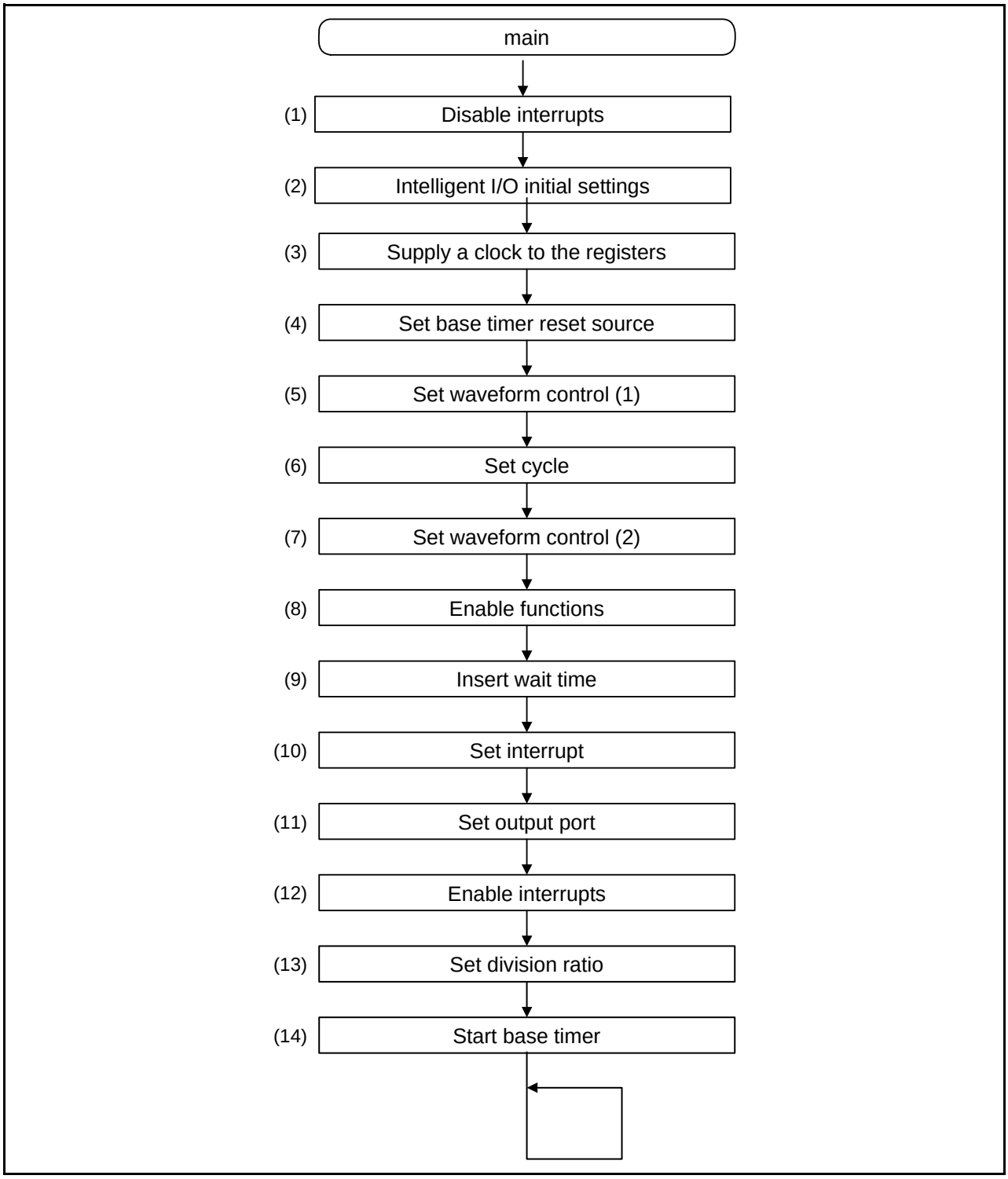



**Figure 5.4 Program Flowchart of Main Function**

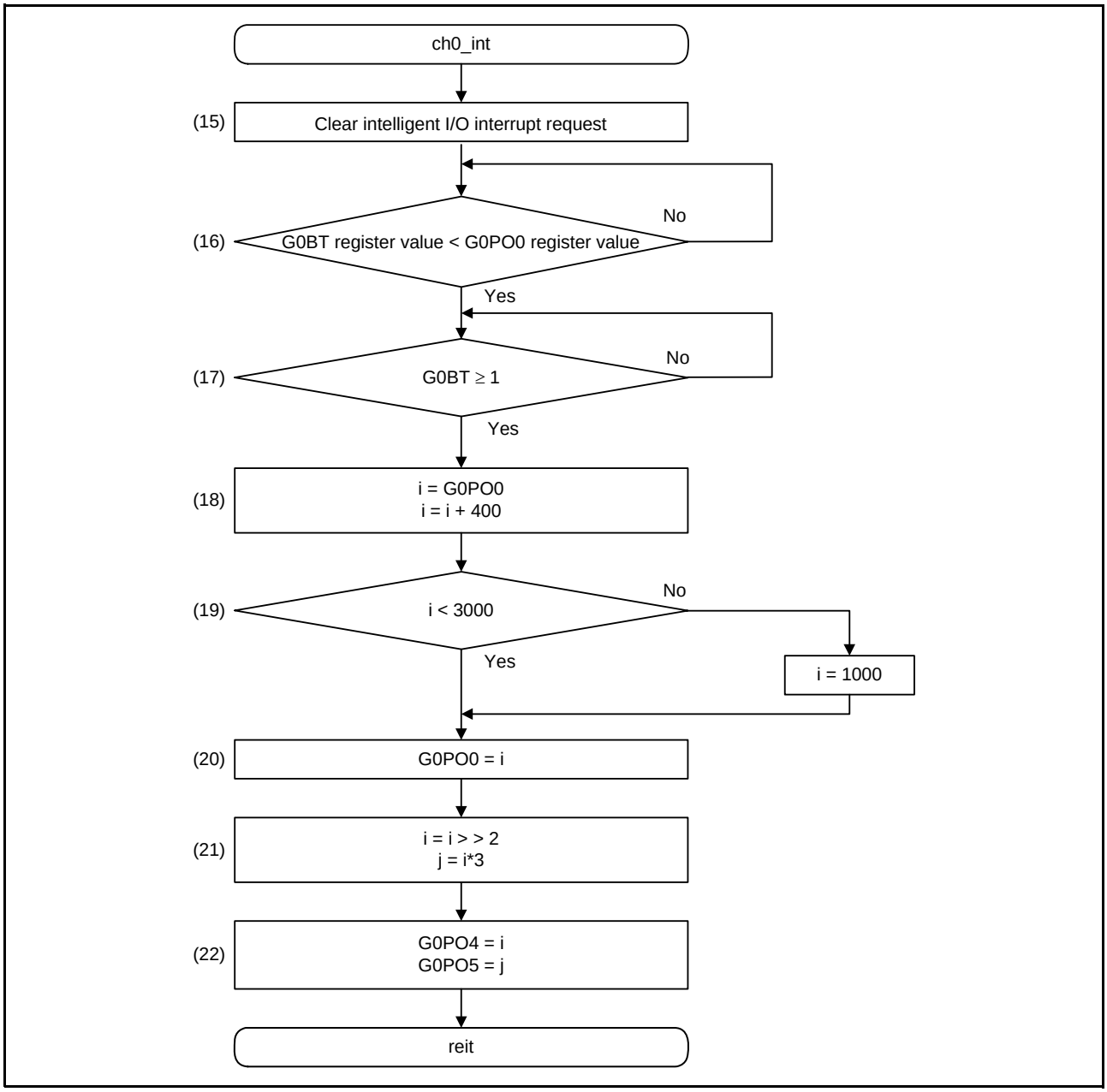



**Figure 5.5 Intelligent I/O Interrupt Function Flowchart**

# 6. Reference Documents

Hardware Manual
R32C/118 Group Hardware Manual Rev.1.00
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C compiler manual
R32C/100 Family C compiler package V.1.02 C compiler user manual Rev.1.00
The latest version can be downloaded from the Renesas Electronics website.

# Website and Support

Renesas Electronics website
http://www.renesas.com/

Inquiries
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| Revision History | R32C/100 Series<br>Intelligent I/O SR Waveform Output Mode |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | May 06, 2010 | — | First edition issued |
| | | | |

# General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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