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H8SX Family

Input Capture by Using the Input-Output Multiplexing Function of TPU Pins

Summary

The input capture function of the 16-bit timer unit (TPU) is applied to measure the width at high level and period of an input pulse signal. By applying the TPU input-output multiplexing function of H8SX microcontrollers, input pins required for simultaneously measuring the width at high level and period can be reduced to one from the conventional two.

Target Device

H8SX/1663F, H8SX/1638F

Introduction

Descriptions in this application note are in line with those in the hardware manual for the H8SX/1663 group, and the program is usable on the above device for which operation has been confirmed.

However, since some functions and the set of included functions will vary with the actual device in use, only apply the program after full evaluation with confirmation against the relevant hardware manual.

Contents

1. Specifications

The TPU functions for multiplexing of input-output pins and input-capture are applied to measure the width at high level and period of an input pulse signal by using a single TIOC input pin.

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Details
Operating frequencies	EXTAL input clock: 12 MHz System clock (Iϕ): 48 MHz (input clock frequency-multiplied by 4) Peripheral-module clock (Pϕ): 24 MHz (input clock frequency-multiplied by 2) External-bus clock (Bϕ): 48 MHz (input clock frequency-multiplied by 4)
MD_CLK pin	MD_CLK = 0
Operating mode	Mode 7 (single-chip mode) Mode-pin setting: MD2 = 1, MD1 = 1, MD0 = 1

3. Description of Operation

3.1 Multiplexing of TPU Input–Output Pins

Figure 1 shows an example of the usual configuration for pulse measurement. Figure 2 shows an example of the configuration when the multiplexing function for TPU input–output pins is applied. The input pins for input capture are determined by the selection bits for the multiplexing function of TPU input–output pins in register PFCR9. The TPUMS0A bit of PFCR9 is set to 1 in this example so that the TIOCA0 input pin for TGRA_0 and the TIOCB0 input pin for TGRB_0 is the same pin (P31). In this way, the input for input capture to TGRA_0 and TGRB_0 becomes the input on the single P31/TIOCA0/TIOCB0 pin.

Note: The multiplexing function for TPU input–output pins is only applicable to input settings. Common application is not possible when the TIOCA0 pin has been set as an output.

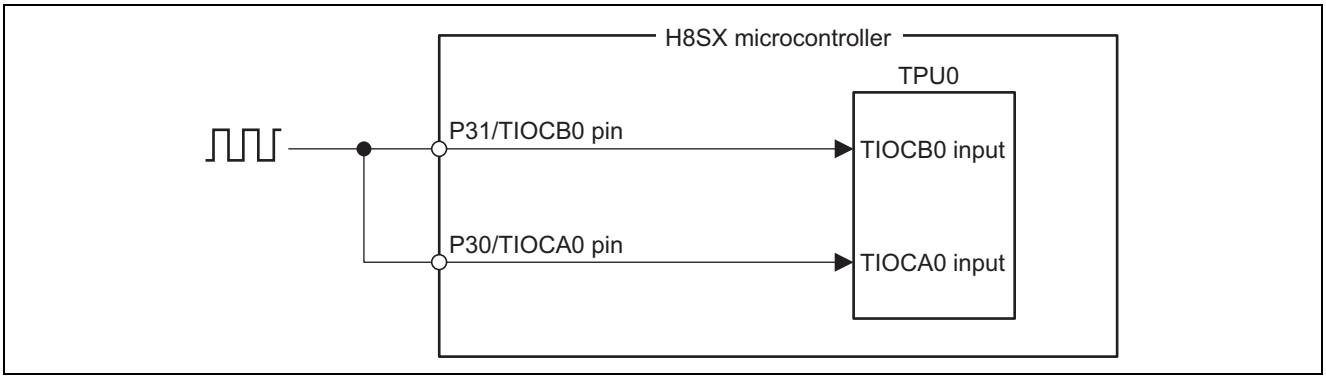


Figure 1 Example of the Usual form of Connection for Pulse Measurement

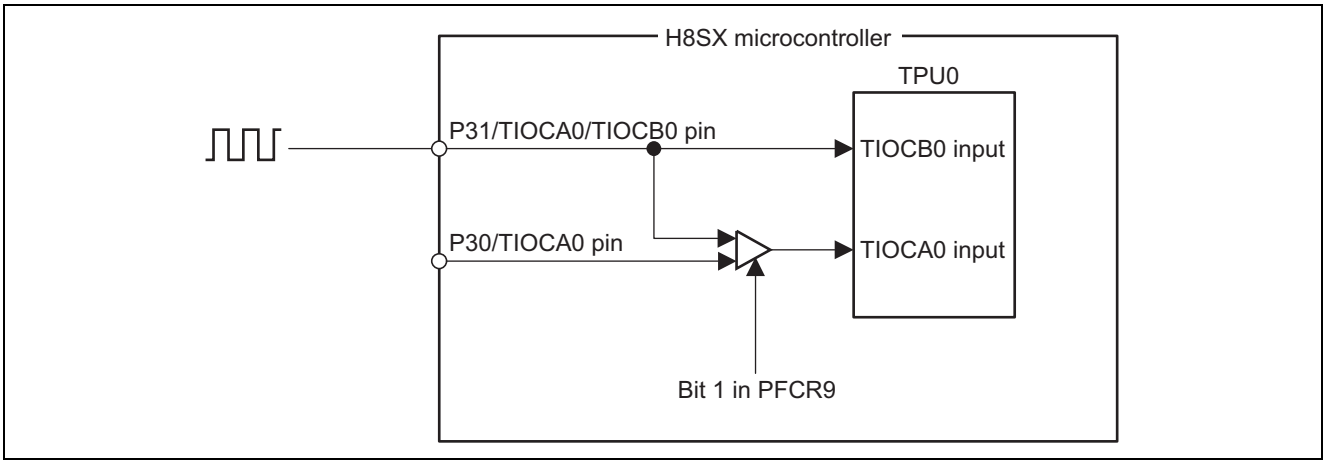


Figure 2 Example of the Connection for Pulse Measurement when the Multiplexing Function for TPU Input-Output Pins is Applied

3.2 Example of the Setting Procedure

An example of the settings for measuring the width at high level and period of a pulse signal by using the input-output multiplexing function for TPU pins is shown in Figure 3. The settings below are for transfer of the number counted while the input pulse is at the high level to TGRA_0 and of the number counted during one period of the input pulse signal to TGRB_0.

1. This setting is for clearing of the TCNT_0 counter by input capture in TGRB_0.
2. TIORH_0 is used to set TGRA_0 and TGRB_0 as input-capture registers. Falling is selected as the input edge on the TIOCA0 input that causes input capture. Rising is selected as the input edge on the TIOCB0 input that causes input capture.
3. The multiplexed-pin function setting for the P31/TIOCA0/TIOCB0 pin is made. Setting the TPUMS0A bit in PFCR9 to 1 selects common operation of the P31/TIOCA0/TIOCB0 pin for TIOCA0 input and TIOCB0 input.
4. Setting the CST0 in TSTR to 1 starts counter operation.

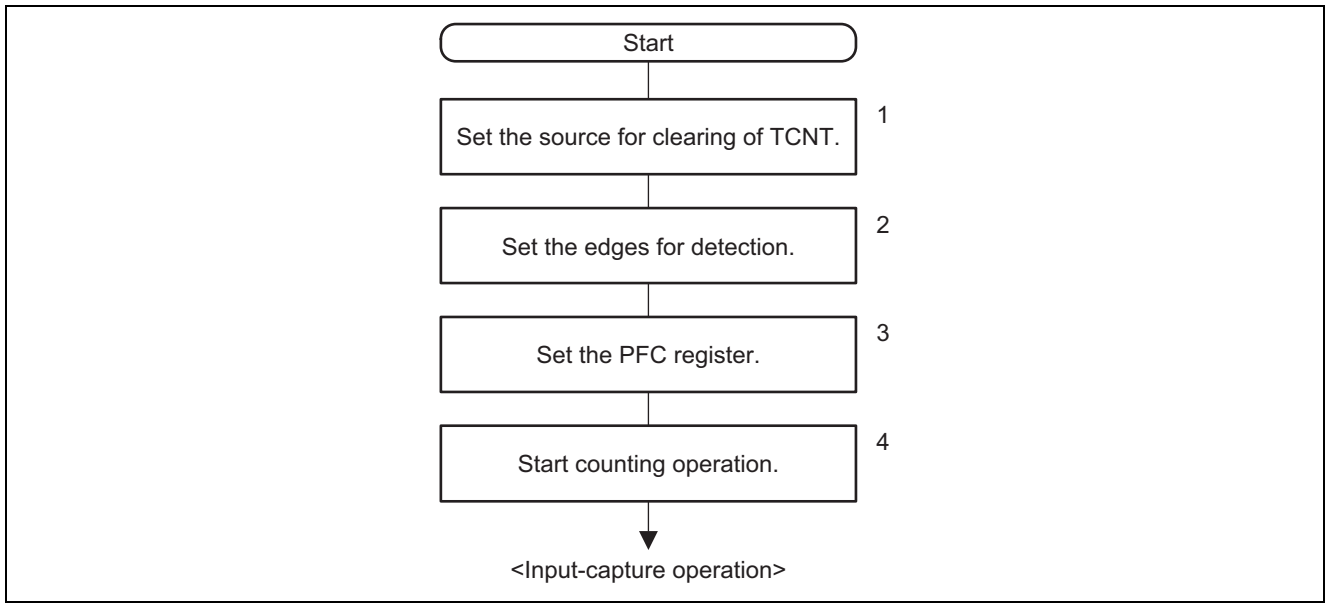


Figure 3 Example of Settings to Apply the Input–Output Multiplexing Function of a TPU Pin for Measuring the Width at High Level and Period of a Pulse Signal

3.3 Example of Measurement of the Width at High Level and Period of the Pulse Signal

Figure 4 illustrates operations for measuring the width at high level and period of the pulse signal. Table 2 gives detailed descriptions of points (1) to (4) in the figure. Please refer to the combination of figure 4 and table 2.

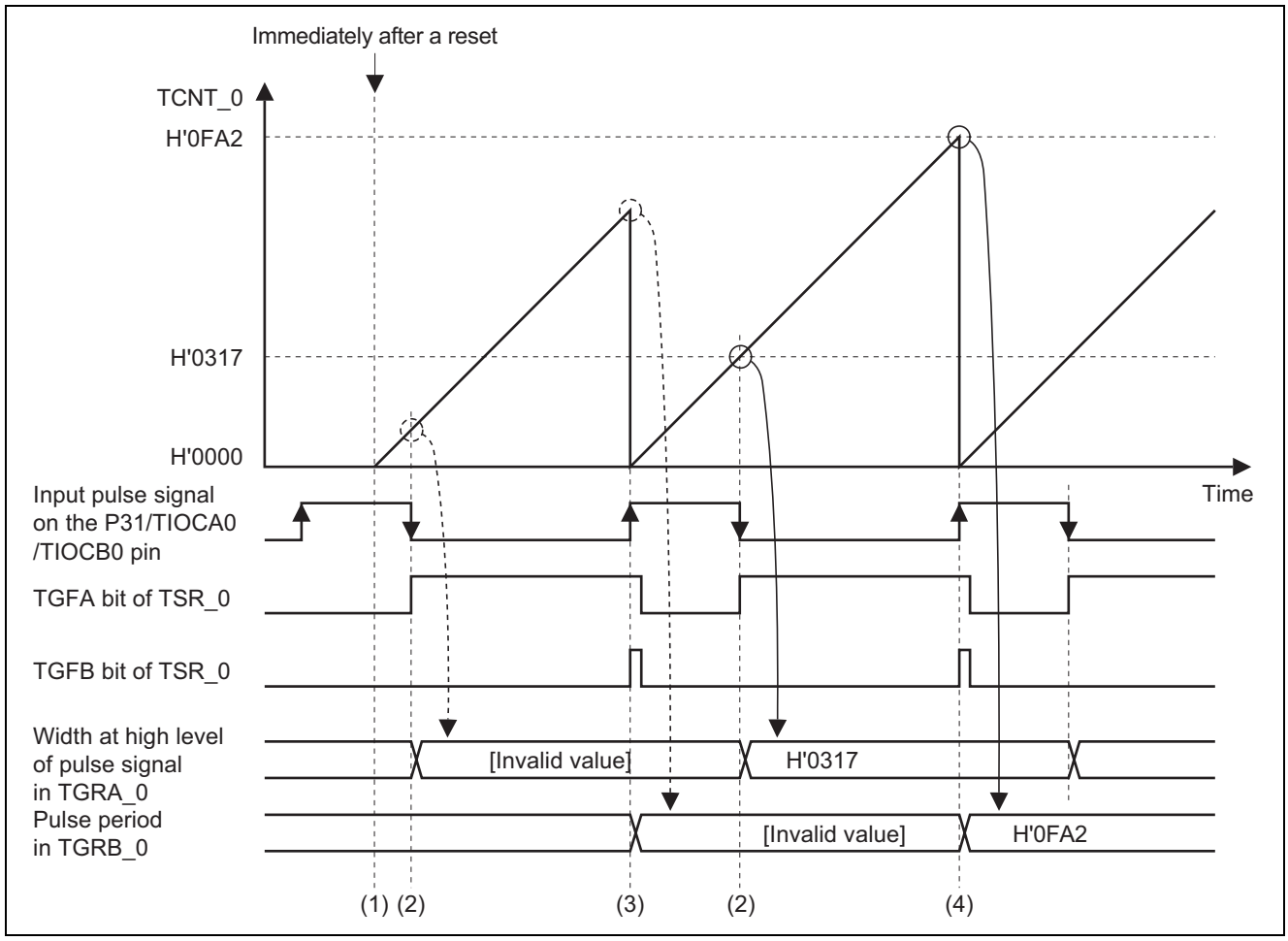


Figure 4 Example of Operation to Measure the Width at High Level and Period of a Pulse Signal by Using the Input-Output Multiplexing Function of a TPU Pin

Table 2 Details of Processing

	Hardware Processing	Software Processing
(1)	No processing	Initial settings For details, see "3.2 Example of the Setting Procedure" and "4. Description of Software".
(2)	(a) Generation of input-capture to TGRA_0 (b) Transfer of value from TCNT_0 to TGRA_0 (c) Setting the TGFA bit in TSR_0 to 1	(a) Poll until the value of the TGFB in TSR_0 becomes 1.
(3)	(a) Generation of input-capture to TGRB_0 (b) Transfer of value from TCNT_0 to TGRB_0 (c) Setting the TGFB bit in TSR_0 to 1 (d) Clearing TCNT_0 (to 0)	(a) Clear (to 0) the TGFA and TGFB bits in TSR_0.
(4)	(a) Generation of input-capture to TGRB_0 (b) Transfer of value from TCNT_0 to TGRB_0 (c) Setting the TGFB bit in TSR_0 to 1 (d) Clearing TCNT_0 (to 0)	(a) Copy the value for pulse width at high level in TGRA_0 to RAM (plshigh). (b) Copy the value for pulse-signal period in TGRB_0 to RAM (plsperiod).

[Legend]
TGRA_0: Timer general register A_0
TGRB_0: Timer general register B_0
TCNT_0: Timer counter 0
TSR_0: Timer status register 0

3.4 Formulae for Calculating Measured Values for the Pulse Signal

The width at high level and period of the input pulse signal are calculated from the values of the counter clock for TCNT_0, and of TGRA_0 and TGRB_0. Calculation of the width at high level and period of the pulse signal is shown below.

When Pϕ = 24 MHz and TGRA_0 = H'0317

pulse width at high level = (TGRA_0 + 1)/Pϕ/1 = (H'0317 + 1)/24 MHz
= 33 µs.

When Pϕ = 24 MHz and TGRB_0 = H'0FA2

pulse period = (TGRB_0 + 1)/Pϕ/1 = (H'0FA2 + 1)/24 MHz
= 166.79… µs ≅ 166.8 µs.

4. Description of Software

4.1 Operating Environment

Table 3 Operating Environment

Item	Details
Development tool	High-performance Embedded Workshop Ver. 4.03.00
C/C++ compiler	H8, H8/300 Series C/C++ Compiler Ver. 6.02.00 from Renesas Technology
	Option settings: -cpu=h8sxa:24:md, -code = machinecode, -optimize=1, -regparam=3 -speed=(register, shift, struct, expression)
Optimizing linkage editor	Optimizing Linkage Editor Ver. 9.03.00 from Renesas Technology
	Option settings: None

Table 4 Section Settings

Address	Section Name	Description
H'001000	P	Program area
H'FF2000	B	Non-initialized data area (RAM area)

Table 5 Exception-processing vector table

Requesting Source	Vector Number	Vector Table Address	Destination Processing Function
Reset	0	H'000000	init

4.2 List of Functions

Table 6 List of Functions

Function Name	Description
init	Initialization routine Releases required modules from the module-stop state, makes clock settings, and calls function main.
main	Main routine Sets the TPU input-capture function and input–output pin multiplexing function, and measures the width at high level and period of the input pulse signal.

4.3 RAM Usage

Table 7 RAM Usage

Type	Variable Name	Description	Used in (Function)
unsigned short	plshigh	Pulse width at high level Storage for the width at high level of the input pulse (2 bytes)	main
unsigned short	plsperiod	Pulse period Storage for the input pulse period (2 bytes)	main

4.4 Description of Functions

4.4.1 Function init

1. Functionality in outline
   Initialization routine. Releases the required modules from module-stop mode, makes clock settings, and calls the main function.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in the sample application are listed below. Note that the settings below are for this sample task and are not the initial values.

- Mode control register (MDCR) Number of bits: 16 Address: H'FFFDC0

Bit	Bit Name	Setting	R/W	Description
15	MDS7	—*	R	Indicates the value set by mode pin (MD3). When MDCR is read, the input level on the MD3 pin is latched. This latching is released by a reset.
11	MDS3	—*	R	Mode Select 3 to 0 These bits indicate the operating mode selected by the mode pins (MD2 to MD0) (see table 8). When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits. These latches are released by a reset.
10	MDS2	—*	R	
9	MDS1	—*	R	
8	MDS0	—*	R	

Note: * Determined by pins MD3 to MD0.

Table 8 Setting of Bits MDS3 to MDS0

MCU Operating Mode	Pins			MDCR			
	MD2	MD1	MD0	MDS3	MDS2	MDS1	MDS0
2	0	1	0	1	1	0	0
4	1	0	0	0	0	1	0
5	1	0	1	0	0	0	1
6	1	1	0	0	1	0	1
7	1	1	1	0	1	0	0

- System clock control register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Setting	R/W	Description
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock provided to
8	ICK0	0	R/W	the CPU, DMAC, and DTC. 000: Input clock × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: Input clock × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	000: Input clock × 4

- MSTPCRA, MSTPCRB, and MSTPCRC set the module stop function. Setting a bit to 1 makes the corresponding module enter the module stop state, while clearing the bit to 0 clears the module stop state.

- Module stop control register A (MSTPCRA) Number of bits: 16 Address: H'FFFDC8

Bit	Bit Name	Setting	R/W	Target Module
15	ACSE	0	R/W	All-Module-Clock-Stop Mode Enable Enables/disables all-module-clock-stop mode for reducing current consumption by stopping the bus controller and I/O ports operations when the CPU executes the SLEEP instruction after the module stop state has been set for all the on-chip peripheral modules controlled by MSTPCR. 0: All-module-clock-stop mode disabled. 1: All-module-clock-stop mode enabled.
13	MSTPA13	1	R/W	DMA controller (DMAC)
12	MSTPA12	1	R/W	Data transfer controller (DTC)
9	MSTPA9	1	R/W	8-bit timers (TMR_3 and TMR_2)
8	MSTPA8	1	R/W	8-bit timers (TMR_1 and TMR_0)
5	MSTPA5	1	R/W	D/A converter (channels 1 and 0)
3	MSTPA3	1	R/W	A/D converter (unit 0)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

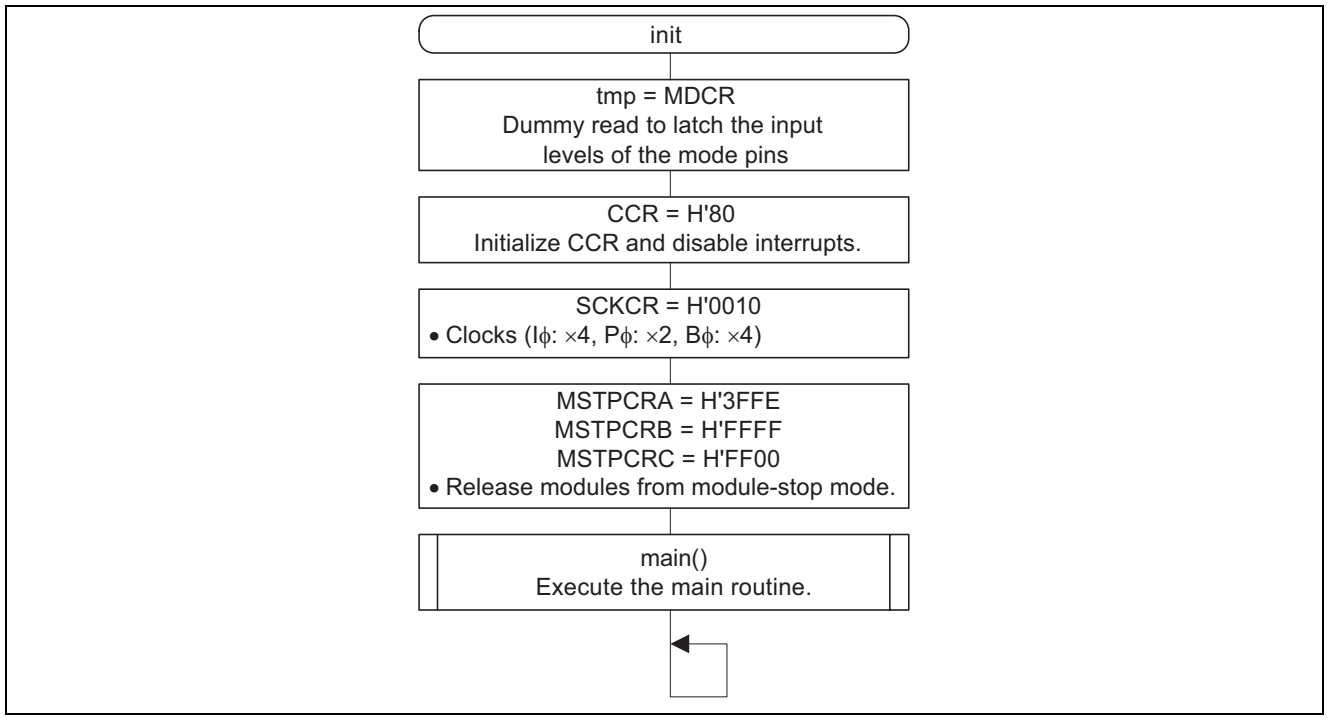
- Module stop control register B (MSTPCRB) Number of bits: 16 Address: H'FFFDCA

Bit	Bit Name	Setting	R/W	Target Module
15	MSTPB15	1	R/W	Programmable pulse generator (PPG)
12	MSTPB12	1	R/W	Serial communications interface_4 (SCI_4)
10	MSTPB10	1	R/W	Serial communications interface_2 (SCI_2)
9	MSTPB9	1	R/W	Serial communications interface_1 (SCI_1)
8	MSTPB8	1	R/W	Serial communications interface_0 (SCI_0)
7	MSTPB7	1	R/W	I^2C bus interface 1 (IIC_1)
6	MSTPB6	1	R/W	I^2C bus interface 0 (IIC_0)

- Module stop control register C (MSTPCRC) Number of bits: 16 Address: H'FFFDCC

Bit	Bit Name	Setting	R/W	Target Module
15	MSTPC15	1	R/W	Serial communications interface_5 (SCI_5), (IrDA)
14	MSTPC14	1	R/W	Serial communications interface_6 (SCI_6)
13	MSTPC13	1	R/W	8-bit timer (TMR_4, TMR_5)
12	MSTPC12	1	R/W	8-bit timer (TMR_6, TMR_7)
11	MSTPC11	1	R/W	Universal serial bus interface (USB)
10	MSTPC10	1	R/W	Cyclic redundancy check
4	MSTPC4	0	R/W	On-chip RAM_4 (H'FF2000 to H'FF3FFF)
3	MSTPC3	0	R/W	On-chip RAM_3 (H'FF4000 to H'FF5FFF)
2	MSTPC2	0	R/W	On-chip RAM_2 (H'FF6000 to H'FF7FFF)
1	MSTPC1	0	R/W	On-chip RAM_1 (H'FF8000 to H'FF9FFF)
0	MSTPC0	0	R/W	On-chip RAM_0 (H'FFA000 to H'FFBFFF)

5. Flowchart



4.4.2 Function main

1. Functionality in outline
   Main routine. Sets the TPU's input capture and input–output pin multiplexing functions, and measures the width at high level and period of the input pulse signal.
2. Arguments
   None
3. Return value
   None
4. Description of internal registers used
   The internal registers used in the sample application are listed below. Note that the settings below are for this sample task and are not the initial values.

- Port 3 Data Direction Register (P3DDR) Number of bits: 8 Address: H'FFFB82

Bit	Bit Name	Setting	R/W	Description
1	P31DDR	0	R/W	0: Sets pin P31 as an input pin 1: Sets pin P31 as an output pin

- Port 3 Input Buffer Control Register (P31CR) Number of bits: 8 Address: H'FFFB92

Bit	Bit Name	Setting	R/W	Description
1	P31ICR	1	R/W	0: Disables the input buffer on pin P31. The input signal from the pin is fixed to the high level. 1: Enables the input buffer on pin P31. The input signal reflects the pin state on the peripheral module side.

- Port Function Control Register 9 (PFCR9) Number of bits: 8 Address: H'FFFBC9

Bit	Bit Name	Setting	R/W	Description
1	TPUMS0A	1	R/W	TPU I/O Pin Multiplex Function Select Selects TIOCA0 function 0: Specifies P30 as output compare output and input capture 1: Specifies P31 as input capture input and P30 as output compare

- Timer start register (TSTR) Number of bits: 8 Address: H'FFFFBC

Bit	Bit Name	Setting	R/W	Description
5	CST5	0	R/W	Counter Start 5 to 0
4	CST4	0	R/W	These bits select operation or stoppage for TCNT.
3	CST3	0	R/W	0: TCNT_5 to TCNT_0 count operation is stopped
2	CST2	0	R/W	1: TCNT_5 to TCNT_0 performs count operation
1	CST1	0	R/W	
0	CST0	0	R/W	

- Timer control register (TCR) Number of bits: 8 Address: H'FFFFC0

Bit	Bit Name	Setting	R/W	Description
7	CCLR2	0	R/W	Counter Clear 2 to 0
6	CCLR1	1	R/W	These bits select the TCNT counter clearing source.
5	CCLR0	0	R/W	010: TGRB_0 compare match/input capture
4	CKEG1	0	R/W	Clock Edge 1 and 0
3	CKEG0	0	R/W	These bits select the input clock edge. 00: Counted on falling edge
2	TPSC2	0	R/W	Timer Prescaler 2 to 0
1	TPSC1	0	R/W	These bits select the TCNT counter clock.
0	TPSC0	0	R/W	000: Internal clock: counts on Pϕ/1

- Timer mode register_0 (TMDR_0) Number of bits: 8 Address: H'FFFFC1

Bit	Bit Name	Setting	R/W	Description
3	MD3	0	R/W	Modes 3 to 0
2	MD2	0	R/W	Set the timer operating mode.
1	MD1	0	R/W	0000: Normal operation
0	MD0	0	R/W	

- Timer I/O control register H_0 (TIORH_0) Number of bits: 8 Address: H'FFFFC2

Bit	Bit Name	Setting	R/W	Description
7	IOB3	1	R/W	I/O Control B3 to B0
6	IOB2	0	R/W	Specify the function of TGRB_0.
5	IOB1	0	R/W	10000: TGRB_0 functions as input capture register. Input
4	IOB0	0	R/W	capture occurs on the rising edge of P31/TIOCA0/TIOCB0 pin.
3	IOA3	1	R/W	I/O Control A3 to A0
2	IOA2	0	R/W	Specify the function of TGRA_0.
1	IOA1	0	R/W	10001: TGRA_0 functions as input capture register. When
0	IOA0	1	R/W	TPUMS0A in PFCR9 = 1, input capture occurs on the falling edge of P31/TIOCA0/TIOCB0 pin.

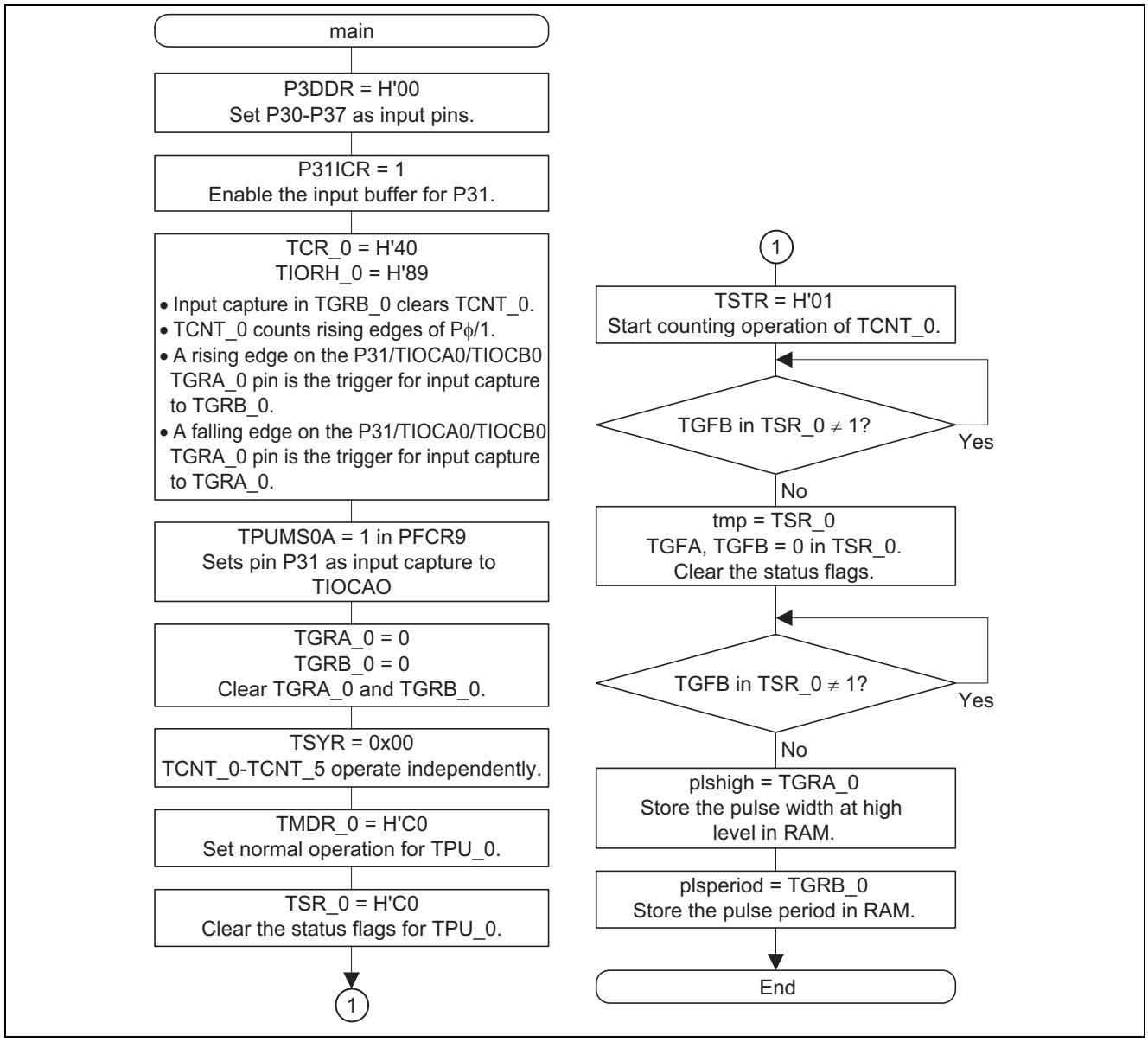
- Timer status register_0 (TSR_0) Number of bits: 8 Address: H'FFFFC5

Bit	Bit Name	Setting	R/W	Description
1	TGFB	0	R/(W)*	Input Capture/Output Compare Flag B When TGRB_0 is functioning as input capture [Setting conditions] When TCNT value is transferred to TGRB by input capture signal [Clearing conditions] When 0 is written to TGFB after reading TGFB = 1
0	TGFA	0	R/(W)*	Input Capture/Output Compare Flag A When TGRA_1 is functioning as input capture [Setting conditions] When TCNT value is transferred to TGRA by input capture signal [Clearing conditions] When 0 is written to TGFA after reading TGFA = 1

Note: * Only 0 can be written to clear the flag.

- Timer general register A_0 (TGRA_0) Number of bits: 16 Address: H'FFFFC8
  Function: TGRA_0 is used as an input capture register.
  Setting: H'0000
- Timer general register B_0 (TGRB_0) Number of bits: 16 Address: H'FFFFCA
  Function: TGRB_0 is used as an input-capture register.
  Setting: H'0000

5. Flowchart


main
P3DDR = H'00
Set P30-P37 as input pins.
P31ICR = 1
Enable the input buffer for P31.
TCR_0 = H'40
TIORH_0 = H'89
• Input capture in TGRB_0 clears TCNT_0.
• TCNT_0 counts rising edges of Pϕ/1.
• A rising edge on the P31/TIOCA0/TIOCB0 TGRA_0 pin is the trigger for input capture to TGRB_0.
• A falling edge on the P31/TIOCA0/TIOCB0 TGRA_0 pin is the trigger for input capture to TGRA_0.
TPUMS0A = 1 in PFCR9
Sets pin P31 as input capture to TIOCAO
TGRA_0 = 0
TGRB_0 = 0
Clear TGRA_0 and TGRB_0.
TSYR = 0x00
TCNT_0-TCNT_5 operate independently.
TMDR_0 = H'C0
Set normal operation for TPU_0.
TSR_0 = H'C0
Clear the status flags for TPU_0.
1
1
TSTR = H'01
Start counting operation of TCNT_0.
TGFB in TSR_0 ≠ 1?
Yes
No
tmp = TSR_0
TGFA, TGFB = 0 in TSR_0.
Clear the status flags.
TGFB in TSR_0 ≠ 1?
Yes
No
plshigh = TGRA_0
Store the pulse width at high level in RAM.
plsperiod = TGRB_0
Store the pulse period in RAM.
End

5. Documents for Reference

- Hardware Manual
  H8SX/1663 Group Hardware Manual
  H8SX/1638 Group Hardware Manual
  The most up-to-date versions of these documents are available on the Renesas Technology Website.
- Technical News/Technical Update
  The most up-to-date information is available on the Renesas Technology Website.

6. Point for Caution

When a pin of the device is used as an input pin for a peripheral module, be sure to set the corresponding bit of the input buffer control register (PnICR) to 1.

See the hardware manual for details.

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