Industrial Ethernet PHY
Layout recommendations and design rules

Single PHY ASSP

uPD60610,
uPD60611
(1) List of Abbreviations and Acronyms

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Full Form</th>
</tr>
</thead>
<tbody>
<tr>
<td>AGND</td>
<td>Analogue Ground</td>
</tr>
<tr>
<td>ASSP</td>
<td>Application Specific Standard Product</td>
</tr>
<tr>
<td>DGND</td>
<td>Digital Ground</td>
</tr>
<tr>
<td>FGND</td>
<td>Frame Ground</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>IO</td>
<td>Input - Output</td>
</tr>
<tr>
<td>LED-MUX</td>
<td>LED Multiplexing</td>
</tr>
<tr>
<td>MAC</td>
<td>Media Access Control</td>
</tr>
<tr>
<td>MDI</td>
<td>Media Dependent Interface</td>
</tr>
<tr>
<td>MII</td>
<td>Media Independent Interface</td>
</tr>
<tr>
<td>PD</td>
<td>Pull-Down</td>
</tr>
<tr>
<td>PHY</td>
<td>Physical Layer</td>
</tr>
<tr>
<td>PU</td>
<td>Pull-Up</td>
</tr>
<tr>
<td>RMS</td>
<td>Root Mean Square</td>
</tr>
<tr>
<td>UM</td>
<td>User’s Manual</td>
</tr>
</tbody>
</table>
Table of Contents

Chapter 1  General Information ................................................................. 4

Chapter 2  Strap Options................................................................. 5

Chapter 3  Media Dependent Interface ............................................ 7
  3.1 Differential Pair Routing .......................................................... 7
  3.2 Twisted Pair Interface ............................................................. 9
  3.3 Optical Interface ................................................................. 13
  3.4 Optical Signal Specification .................................................... 14
  3.5 Configurable Twisted Pair or Optical Interface ....................... 15

Chapter 4  MAC Interfaces – MII and RMII ........................................... 17

Chapter 5  Power Supply ................................................................. 21
  5.1 Power Supply Related Port Pins .............................................. 21
  5.2 3.3 V Power Supply .............................................................. 22
  5.3 1.5V Power Supply .............................................................. 23
    5.3.1 Regulator Operation – 1.5V Generation ............................ 23
    5.3.2 Regulator Disabled – External 1.5V Supply ....................... 25

Chapter 6  Layout of Power Supply and GND Planes ......................... 26
  6.1.1 3.3V supply ................................................................. 26
  6.1.2 External 1.5V supply ..................................................... 26
  6.1.3 GNDs ................................................................. 27
  6.1.4 Layout example ............................................................. 27

Chapter 7  External Reference Clock ................................................. 30
  7.1 Reference Clock ................................................................. 30
  7.2 Circuit and layout for clock input .......................................... 30

Chapter 8  LED Control ................................................................. 33

Chapter 9  EXTRES ........................................................................ 35

Chapter 10 Unused pins ................................................................. 36

Chapter 11 Mount Pad Dimensions .................................................. 37
Chapter 1 General Information

UPD60610/11 is a single port Ethernet physical layer device for 10Base-T100Base-TX and 100Base-FX operation.

This application note is complementary material to the following documents. Please read these documents for further information.

- Industrial Ethernet PHY - Single PHY ASSP User Manual
  R19UH0082EDxxxx
- Industrial Ethernet PHY - Programming Guide
  R19AN0010EDxxxx

Note:
xxxx – version number
Chapter 2  Strap Options

The Ethernet PHY ASSP provides the opportunity to set initial start-up configurations by external strap pin configuration. These strap options are read during power-up or hardware reset (resetb).

The strap pins are normal port pins that have only during the start-up phase the strap option functionality. The strap configuration is realized by a pull-up or pull-down resistance. Every strap pin has a default setting that is set by an internal 40kΩ resistance. To set an external strap-pin configuration a resistor of about 4kΩ should be used. In a noisy environment it is recommended to connect every strap-pin to an external pull-up/-down irrespective to its internal configuration.

An example of a schematic for two different strap-pin ports is shown in figure 2-1 with the related parts in table 2-1.

Table 2-2 is taken from the UM and lists all strap-pins and its functions.

Figure 2-1  Schematic example for pull-up and pull-down configuration at a strap pin

Note: The dashed box includes the MII related circuit parts. See also chapter 4.

<table>
<thead>
<tr>
<th>Part</th>
<th>Type</th>
<th>Characteristics</th>
<th>Recommended components</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1, R4</td>
<td>Resistor</td>
<td>10Ω</td>
<td></td>
</tr>
<tr>
<td>R2, R5</td>
<td>Resistor</td>
<td>~ 3.9kΩ</td>
<td></td>
</tr>
<tr>
<td>R3, R6</td>
<td>Internal resistance</td>
<td>~ 40kΩ</td>
<td></td>
</tr>
</tbody>
</table>
Table 2-2  Strap options

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Function</th>
<th>Default value</th>
</tr>
</thead>
</table>
| P0RXD3   | 0: Autoneg disabled, 100BaseT  
1: Autoneg enabled, 100BaseT                                              | 1, PU         |
| P0RXD2   | If Autoneg disabled:  
0: Half Duplex  
1: Full Duplex  
If Autoneg enabled:  
0: Parallel detect ends in half duplex mode  
1: Forced Full Duplex in parallel detect | 1, PU         |
| P0RXCLK  | 0: Disable Quick Autonegotiation  
If Autoneg enabled:  
1: Quick Autonegotiation, shortest times  
If Autoneg disabled  
1: Special Isolate. In this mode the PHYs will not set up a link unless programmed and enabled through the SMI. | 1, PU         |
| P0RXERR  | 0: Configure RMII Interface  
1: Configure MII Interface                                                   | 1, PU         |
| P0TXCLK  | 0: Standard Mode, “JK” required for Start of Frame detection  
1: Fast Mode, Only “J” required for Start of Frame detection. Do not use in RMII Mode. | 1, PU         |
| P0CRS    | 0: AUTOMDI-X disabled.  
1: AUTOMDI-X enabled                                                        | 1, PU         |
| P0RXDV   | 0: FX Mode for Phy0, in this case the values of Autoneg, Duplex, Quick Autoneg are ignored for this PHY.  
1: TX Mode for Phy0                                                          | 1, PU         |
| P0RXD0 / P0RXD1 | Configures the upper two bits N and M of the PHY addresses  
00: device uses address 00xxx for SMI  
01: device uses address 01xxx for SMI  
10: device uses address 10xxx for SMI  
11: device uses address 11xxx for SMI | 00, PD         |
Chapter 3  Media Dependent Interface

This PHY device supports two kinds of media interfaces:

- IEEE802.3 compliant twisted pair interface for 100Base-TX and 10Base-T operation.
- IEEE802.3 compliant optical media interface.

The start-up mode of the PHY can be set via strap pin configuration.

3.1 Differential Pair Routing

This chapter describes how to design the differential pairs between PHY and connector. Some general design rules for differential pair routing are given here. Furthermore some recommendations of the specific realization for the Ethernet PHY are described.

- Long wires should be avoided. The PHY, the transformer, and the connector should be placed together as close as possible.
- Crossing of differential traces with other lines and among each other should be avoided. The components should be placed that way that crossing of differential pairs of TxP/N and RxP/N is not necessary.
- Differential lines should be routed straight and as short as possible.
- Lines should bend with a 45 degree angle or less. (figure 3-1)
- Traces between PHY device, transformer and RJ45 connector should be designed with a differential impedance of 100Ω±10% and with an impedance of 50Ω related to GND.
- The traces of a differential pair should match in length. 0.5mm is the maximum deviation. Adjustments of the length should be done at the connector, device or transformer.
- Additional to the length the single traces should be designed symmetrical. They should be parallel and routed in the same layer with continuous width and a preferable fixed spacing. Components, vias and connections should also be symmetrical.
- Stubs should be avoided.
- Preferable is a large edge gap at differential pairs (‘g’ in figure 3-2). An empty space of five times of the trace width between differential pair and other signals, planes or components is recommended.
- Differential lines should not cross edges of the GND/supply plane, other planes or voids in the layer below. For continuous impedance a GND plane in the layer below is preferable.
- Beneath the magnetics no lines or planes should be routed.
- Preferable differential pairs should be routed via as little vias as possible. If vias are necessary please note the following:
- Vias of the related plane (e.g. AGND) should be placed near the signal vias. The distance between signal via and GND via should be equal to the distance between the layers to avoid a discontinuity of the impedance. (See ‘a’ in figure 3-3)

- Void and no planes between and around the signal vias (see figure 3-3). Metal of planes close to the differential vias could influence the impedance.

- The diameter of the vias should be almost equal to the trace width. (See ‘w’ in figure 3-3)
3.2 Twisted Pair Interface

Figure 3-4 and figure 3-5 show examples of twisted pair interface circuits with external and integrated magnetics. The following table 3-1 gives recommendations for values and parts. Additionally a layout example is given in figure 3-6 (Dimensions not true to scale).
Figure 3-4  Schematics for twisted pair interface circuit with external magnetics

Figure 3-5  Schematics for twisted pair interface circuit with integrated magnetics
Table 3-1 Part list – TX Interface

<table>
<thead>
<tr>
<th>Part</th>
<th>Type</th>
<th>Characteristics</th>
<th>Recommended components</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1, R2, R3, R4</td>
<td>Resistor</td>
<td>49.9Ω±1% 1/16W</td>
<td></td>
</tr>
<tr>
<td>R5, R6</td>
<td>Resistor</td>
<td>10Ω±1% 1/16W</td>
<td></td>
</tr>
<tr>
<td>R7, R8, R9, R10</td>
<td>Resistor</td>
<td>75Ω±1% 1/16W</td>
<td></td>
</tr>
<tr>
<td>C1</td>
<td>Capacitor</td>
<td>10nF – 100nF</td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td>Capacitor</td>
<td>10nF – 100nF</td>
<td></td>
</tr>
<tr>
<td>C3</td>
<td>Capacitor</td>
<td>10nF - 22nF</td>
<td></td>
</tr>
<tr>
<td>C4</td>
<td>Capacitor</td>
<td>10nF - 22nF</td>
<td></td>
</tr>
<tr>
<td>C5</td>
<td>Capacitor</td>
<td>4.7nF±10%</td>
<td></td>
</tr>
<tr>
<td>Transformer</td>
<td>One channel</td>
<td>Pulse Engineering H1012NL, H1102NL</td>
<td></td>
</tr>
<tr>
<td>RJ45 with integrated magnetics</td>
<td>One channel</td>
<td>Pulse Engineering J0011D21BNL</td>
<td></td>
</tr>
</tbody>
</table>

Notes:

- R1, R2, R3, R4, C1, C2 should be placed close to the PHY device
- R5, R6, C3, C4 should be placed close to the magnetics
- If an external transformer is used R8 and R10 should be placed next to the RJ45 connector
- The turns ratio of the transformer must be 1:1.
- The transformer should support AutoMDIX / MDIX if this function will be used by application
Figure 3-6  Example of twisted pair interface layout with external magnetics

PHY

R1 R2 R3 R4

C1 C2 C3 C4

R5 R6

R7 R8 R9 R10

C5

Magnetics

RJ45

P0 RXP

P0 T XP

PSTXN

PST XP

PHY, Magnetics and RJ45 in Top Layer

+: Top Layer Track

: Bottom Layer Track

: Contact in Top Layer

: Contact in Bottom Layer

: Via

: Component (Bottom)

: VIA to AGND

: FGND

: +3.3VA

: Conductor plane in Bottom Layer

R5
R7
R8
R9
R10
C5

+3.3VA

Conductor plane in Bottom Layer

+3.3VA

RJ45

PHY

Magnetics

Top Layer Track

Bottom Layer Track

Contact in Top Layer

Contact in Bottom Layer

Via

Component (Bottom)

Via to AGND

FGND
3.3 Optical Interface

Figure 3-7 shows an example schematic for a connection between an optical interface and the Ethernet PHY. Component details are shown in table 3-2 below.

Figure 3-7  Schematics for optical interface circuit

Table 3-2  Part list – optical interface

<table>
<thead>
<tr>
<th>Part</th>
<th>Type</th>
<th>Characteristics</th>
<th>Recommended components</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1, R2,</td>
<td>Resistor</td>
<td>51Ω±1%</td>
<td></td>
</tr>
<tr>
<td>R3, R4, R5</td>
<td>Resistor</td>
<td>130Ω±1%</td>
<td></td>
</tr>
<tr>
<td>R6, R7</td>
<td>Resistor</td>
<td>750Ω±1%</td>
<td></td>
</tr>
<tr>
<td>R8, R9, R10</td>
<td>Resistor</td>
<td>82Ω±1%</td>
<td></td>
</tr>
<tr>
<td>Optical Transceiver</td>
<td>One channel 1300nm</td>
<td>Avago Technologies AFBR-5803</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
- All resistors should be placed as close as possible to the optical transceiver.
3.4 Optical Signal Specification

The behaviour of the optical interfaces is described here.
The min and max values for these signals are shown in table 3-3.
The ranges for the optical signalling are dependent from the 3.3V supply voltage.
3.0V - 3.6V is the allowed range for this voltage supply. An example for the typical
3.3V is shown in figure 3-8.
The nominal 3.3 V is shown as VDD.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Voltage Low - VOL [V]</td>
<td>VDD - 1.81</td>
<td>VDD - 1.55</td>
</tr>
<tr>
<td>Output Voltage High - VOH [V]</td>
<td>VDD - 1.12</td>
<td>VDD - 0.88</td>
</tr>
</tbody>
</table>

Figure 3-8 Optical output signal for typical supply voltage

\[
VOL_{\text{min}} = VDD - 1.81 \text{V} \\
\text{typical VDD} = 3.3\text{V} \\
VOL_{\text{max}} = VDD - 1.55 \text{V} \\
VOH_{\text{max}} = VDD - 0.88 \text{V} \\
VOH_{\text{min}} = VDD - 1.12 \text{V} \\
VOL_{\text{min}} = VDD - 1.81 \text{V} \\
\]

2.42V
2.18V
1.75V
1.49V
3.5 Configurable Twisted Pair or Optical Interface

As described at the beginning of this chapter and in chapter 2 the PHY mode of the connected MDI interface should be set via strap pin configuration. Thus the PHY can be used in Twisted Pair or optical configuration – not both at the same time.

In some cases (e.g. for evaluation) it could be necessary to develop a board with the possibility to change the used medium of the Ethernet PHY. This chapter describes shortly how to arrange such a flexible board design. Please note that such a configuration is not an optimized design for differential pair routing and should be avoided if possible.

To create a flexible board design connection options for 0Ω resistors should be placed in the differential pair traces. An example circuit design is shown in figure 3-9. For the related operation mode the resistors R1-R4 (optical) or R5-R8 Twisted Pair) have to be soldered on the PCB. The unused traces must be open.

Figure 3-10 shows a layout example. It has to be considered that the splitting connections are placed very close to the device, as some of the following components in the twisted pair circuitry should also be very close at the PHY. To avoid crossing lines these connections should be vias to route both circuitry in different layers. To avoid large stubs the 0Ω resistors footprints should be closest to the via.

Figure 3-9 Schematic for parallel twisted pair and optical preparation

![Schematic for parallel twisted pair and optical preparation]
Figure 3-10  Layout Example parallel twisted pair and optical preparation

- **PHY**
  - Twisted Pair Circuitry
  - Optical Circuitry

**Top Layer Track**
- P0TXP
- P0TXN
- P0RXP
- P0RXN

**Bottom Layer Track**
- 0Ω Resistor (Bottom)*

**Via**
- Via to AGND

* only top or bottom resistors coexistent for final usage

Legend:
- Green: Top Layer Track
- Green: Bottom Layer Track
- 0Ω Resistor (Top)*
- 0Ω Resistor (Bottom)*
- Green: Via
- Green: Via to AGND
Chapter 4  MAC Interfaces – MII and RMII

The Ethernet PHY ASSP supports MII and RMII configuration to be connected to a MAC. Both modes need special hardware configuration and only one of these modes can exclusively operate at one time. The mode can be set via strap-pin configuration.

The tables below give an overview of all MII or RMII related pins. Table 4-1 shows all pins for MII/RMII and table 4-3 the two SMI pins for the PHY control.

In figure 4-1 and 4-2 example schematics for MII and RMII are given.

<table>
<thead>
<tr>
<th>Table 4-1</th>
<th>PHY ports: MII – RMII</th>
</tr>
</thead>
<tbody>
<tr>
<td>Port name</td>
<td>I/O</td>
</tr>
<tr>
<td>P0COL</td>
<td>O</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>P0TXD0</td>
<td>I</td>
</tr>
<tr>
<td>P0TXD1</td>
<td>I</td>
</tr>
<tr>
<td>P0TXD2</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>P0TXD3</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>P0TXERR</td>
<td>I</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>P0TXEN</td>
<td>I</td>
</tr>
<tr>
<td>P0TXCLK</td>
<td>O</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>P0RXD0</td>
<td>O</td>
</tr>
<tr>
<td>P0RXD1</td>
<td>O</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>P0RXD2</td>
<td>O</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>P0RXD3</td>
<td>O</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>P0RXDV</td>
<td>O</td>
</tr>
<tr>
<td>P0RXERR</td>
<td>O</td>
</tr>
<tr>
<td>P0RXCLK</td>
<td>O</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>P0CRS</td>
<td>O</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 4-2  SMI signals

<table>
<thead>
<tr>
<th>Port name</th>
<th>I/O</th>
<th>Pin</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>MDC</td>
<td>I</td>
<td>13</td>
<td>Data clock for PHY control</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Timing clock of MDIO</td>
</tr>
<tr>
<td>MDIO</td>
<td>I/O</td>
<td>14</td>
<td>Data I/O for PHY control</td>
</tr>
</tbody>
</table>

Figure 4.1 and 4.2 show schematics for an MII and an RMII interface. The direction of the signaling is shown with blue arrows. The component values are displayed in table 4-3 below.

Some layout recommendations are described by the following notes. For further information the documentation of the used MAC and standardization notes (IEEE) should be considered.

**General Notes:**

- The MDIO signal line should be connected to a 1.5kΩ resistor.
- 10Ω resistors at the outputs reduce reflections on the signal lines
- Some the MII/RMII ports provide a strap pin configuration. This additional wiring is described in chapter 2.
- The recommended impedance for all MII signal lines to GND is 50Ω±10%.
- The Data Signals (TXD3:0 and RXD3:0) and the related clock (TXCLK, RXCLK) are handled as bus communication lines. Thus the four data lines and the related clock line should match in length (deviation within 10mm). Also the other related signals (TXEN/RXDV, ERR) should have this length. Same length match is also important in RMII mode.
- All MII/RMII lines should be wired as short as possible.
- The signals should be routed in one layer, vias should be avoided
- Similar to all other signal lines the routing should be as straight as possible. Lines should bend with a 45 degree angle or less.
- For clock lines it can be useful to shield them by GND lines especially if longer traces are necessary.
### RMII Specific Notes:

- In RMII mode no clock is provided from the interface itself. Reference clock for the MAC is the same 50 MHz clock used for the whole PHY device (see also chapter 7).
- R26 is simply one example for a strap pin pull-down resistor. This one configures the PHY to RMII mode (see also chapter 2)
- Not used port pins can be used as additional GPIOs.
- If they are not used as GPIO please handle as follows:
  - Consider if there is needed a strap-pin option which needs a resistor
  - If a not used pin is programmed as input please pull it to GND
  - If a not used pin is programmed as output please leave it open
  - Best solution is to leave all unused pins open and program these GPIOs to an output function (e.g. 0x0011). If you need a strap resistance program the port as input (0x1111).
Figure 4-2  RMII interface

* R26 is just one example for a strap pull down. As this sets RMII configuration it is usual for this setup
** XCLK0 is the clock input of the PHY device – not part of the RMII interface

Table 4-3  Part list – MII and RMII interfaces

<table>
<thead>
<tr>
<th>Part</th>
<th>Type</th>
<th>Characteristics</th>
<th>Recommended components</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1, R18</td>
<td>Resistor</td>
<td>1.5kΩ</td>
<td></td>
</tr>
<tr>
<td>R2 – R17, R19 – R25</td>
<td>Resistor</td>
<td>10Ω</td>
<td></td>
</tr>
<tr>
<td>R26</td>
<td>Resistor</td>
<td>~ 3.9kΩ</td>
<td></td>
</tr>
</tbody>
</table>
Chapter 5  Power Supply

This chapter describes the power supply of the single channel PHY ASSP. It gives some important recommendations and shows examples for schematic and layout design. The PHY needs 3.3V and 1.5V power supplies. The 1.5V can be supplied via the system power supply or by internal voltage regulator. In this case the PHY can be supplied with 3.3V only.

Note:
In the following schematics of the power supply a lot of filtering components are used (Capacitors, ferrites, etc.). The given values of these parts are simply examples of running designs. The choice of these values depends on the quality of the supplied system power and the PCB design itself.

5.1 Power Supply Related Port Pins

Table 5-1 shows all power supply and GND pins of the PHY device. For the following explanations the pin names are used.

<table>
<thead>
<tr>
<th>Power Supply</th>
<th>Pins</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDIO</td>
<td>19, 31, 38</td>
<td>3.3V/2.5V IO power supply</td>
</tr>
<tr>
<td>VDD33ESD</td>
<td>10</td>
<td>3.3V input</td>
</tr>
<tr>
<td>P0AGND</td>
<td>5, 8</td>
<td>Analog GND for PHY</td>
</tr>
<tr>
<td>GNDIO</td>
<td>20, 36</td>
<td>GND for IO</td>
</tr>
<tr>
<td>VDD15</td>
<td>11</td>
<td>1.5V Digital VDD</td>
</tr>
<tr>
<td>GNDAPLL</td>
<td>48</td>
<td>Analog GND for PLL</td>
</tr>
<tr>
<td>VDDA15</td>
<td>9</td>
<td>Analog 1.5V power supply for PHY</td>
</tr>
<tr>
<td>VDDAPLL</td>
<td>47</td>
<td>Analog 1.5V power supply for PLL</td>
</tr>
<tr>
<td>VDDA33REG</td>
<td>46</td>
<td>3.3V power supply for voltage regulator</td>
</tr>
<tr>
<td>DVOUT15</td>
<td>37</td>
<td>Output voltage regulator for digital part</td>
</tr>
<tr>
<td>AVOUT15</td>
<td>45</td>
<td>Output voltage regulator for analog part</td>
</tr>
<tr>
<td>GNDAREF</td>
<td>43</td>
<td>Analog GND for PHY</td>
</tr>
<tr>
<td>REGOFF</td>
<td>44</td>
<td>Regulator disable:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hi: Regulator disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low: Regulator enabled</td>
</tr>
</tbody>
</table>
5.2 3.3 V Power Supply

A schematic for the 3.3 V Power supply is shown in figure 5-1. The related part list is shown in table 5-2.

Note:

- The capacitors C3, C4, C7, C8, C9 should be placed closest to the PHY. The other components could be arranged with some little space to the PHY.

![3.3V power supply](image)

Table 5-2 Part list – 3.3V power supply

<table>
<thead>
<tr>
<th>Part</th>
<th>Type</th>
<th>Characteristics</th>
<th>Recommended components</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1, C5</td>
<td>Capacitor</td>
<td>10uF±10%</td>
<td></td>
</tr>
<tr>
<td>C2, C3, C4, C6, C7, C8, C9</td>
<td>Capacitor</td>
<td>100nF±10%</td>
<td></td>
</tr>
<tr>
<td>L1</td>
<td>Ferrite Bead</td>
<td>120Ω @ 100MHz</td>
<td>Murata BLM21AG121SH1</td>
</tr>
</tbody>
</table>
5.3 1.5V Power Supply

As outlined above the PHY ASSP has an integrated voltage regulator to generate the needed 1.5V itself. Thus a 3.3V only operation is possible. The regulator is a linear regulator. This chapter describes the wiring of the 1.5V circuits for both cases: regulator operation and regulator disabled.

5.3.1 Regulator Operation – 1.5V Generation

A schematic for the 1.5 V Power supply is shown in figure 5-2. The related part list is shown in table 5-3.

Note:
- Similar to the 3.3V supply circuits the capacitors C11, C12, C13, C14, C15, C17 should be placed closest to the PHY and the other components could be arranged some centimetres away.
- REGOFF has to be connected to DGND via a pull-down resistor.

Figure 5-2 1.5V power supply with regulator usage
Table 5-3  Part list – 1.5V power supply

<table>
<thead>
<tr>
<th>Part</th>
<th>Type</th>
<th>Characteristics</th>
<th>Recommended components</th>
</tr>
</thead>
<tbody>
<tr>
<td>C10, C14</td>
<td>Capacitor</td>
<td>10uF±10%</td>
<td></td>
</tr>
<tr>
<td>C11, C12, C13, C15</td>
<td>Capacitor</td>
<td>100nF±10%</td>
<td></td>
</tr>
<tr>
<td>L2</td>
<td>Ferrite Bead</td>
<td>120Ω @ 100MHz</td>
<td>Murata BLM21AG121SH1</td>
</tr>
<tr>
<td>R1, R2(figure 5-4)</td>
<td>Resistor</td>
<td>~ 4.7kΩ</td>
<td></td>
</tr>
</tbody>
</table>

Figure 5-3 shows a layout example for the digital 1.5 V circuit.

Note:
- The connection between DVOUT15 and VDD15 should be short and low resistant. Best solution is a wide trace below the PHY device as shown in figure 5-3.
- The capacitor C14 should be placed close to DVOUT15, C15 close to VDD15
5.3.2 Regulator Disabled – External 1.5V Supply

The wiring for external 1.5V power supply is shown in figure 5-4. As the external parts are similar (except pull-up/down resistor) to the regulator wiring refer part list in table 5-3.

Notes:

- DVOUT15 should be connected to 1.5V power supply
- AVOUT15 should be left open
- Similar to the regulator usage C12, C13, C14 and C15 should be close to the PHY
- To disable the regulator REGOFF has to be connected to 3.3V via a pull-up resistor.

Figure 5-4  1.5V power supply without regulator usage
Chapter 6 Layout of Power Supply and GND Planes

This chapter gives some recommendations how to design supply and GND areas. Table 6-1 shows the three kinds of supply and GND and the related sections.

Table 6-1 Power supplies and GNDs

<table>
<thead>
<tr>
<th>Category</th>
<th>Name</th>
<th>Detail</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3V</td>
<td>3.3V</td>
<td>3.3V system power – board supply</td>
</tr>
<tr>
<td></td>
<td>3.3VD</td>
<td>+3.3V for digital</td>
</tr>
<tr>
<td></td>
<td>3.3VA</td>
<td>+3.3V for analog</td>
</tr>
<tr>
<td>1.5V (if supplied externally)</td>
<td>1.5V</td>
<td>1.5V system power – board supply</td>
</tr>
<tr>
<td></td>
<td>1.5VD</td>
<td>+1.5V for digital</td>
</tr>
<tr>
<td></td>
<td>1.5VA</td>
<td>+1.5V for analog</td>
</tr>
<tr>
<td>Ground</td>
<td>DGND</td>
<td>Digital Ground</td>
</tr>
<tr>
<td></td>
<td>AGND</td>
<td>Analog Ground</td>
</tr>
<tr>
<td></td>
<td>FGND</td>
<td>Frame Ground</td>
</tr>
</tbody>
</table>

6.1.1 3.3V supply

The 3.3V supply includes 3.3V board supply and the PHY related analogue and digital supplies 3.3VA and 3.3VD.

Note:

- These supplies should be connected at one point via a filter structure.

6.1.2 External 1.5V supply

External 1.5V supply is needed if the built-in regulator is not used.

Similar to the 3.3V supply the 1.5V includes a board supply and the PHY related analogue and digital supplies 1.5VA and 1.5VD.

Note:

- These supplies should be connected at one point via a filter structure.
6.1.3 GNDs

For a PHY board three separated GNDs are recommended: Digital ground (DGND), analogue ground (AGND) and frame ground (FGND).

Notes:
- DGND and AGND should be connected at one point via a 0Ω resistor.
- The components connected to DGND and AGND should be placed beneath or above the related GND plane.
- The FGND should surround the PCB at its edge.
- The FGND should be at the top and the bottom layer of the PCB.
- The FGND should also be connected to the other GNDs. This can be done via low impedance path or any special circuit, e.g. ESD protection.
- The FGND can be connected to chassis grounding.
- Ground wires and areas especially at shields or close to differential pairs should have enough vias to the GND plane (e.g. every 5-10mm).

6.1.4 Layout example

Figure 6.1 – 6.4 show a layout example for a four layer PCB. This layout is an idealized and simplified illustration.

![Power and GND layout – Layer 1](image-url)
Figure 6-2  Power and GND layout – Layer 2

Figure 6-3  Power and GND layout – Layer 3
Figure 6-4  Power and GND layout – Layer 4
Chapter 7  External Reference Clock

7.1 Reference Clock

For operation of the Ethernet PHY ASSP an external clock is needed. For MII operation a 25MHz clock has to be applied to the PHY device. For RMII operation the frequency of the clock has to be 50MHz.

The external clock can be provided by a quartz crystal or any other oscillator.

In case of 50MHz usage for RMII configuration an oscillator should be used because the signal is also used as clock for data transfer (see chapter 4).

The requirements of an oscillator that can be used are shown in table 7-1.

<table>
<thead>
<tr>
<th>Item</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference Clock frequency</td>
<td></td>
<td>25</td>
<td></td>
<td>MHz</td>
<td>For MII mode</td>
</tr>
<tr>
<td>Allowed error margin</td>
<td>-100</td>
<td>50</td>
<td>100</td>
<td>ppm</td>
<td></td>
</tr>
<tr>
<td>Duty cycle</td>
<td></td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>%</td>
</tr>
<tr>
<td>Allowed Jitter</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RMS value</td>
</tr>
</tbody>
</table>

7.2 Circuit and layout for clock input

As described different clock sources are possible.

Two examples for schematic and layout are given here. Figure 7-1 shows a schematic and layout example for a quartz crystal use. Similar examples for an oscillator are shown in figure 7-2.

General notes:

- The clock supply circuit should be placed near to the clock input pins (XCLK0, XCLK1).
- The clock supply circuit should be separated from other signal and communication lines.
- Preferable the clock supply circuit is surrounded with DGND.
- The used devices for the external clock may have their own design recommendations. They should also be considered.
Figure 7-1  Schematic and layout example for quartz crystal usage

Notes related to quartz crystal usage:

- A quartz crystal has to be connected to XCLK0 and XCLK1.
- C1 and C2 are load capacitors for the quartz crystal. For the capacity values of C1 and C2 the data sheet of the used quartz should be considered.
- It is preferable to shield the clock signals with a surrounding DGND plane as shown in the layout Example.
- As mentioned before a quartz crystal is applicable for 25MHz only.
Notes related to oscillator usage:

- If the clock is applied by an oscillator this has to be connected to XCLK0.
- XCLK1 port should be open and not connected to anything.
- R1 is a damping resistance. Its value depends on the used oscillator.
- C3 is a decoupling capacitor. For its value the oscillator data sheet should be considered.
- It is preferable to shield the oscillator and the signal with a surrounding DGND plane as shown in the layout Example.
Chapter 8  LED Control

The single channel PHY provides by default configuration an LED output signal for link indication. The PHY can output four different LED signals. The LED signals can be configured to represent a lot of different statuses. Every GPIO pin can be configured to output one of these LED signals.

A LED output can be configured to display one static signal or to display two signals in a multiplexing (LED-MUX) mode. For a detailed description please refer the UM.

The schematic in figure 8-1 shows the wiring for a standard static LED. In contrast to all other GPIOs signals the LEDs are active low. Thus a LED has to be connected between 3.3V and LED output.

Figure 8-1  Circuit for standard LED operation

In the optional LED-MUX mode it is possible due to switched signals to control 2 LEDs via one output pin. The output is also reversed (low active). A wiring for two LEDs for LED-MUX a schematic is shown in figure 8-2.
Figure 8-2 Circuit for LED-MUX operation

Notes:
- No component recommendations are given because their values interdepend. The strength of the used output port should also be considered (refer UM).
- To avoid a light glinting of the LEDs the two standard diodes are recommended.
Chapter 9          EXTRES

The EXTRES port defines the bias current of the PHY. It should be connected to DGND via 12.4kΩ as shown in figure 9-1.

Notes:
- The 12.4kΩ resistor should be placed near the PHY.
- It is recommended to use a 12.4kΩ resistance with maximum 1% range and 1/16W.
- Do not compose the 12.4kΩ resistance from two resistors (e.g. 12kΩ and 390Ω).

Figure 9-1          Wiring of EXTRES
Chapter 10  Unused pins

Table 10-1 shows the unused ports of the Single Channel PHY ASSP and gives a recommendation how to terminate them in a design.

Table 10-1  Unused port pins

<table>
<thead>
<tr>
<th>Port name</th>
<th>Pin</th>
<th>Termination</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEST</td>
<td>41</td>
<td>pull-down with ~4.7kΩ</td>
</tr>
<tr>
<td>ATP</td>
<td>2</td>
<td>pull-down with ~4.7kΩ</td>
</tr>
</tbody>
</table>
Chapter 11  Mount Pad Dimensions

Figure 11-1 and table 11-1 shows the recommended dimensions for the mount pads for the PHY ASSP. The related device dimensions are shown in table 11-2. For complete device dimensions refer the UM.

Table 11-1  Mount Pad Dimensions

<table>
<thead>
<tr>
<th>Variable</th>
<th>Value in mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\alpha$</td>
<td>0.10 – 0.30</td>
</tr>
<tr>
<td>$\beta_1$</td>
<td>0.20 – 0.40</td>
</tr>
<tr>
<td>$\beta_2$</td>
<td>0.20 – 0.40</td>
</tr>
<tr>
<td>$\gamma$</td>
<td>0.25</td>
</tr>
</tbody>
</table>

Table 11-2  Related Device Dimensions

<table>
<thead>
<tr>
<th>Variable</th>
<th>Value in mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L$</td>
<td>0.50</td>
</tr>
<tr>
<td>$e'$</td>
<td>0.50</td>
</tr>
<tr>
<td>$b$</td>
<td>0.2 + 0.07  - 0.03</td>
</tr>
</tbody>
</table>
## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>December 17, 2012</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>March 19, 2013</td>
<td>Minor changes</td>
</tr>
<tr>
<td>1.2</td>
<td>July 1, 2013</td>
<td>Optical Transceiver specs changed, other minor changes</td>
</tr>
</tbody>
</table>
General Precautions in the Handling of ASSP Products

The following usage notes are applicable to all ASSP products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of ASSP products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.

   The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.

   The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   The characteristics of ASSP in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.
Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.

2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.

4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the functionality, reliability, and safety of any such circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.

5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.

6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.

7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics.

The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

- **“Standard”**: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

- **“High Quality”**: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

- **“Specific”**: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.

8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.

9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for
hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.

10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.
Refer to "http://www.renesas.com/" for the latest and detailed information.

**Renesas Electronics America Inc.**
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

**Renesas Electronics Canada Limited**
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

**Renesas Electronics Europe Limited**
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

**Renesas Electronics Europe GmbH**
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / 7898

**Renesas Electronics Hong Kong Limited**
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

**Renesas Electronics Taiwan Co., Ltd.**
7F, No. 363 Fu Shing North Road Taipei, Taiwan, R.O.C.
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

**Renesas Electronics Singapore Pte. Ltd.**
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

**Renesas Electronics Malaysia Sdn.Bhd.**
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

**Renesas Electronics Korea Co., Ltd.**
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141