IGBT

Wafer Testing in Chip Shipment

Introduction

This application note explains the need for and how to perform wafer testing during wafer level, chip level shipment.

Target Device

IGBT wafer products

Contents

1. Gap between wafer testing and module testing

As widely known, there is a big gap between the test current at wafer level and the test current at module level.

On the other hand, multiple IGBT chips are mounted on one module. It is important for improving the module quality that the IGBT wafer testing level is close to the module testing level.

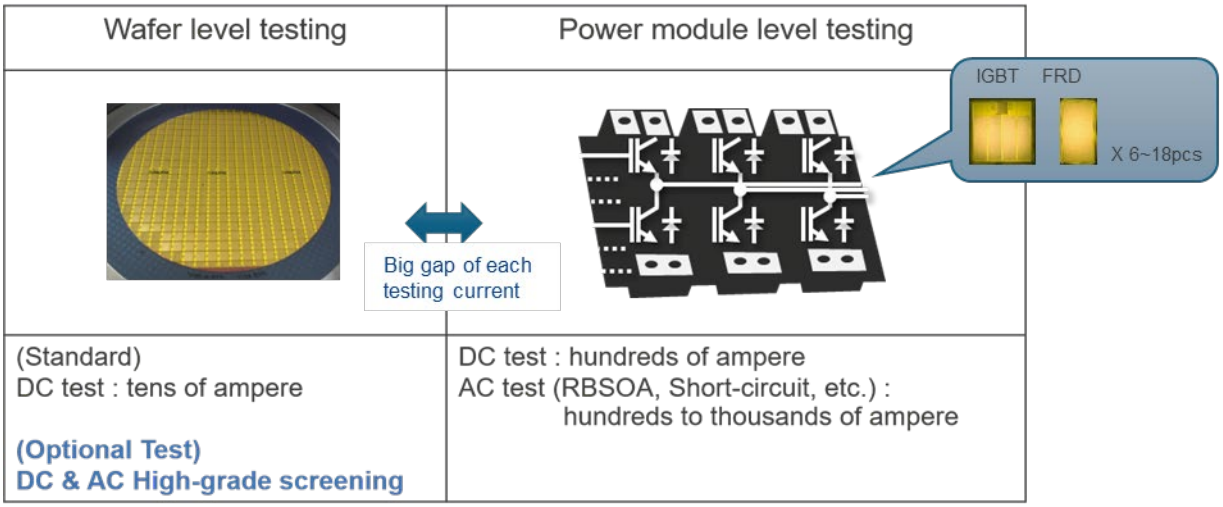

Figure 1-1 Gap of each testing current between at Wafer and Module 1

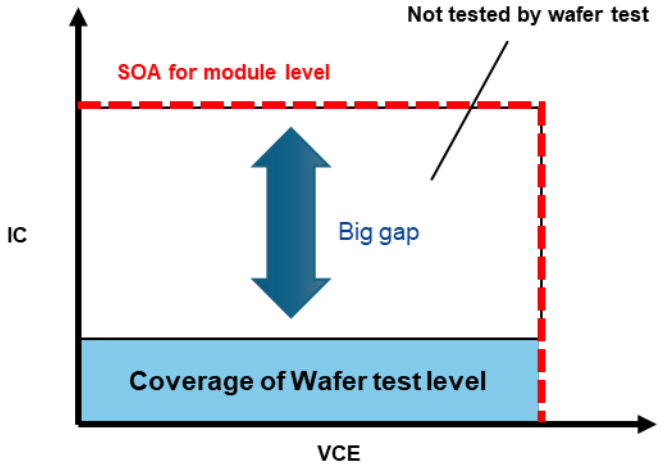

Figure 1-2 Gap of each testing current between at Wafer and Module 2

2. General IGBT failure modes and Test specifications

The major failure modes of IGBT are gate failure and SOA destruction due to current concentration in abnormal cell area.

High-level screenings help earlier-phase failure detection and contributes on yield saving in the following test at Module / Inverter manufacture.

Table 2-1 General IGBT failure modes

Failure mode	Test		Purpose
Gate Failure Mode (short)	DC	Screening by application of high electric field	Detect oxide film abnormality
SOA Failure mode	AC	Applied high current and voltage by switching test	Detects transient current concentration and breakdown failure at dynamic operation *
Over temperature due to abnormality assembly	DC	Thermal resistance test	Detect die bonding abnormality

Coverage of the screening

*Note. There are defects that are NOT detectable in static measurement only but can dynamically lead to failures. This test can help to screen such an inherent defect factor in module screen test.

3. Gate Failure Mode

3.1 Gate screening

Gate screening is applied more higher voltage (electric field) than normal operating voltage to Gate, It is the method to reduce defects incidence of initial failure and useful life due to particle and defects by applying stress accelerated than the actual use environment.

It shows the estimated graph of cumulative failure rate after gate screening in the figure below. Optimal screening conditions are set so that failure rate is 0.1% or less in the operation of 20 years.

And all IGBT chips is screening in this condition.

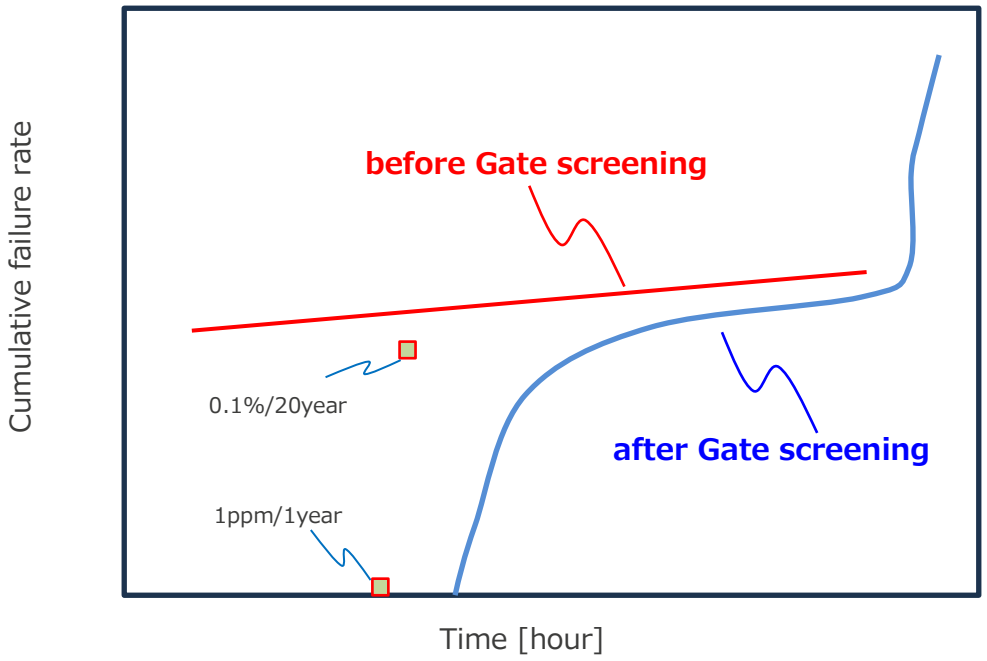

Figure 3-1 Failure rate before and after gate screening

(by the Weibull distribution of TDDB * evaluation)

* TDDB : Time Dependent Dielectric Breakdown

4. SOA Failure Mode

4.1 L-load (AC) screening effect

In case of X chips in module, X times of die-level screening rate should be reflected on yield saving in module test. Early phase screening should work for total cost saving.

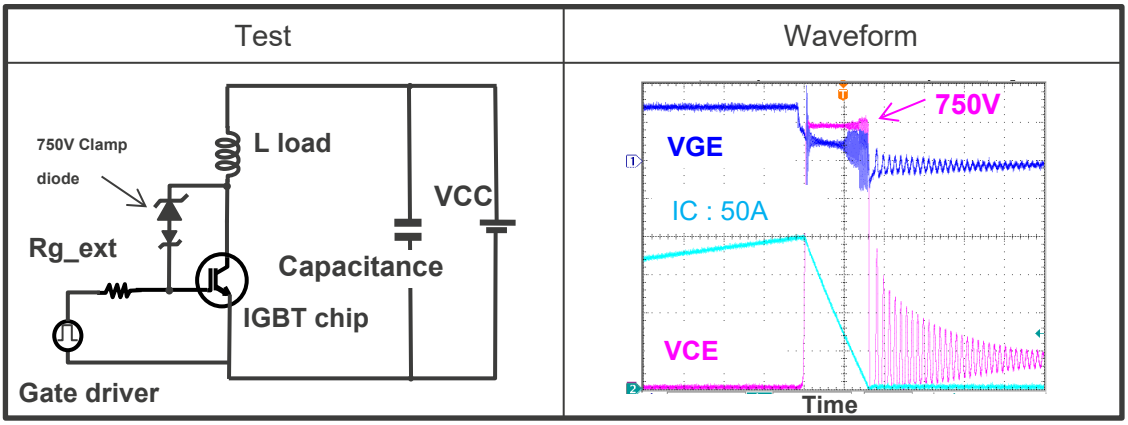

Figure 4-1 Wafer AC Test Circuit

Test condition: Clamped_VCE=750V, IC=50A, VGE=15 -> 0V, Tj=25degC

L load test is performed to reject defective chips with SOA failure (latch-up failure). Figure 4-1 shows an example of L-load screening. In this example waveform, VCE is clamped at the maximum rated voltage because IGBTs can't stand avalanche.

In the front-end process, unavoidable defect rerated to AC failure could be inherent, and it can lead to parasitic NPN-Bipolar Transistor turn-on (Latch-up) at switching off timing. To reject such potential failure die, L-load screening test at wafer level is effective.

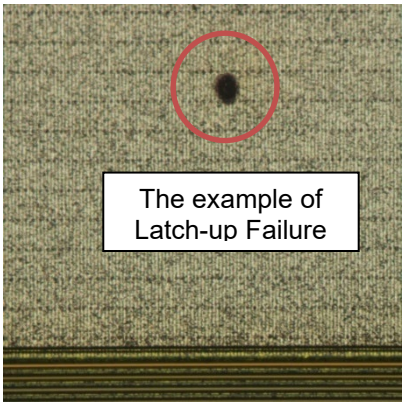

Figure 4-2 Representative failure mode

5. Example of Test Flow

Testing in bare die shipping can take many forms. The following tests are commonly considered, as well as special practices such as high temperatures test in high quality grade products.

It is important to understand that the form of testing will vary for each individual product.

5.1 Wafer level test and optional

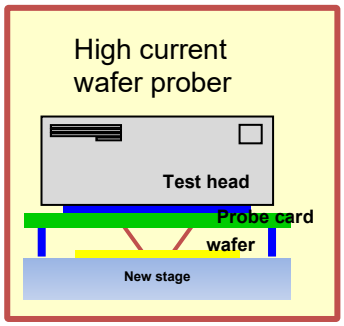

Figure 5-1

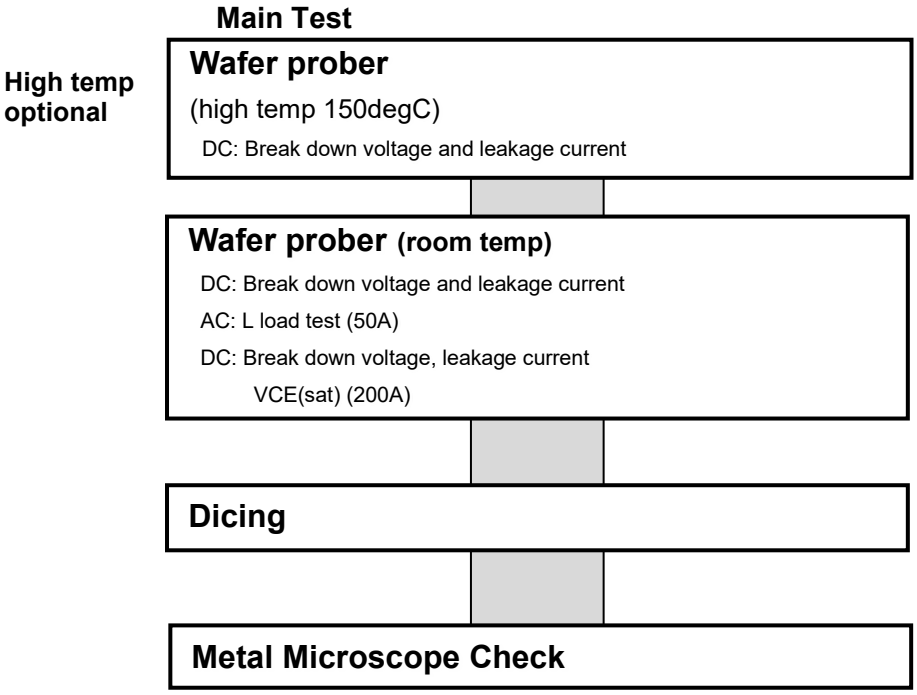

Figure 5-2

5.2 Single bare die test and optional

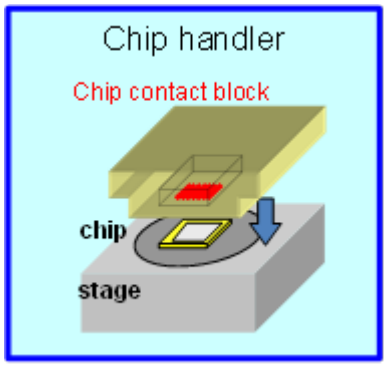

Figure 5-3

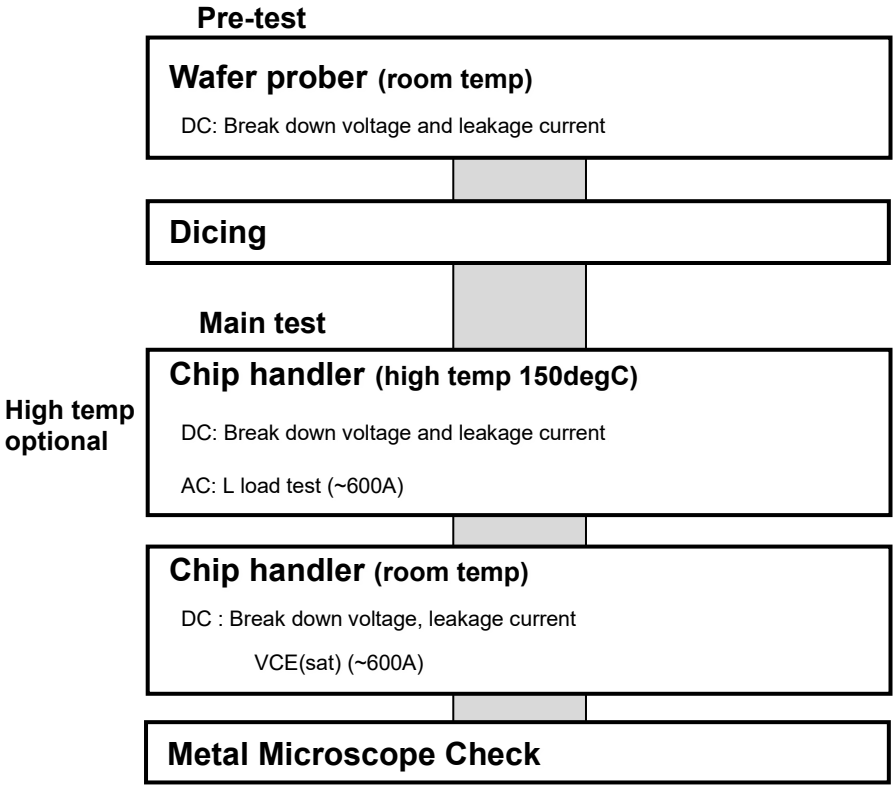

Figure 5-4

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Aug.21.24	-	First edition

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