1. Abstract

This document describes the slave transmit/receive processes in I²C-bus interface slave communication using the R32C/100 Series serial interface (UART2) special mode 1 (I²C mode).

Seven channels (UART0 to UART6) can be used in special mode 1 in the R32C/118 Group. If channels other than UART0 to UART6 are used, refer to the hardware user's manual and modify the registers associated with UARTi (i = 0 to 6).

2. Introduction

The application example described in this document applies to the following microcomputer (MCU) and parameter:

- MCU: R32C/118 Group
- XIN Clock: 16 MHz

This application note can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the above group. Check the user’s manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. Application Example

3.1 Program Outline

I2C-bus interface slave communication (slave transmission/reception) using UART2 special mode 1 is processed in the application example. A maximum of 255 bytes of data can be transmitted/received.

The transmission and reception procedures conform to the I2C-bus communication protocol when used under the following conditions:

- Slave address: 7 bits
- Standard-mode and Fast-mode are supported
- Communication data length: 1 to 255 bytes (not including the slave address)
- Restart condition is not supported

Figure 3.1 shows the Communication Format, Figure 3.2 shows the Block Diagram, Figure 3.3 shows the Outline Flowchart, and Figure 3.4 to Figure 3.6 show Timing Diagrams.
**Figure 3.3 Outline Flowchart**

- **Start**
- **Initial setting**
- **(2) UART2 receive interrupt**
- **(3) UART2 transmit interrupt**
- **(4) Stop condition detection interrupt**
The numbers in Figure 3.3 correspond to the numbers indicated in the program processing in the operating timing charts in Figure 3.4 to Figure 3.6.

(1) Initial setting
   Initialize the system clock, UART2 associated SFRs, and variables used.

(2) UART2 receive interrupt
   When a slave address is received, a UART2 receive interrupt is generated at the falling edge of the eighth bit of the SCL clock. The slave address is determined after reading the U2RB register.
   When the slave address is matched:
   • Generate an ACK and set the SCL2 pin to low hold at the ninth bit.
   • Enable the stop condition detection interrupt and UART2 transmit interrupt. Disable the UART2 receive interrupt.
   • Set transmit/receive data to the U2TB register. (1)
   When the slave address is not matched:
   • Generate a NACK.
   After the above processing, release the SCL2 pin low hold at the eighth bit.

(3) UART2 transmit interrupt
   A UART2 transmit interrupt is generated at the falling edge of the ninth bit of the SCL clock. When the first byte (slave address) is received, ACK output set in the UART2 receive interrupt handling is released. When transmitting, determine the ACK/NACK and set the next byte transmit data. When receiving, store the receive data and set ACK for the next byte.

(4) Stop condition detection interrupt
   When a stop condition is detected, an interrupt is generated. SFR values which changed in mid-communication are returned to their initial settings. Disable the stop condition detection interrupt and UART2 transmit interrupt. Enable the UART2 receive interrupt.

Note:
1. When the TXEPT bit in the UiC0 register is 0 (data in the transmit register) in slave mode, write data to the UiTB register.
   If no data exists in the transmit buffer register, the TXEPT bit becomes 1 at the rising edge of the ninth bit of the SCL1 clock.
   The following procedure should be met the condition above.
   • When receiving the first byte (slave address):
     (1) Set the second byte data to the UiTB register in the receive interrupt.
     (2) Set the third byte data to the UiTB register in the transmit interrupt.
   • After the first byte, set fourth or later byte data every transmit interrupt is requested.
I²C-bus Interface Using UART2 Special Mode 1
(Slave Transmit/Receive)

Figure 3.4 Slave Receive Timing
Figure 3.5  Slave Transmit Timing (1)

Figure 3.6  Slave Transmit Timing (2)
### 3.1.1 Peripheral Functions

Serial interface (UART2) special mode 1 (I²C mode) is used under the following setting conditions:

- I²C mode is used.
- Transfer clock is external clock.
- f1 is used as U2BRG count source.
- SDA2 and SCL2 pins are N-channel open drain output.
- Transfer format is MSB first.
- Transmission completed (TXEPT is 1) is selected as the UART2 transmit interrupt source.
- Clock phase setting is clock delay.
- Seven to eight cycles of the U2BRG count source is selected as SDA2 digital delay value.
- UART2 auto initialize function is used.
- SCL2 wait auto insert function is used.
- SCL2 wait output function 2 is not used.
- SCL2 wait auto insert function 3 is used.
- SDA2 output stop function is used.
- Start condition detection interrupt is not used.
- Stop condition detection interrupt is used.
- UART2 transmit interrupt is used.
- UART2 receive interrupt is used.
- PLL clock is 100 MHz.
- Base clock is 50 MHz.
- CPU clock is 50 MHz.
- Peripheral bus clock is 25 MHz.
- Peripheral clock source is 25 MHz.

### Table 3.1 Pins Used and Their Function

<table>
<thead>
<tr>
<th>Pin</th>
<th>I/O</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>P7_1/SCL2</td>
<td>I/O</td>
<td>I²C mode clock I/O pin</td>
</tr>
<tr>
<td>P7_0/SDA2</td>
<td>I/O</td>
<td>I²C mode data I/O pin</td>
</tr>
</tbody>
</table>

### 3.1.2 Notes on Using the Attached Sample Program

Note the following when using the program included with this application note:

1. Do not use multiple interrupts.
2. The size of the receive buffer and the transmit buffer are set to 255 bytes. The buffer size is defined by the BUFSIZE macro (1 to 255 bytes). When the number of transmit/receive bytes exceeds the size of the buffer, the slave disregards the communication. Disable the UART2 transmit interrupt, and release pins SCL2 and SDA2.
3. After the master generates a stop condition, when the slave processing time \(^{(1)}\) has passed, start the next transmit/receive operation (start condition is generated/generate a start condition).

Note:

1. The slave processing time indicates the time between detecting a stop condition and enabling I²C mode in the main processing, and is dependent on the processing of the user program. The maximum processing time for this sample program is approximately 100 μs.
3.2 Memory

Table 3.2 Memory

<table>
<thead>
<tr>
<th>Memory</th>
<th>Size</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROM</td>
<td>657 bytes</td>
<td>In the iic.c module</td>
</tr>
<tr>
<td>RAM</td>
<td>6 bytes</td>
<td>In the iic.c module</td>
</tr>
<tr>
<td>Maximum user stack</td>
<td>28 bytes</td>
<td></td>
</tr>
<tr>
<td>Maximum interrupt stack</td>
<td>64 bytes</td>
<td></td>
</tr>
</tbody>
</table>

Usage memory size varies depending on C compiler version and compile options. The above applies under the following conditions:
C compiler: R32C/100 Series C Compiler V.1.02 Release 01
C compile option: -c -finfo -dir "$(CONFIGDIR)"
4. Software

This chapter shows the program example to set the example described in chapter 3. Application Example. Refer to the latest hardware user’s manual for details on individual registers.

4.1 Variables

Definition file name: rej05b1396_src.c

<table>
<thead>
<tr>
<th>Variable Name</th>
<th>Size</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char iic_tx[BUFSIZE]</td>
<td>255 bytes</td>
<td>Transmit buffer</td>
</tr>
<tr>
<td>unsigned char iic_rx[BUFSIZE]</td>
<td>255 bytes</td>
<td>Receive buffer</td>
</tr>
<tr>
<td>unsigned char rcv_data[BUFSIZE]</td>
<td>255 bytes</td>
<td>Store receive data read from receive buffer</td>
</tr>
</tbody>
</table>

Definition file name: iic.c

<table>
<thead>
<tr>
<th>Variable Name</th>
<th>Size /Bit Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>static byte_dt iic_str</td>
<td>-</td>
<td>Structure to store statuses</td>
</tr>
<tr>
<td>iic_status</td>
<td>1 byte</td>
<td>All statuses</td>
</tr>
<tr>
<td>iic_rw</td>
<td>b0</td>
<td>R/W flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Write (W) slave receive</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Read (R) slave transmit</td>
</tr>
<tr>
<td>iic_buf_full</td>
<td>b1</td>
<td>Buffer full flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Within buffer size (transmit/receive bytes &lt; buffer size)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Buffer full (transmit/receive bytes ≥ buffer size)</td>
</tr>
<tr>
<td>iic_end</td>
<td>b2</td>
<td>Communication completed flag</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Busy (mid-communication)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Ready (except for mid-communication)</td>
</tr>
<tr>
<td></td>
<td>b7 to b3</td>
<td>Not used (undefined)</td>
</tr>
<tr>
<td>static unsigned char far* iic_pointer</td>
<td>4 bytes</td>
<td>Transmit/receive buffer pointer</td>
</tr>
<tr>
<td>static unsigned char iic_index</td>
<td>1 byte</td>
<td>Number of transmit/receive bytes</td>
</tr>
</tbody>
</table>
## 4.2 Function Tables

<table>
<thead>
<tr>
<th>Declaration</th>
<th>void main(void)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outline</td>
<td>Main processing</td>
</tr>
<tr>
<td>Argument</td>
<td>Argument name</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Variable (global)</td>
<td>Variable name</td>
</tr>
<tr>
<td></td>
<td>unsigned char iic_tx[BUFSIZE]</td>
</tr>
<tr>
<td></td>
<td>unsigned char iic_rx[BUFSIZE]</td>
</tr>
<tr>
<td></td>
<td>unsigned char rcv_data[BUFSIZE]</td>
</tr>
<tr>
<td>Returned value</td>
<td>Type</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Function</td>
<td>After setting the system clock, I2C mode is enabled. Communication status is determined by the returned value of the iic_slave_end function. Each status is processed after communication is completed, and the uart2_init function is called to enable I2C mode.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Declaration</th>
<th>void SetPLLClock(void)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outline</td>
<td>PLL mode setting</td>
</tr>
<tr>
<td>Argument</td>
<td>Argument name</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Variable (global)</td>
<td>Variable name</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Returned value</td>
<td>Type</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Function</td>
<td>Call this function from the main processing. This is the process for PLL mode transmission. Set peripheral clock source to 25 MHz.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Declaration</th>
<th>void uart2_init(unsigned char ini)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Outline</td>
<td>UART2 initial setting</td>
</tr>
<tr>
<td>Argument</td>
<td>Argument name</td>
</tr>
<tr>
<td></td>
<td>unsigned char ini</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>Variable (global)</td>
<td>Variable name</td>
</tr>
<tr>
<td></td>
<td>(structure member) iic_status</td>
</tr>
<tr>
<td>Returned value</td>
<td>Type</td>
</tr>
<tr>
<td></td>
<td>None</td>
</tr>
<tr>
<td>Function</td>
<td>Call this function from the main processing. Initialize SFRs to use UART2 special mode 1 (I2C mode). When I2C mode is enabled, set iic_status to 0x00 (clear all statuses). When executing this function, interrupts are disabled by the I flag.</td>
</tr>
</tbody>
</table>
I2C-bus Interface Using UART2 Special Mode 1  
(Slave Transmit/Receive)

#### Declaration

<table>
<thead>
<tr>
<th>void _stop_condition_detection(void)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Outline</strong> Stop condition detection interrupt handling</td>
</tr>
<tr>
<td><strong>Argument</strong></td>
</tr>
<tr>
<td>Argument name</td>
</tr>
<tr>
<td>None</td>
</tr>
<tr>
<td><strong>Variable (global)</strong></td>
</tr>
<tr>
<td>Variable name</td>
</tr>
<tr>
<td>None</td>
</tr>
<tr>
<td><strong>Returned value</strong></td>
</tr>
<tr>
<td>Type</td>
</tr>
<tr>
<td>None</td>
</tr>
<tr>
<td><strong>Function</strong></td>
</tr>
<tr>
<td>An interrupt is generated when a stop condition is detected, and the stp_int function is called.</td>
</tr>
</tbody>
</table>

#### Declaration

<table>
<thead>
<tr>
<th>static void stp_init(void)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Outline</strong> Stop condition detection processing</td>
</tr>
<tr>
<td><strong>Argument</strong></td>
</tr>
<tr>
<td>Argument name</td>
</tr>
<tr>
<td>None</td>
</tr>
<tr>
<td><strong>Variable (global)</strong></td>
</tr>
<tr>
<td>Variable name</td>
</tr>
<tr>
<td>(structure member) iic_end</td>
</tr>
<tr>
<td><strong>Returned value</strong></td>
</tr>
<tr>
<td>Type</td>
</tr>
<tr>
<td>None</td>
</tr>
<tr>
<td><strong>Function</strong></td>
</tr>
<tr>
<td>Called from the stop condition detection interrupt handling. UART2 associated SFR values changed mid-communication are returned to their initial values, and the communication completed flag is set to 1.</td>
</tr>
</tbody>
</table>

#### Declaration

<table>
<thead>
<tr>
<th>void_uart2_receive(void)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Outline</strong> UART2 receive interrupt handling</td>
</tr>
<tr>
<td><strong>Argument</strong></td>
</tr>
<tr>
<td>Argument name</td>
</tr>
<tr>
<td>None</td>
</tr>
<tr>
<td><strong>Variable (global)</strong></td>
</tr>
<tr>
<td>Variable name</td>
</tr>
<tr>
<td>unsigned char far* iic_pointer</td>
</tr>
<tr>
<td>unsigned char iic_index</td>
</tr>
<tr>
<td>(structure member) iic_status</td>
</tr>
<tr>
<td>(structure member) iic_rw</td>
</tr>
<tr>
<td><strong>Returned value</strong></td>
</tr>
<tr>
<td>Type</td>
</tr>
<tr>
<td>None</td>
</tr>
<tr>
<td><strong>Functions</strong></td>
</tr>
<tr>
<td>An interrupt is generated at the falling edge of the eighth bit of the SCL clock. This function calls the iic_id_check function after reading the U2RB register in the function header.</td>
</tr>
<tr>
<td>• When the slave address is matched, generate an ACK, and set the SCL2 pin to low hold at the ninth bit. The receive interrupt is disabled, and the transmit interrupt and stop condition detection interrupt are enabled. The number of transmit/receive bytes and all statuses are cleared. When the slave is receiving, set the ACK for the next byte. When the slave is transmitting, set transmit data for the next byte.</td>
</tr>
<tr>
<td>• When the slave address is not matched, generate a NACK. After the above processing, release the SCL2 pin low hold.</td>
</tr>
</tbody>
</table>
### I2C-bus Interface Using UART2 Special Mode 1 (Slave Transmit/Receive)

#### Declaration

```c
unsigned char* iic_id_check(unsigned char id, unsigned char rw)
```

#### Outline

Slave address determine processing

#### Argument

<table>
<thead>
<tr>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char id</td>
<td>Received slave address</td>
</tr>
<tr>
<td>unsigned char rw</td>
<td>R/W flag</td>
</tr>
</tbody>
</table>

#### Variable (global)

<table>
<thead>
<tr>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
</tr>
</tbody>
</table>

#### Returned value

<table>
<thead>
<tr>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char*</td>
<td>iic_rx</td>
<td>Receive buffer address</td>
</tr>
<tr>
<td>NULL</td>
<td>NULL</td>
<td>Slave address does not match</td>
</tr>
</tbody>
</table>

#### Function

Called from the UART2 receive interrupt handling. The received slave address is determined. When the slave address is matched, the returned value is the buffer address. When the slave address is not matched, the returned value is NULL.

---

#### Declaration

```c
void _uart2_trans(void)
```

#### Outline

UART2 transmit interrupt handling

#### Argument

<table>
<thead>
<tr>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
</tr>
</tbody>
</table>

#### Variable (global)

<table>
<thead>
<tr>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char iic_index</td>
<td>Number of transmit/receive bytes</td>
</tr>
<tr>
<td>(structure member) iic_rw</td>
<td>R/W flag</td>
</tr>
</tbody>
</table>

#### Returned value

<table>
<thead>
<tr>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

#### Function

An interrupt is generated at the falling edge of the ninth bit of the SCL clock. The U2RB register is read in the function header. When the first byte (slave address) is received, disable ACK output set by the receive interrupt handler. After the first byte is received, the slave_rcv_int function is called when the slave is receiving and the slave_trn_int function is called when the slave is transmitting.

---

#### Declaration

```c
static void slave_rcv_int(unsigned char rb_data)
```

#### Outline

Slave receive processing

#### Argument

<table>
<thead>
<tr>
<th>Argument name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char rb_data</td>
<td>Receive data from the U2RB register</td>
</tr>
</tbody>
</table>

#### Variable (global)

<table>
<thead>
<tr>
<th>Variable name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char iic_index</td>
<td>Number of transmit/receive bytes</td>
</tr>
<tr>
<td>unsigned char far* iic_pointer</td>
<td>Transmit/receive buffer pointer</td>
</tr>
<tr>
<td>(structure member) iic_buf_full</td>
<td>Buffer full flag</td>
</tr>
</tbody>
</table>

#### Returned value

<table>
<thead>
<tr>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

#### Function

Called from the UART2 transmit interrupt handling. The argument value is stored in the receive buffer (except the slave address).
- When the number of received bytes is less than the buffer size, set an ACK for the next byte. Release the SCL2 pin low hold, then enable the SCL2 pin to low hold for the next byte.
- When the number of received bytes is the same as or greater than the buffer size, the buffer full flag is set to 1. Release pins SCL2 and SDA2, and disable the UART2 transmit interrupt.
### Declaration

static void slave_trn_int(unsigned char rb_data)

### Outline

Slave transmit processing

### Argument

<table>
<thead>
<tr>
<th>Name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char rb_data</td>
<td>ACK/NACK read from the U2RB register</td>
</tr>
</tbody>
</table>

### Variable (global)

<table>
<thead>
<tr>
<th>Name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned char iic_index</td>
<td>Number of transmit/receive bytes</td>
</tr>
<tr>
<td>unsigned char far* iic_pointer</td>
<td>Transmit/receive buffer pointer</td>
</tr>
<tr>
<td>(structure member) iic_buf_full</td>
<td>Buffer full flag</td>
</tr>
</tbody>
</table>

### Returned value

<table>
<thead>
<tr>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

### Function

Called from the UART2 transmit interrupt handling.

- When an ACK is detected and the number of transmit bytes is less than the buffer size, set transmit data for the next byte. Release the SCL2 pin low hold, then enable the SCL2 pin to low hold for the next byte.
- When the number of transmit bytes is the same as or greater than the buffer size, set the buffer full flag to 1. Release pins SCL2 and SDA2, and disable the UART2 transmit interrupt.
- When a NACK is detected, release pins SCL2 and SDA2, and disable the UART2 transmit interrupt.

---

### Declaration

unsigned short iic_slave_end(void)

### Outline

Slave control completed processing

### Argument

<table>
<thead>
<tr>
<th>Name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>-</td>
</tr>
</tbody>
</table>

### Variable (global)

<table>
<thead>
<tr>
<th>Name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>(structure member) iic_end</td>
<td>Communication completed flag</td>
</tr>
<tr>
<td>(structure member) iic_rw</td>
<td>R/W flag</td>
</tr>
<tr>
<td>unsigned char iic_index</td>
<td>Number of transmit/receive bytes</td>
</tr>
</tbody>
</table>

### Returned value

<table>
<thead>
<tr>
<th>Type</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned short</td>
<td>IIC_BUSY</td>
<td>Mid-communication</td>
</tr>
<tr>
<td></td>
<td>IIC_REND</td>
<td>Reception completed</td>
</tr>
<tr>
<td></td>
<td>IIC_TEND</td>
<td>Transmission completed</td>
</tr>
<tr>
<td></td>
<td>IIC_ERR</td>
<td>Overrun error detected</td>
</tr>
<tr>
<td>Lower byte</td>
<td>1 to 255</td>
<td>Number of transmit/receive bytes</td>
</tr>
<tr>
<td>Upper byte</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Function

Called from the main processing. It informs the user of the state of slave control completion.

- When the communication completed flag is 1 and there is transmit/receive data except for the slave address, disable I2C mode. Otherwise, return IIC_BUSY (mid-communication).
- After disabling I2C mode, when the communication completed flag is 0, the next communication is determined to be started and the IIC_ERR (overrun error detection) function is returned. When the communication completed flag is 1, return IIC_REND (reception completed) or IIC_TEND (transmission completed).
4.3 Main Processing

main()

asm("FCLR I")

PLL mode setting
SetPLLClock()

asm("FSET I")

loop
    i = 0; i < BUFSIZE; i++
    iic_tx[i] ← i + 1
    iic_rx[i] ← 0x00

UART2 initial setting
uart2_init()

Slave control completed processing
iic_slave_end()

temp.all ← Returned value

temp.byte.byte0

= IIC_REND (reception completed)
= IIC_TEND (transmission completed)
= IIC_ERR (overrun error)

Read receive buffer (1)
Set transmit data (1)
Initialize receive buffer (1)

UART2 initial setting
uart2_init()

UART2 special mode 1 (I²C mode) enabled

Note:
1. Additional processing can be added as needed.
### 4.4 UART2 Initial Setting

```c
uart2_init()

asm("FCLR I")

ini = 1?

= 1 (I2C mode enabled)

U2CMR ← 0x01

BCN2IC ← 0x00

S2TIC ← 0x00

S2RIC ← 0x00

U2C1 ← 0x00

U2MR ← 0x0A

U2SMR2 ← 0x11

U2SMR3 ← 0xE2

U2SMR4 ← 0x30

U2C0 ← 0x90

U2C1 ← 0x15

BCN2IC ← 0x00

S2TIC ← 0x00

S2RIC ← 0x01

P7_0S ← 0x43

P7_1S ← 0x43

PD_IIC ← PD_IIC & PD_IIC_INIT_INPUT

iic_status ← 0x00

U2C1 ← 0x00

asm("FSET I")

return
```

**Arguments**

- `ini`: unsigned char
  - 0: I2C mode disabled
  - 1: I2C mode enabled

**Description**

- **uart2_init()**
  - Disable interrupts.
  - Select I2C mode.
  - Disable stop condition detection interrupt.
  - Disable UART2 transmit interrupt.
  - Disable UART2 receive interrupt.
  - Disable transmission/reception.
  - Select I2C mode, select external clock.
  - Select UART2 transmit/UART2 receive interrupt, enable UART2 auto initialize function.
  - Clock phase: With clock delay SDA2 digital delay: 7 to 8 cycles of U2BRG count source
  - Enable NACK output.
  - U2BRG count source: f1 Transfer format: MSB first
  - Disable transmission/reception.
  - Select transmission completed (TXEPT is 1) as UART2 transmit interrupt source.
  - Set IR bit to 0.
  - Enable UART2 receive interrupt.
  - Set SDA2 pin to N-channel open drain output.
  - Set SCL2 pin to N-channel open drain output.
  - Set pins P7_0 (SDA2) and P7_1 (SCL2) to output mode.
  - Clear all status flags.
  - Enable transmission/reception.
  - Enable interrupts.

**Note**

- `asm("FCLR I")`
- `asm("FSET I")`
4.5 Stop Condition Detection Interrupt Handling

```
_stop_condition_detection()

BBS = 0?
  ≠ 0 (start condition detection (busy))
  = 0 (stop condition detection)
  = 0 (stop condition detection)

Stop condition detection processing
stp_int()

return
```

4.6 Stop Condition Detection Processing

```
stp_int()

U2C1 ← 0x10
PD_IIC ← PD_IIC_INIT_INPUT
U2MR ← 0x00
U2SMR4 ← 0x30
U2MR ← 0x0A
U2SMR2 ← 0x11
BCN2IC ← 0x00
S2TIC ← 0x00
S2RIC ← 0x01
PD_IIC ← PD_IIC_INIT
iic_end ← 1
U2C1 ← 0x15

return

Disable transmission/reception.
Set pins P7_0 (SDA2) and P7_1 (SCL2) to input mode.
Disable serial interface.
Output NACK (release SDA2 pin).
Select I^2C mode, select external clock.
Select UART2 transmit/UART2 receive interrupt.
Disable stop condition detection interrupt.
Disable UART2 transmit interrupt.
Enable UART2 receive interrupt.
Set pins P7_0 (SDA2) and P7_1 (SCL2) to output mode.
Set communication completed flag to 1.
Enable transmission/reception.
4.7 UART2 Receive Interrupt Handling

```c
__uart2_receive()

temp.all ← U2RB

Slave address determine processing
iic_id_check()

iic_pointer ← Retumed value

(iic_pointer = NULL) = NULL (slave address match)

U2SMR4 ← 0xA0

Wait releasing SDA2 pin
U2BRG count source \times \text{Waiting time of SDA2 digital delay or more}

S2TIC ← (S2TIC | 0x01) & 0x0F

S2RIC ← 0x00

BCN2IC ← 0x01

iic_index ← 0

iic_status ← 0x00

iic_rw ← temp.bit.b8

iic_rw = 0?

= 0 (slave receive)

Set the next byte transmit data.

temp.byte.byte0 ← *iic_pointer

temp.byte.byte1 ← 0x01

iic_pointer++

U2TB ← temp.all

U2SMR2 ← 0x11

Release SCL2 pin to low hold.

return

Note:
1. U2BRG count source \times \text{Waiting time of SDA2 digital delay or more}
```
4.8 Slave Address Determine Processing

```
void iic_id_check()
{
  [Argument]
  unsigned char id: Received slave address
  unsigned char rw: R/W flag

  (id & 0x7F) ≠ DEVICE_ADDRESS (slave address not match)

  = DEVICE_ADDRESS (slave address match)

  (rw & 0x01) = 0x00? = DEVICE_ADDRESS (slave address match)

  ≠ 0x00 (slave transmit)

  = 0x00 (slave receive)

  return(iic_rx)
}
```

4.9 UART2 Transmit Interrupt Handling

```
void _uart2_trans()
{
  temp.all ← U2RB
  Read the U2RB register.

  iic_index = 0?

  ≠ 0 (from second byte on)

  = 0 (first byte (slave address))

  ACKC ← 0
  Disable ACK output.

  Wait releasing SDA2 pin (1)

  iic_rw = 0?

  ≠ 0 (slave transmit)

  = 0 (slave receive)

  Slave receive processing

  slave_rcv_int()

  Slave transmit processing

  slave_trn_int()

  return
}
```

Note:
1. U2BRG count source × Waiting time of SDA2 digital delay or more
4.10 Slave Receive Processing

```
slave_rsv_int()

iic_index < BUFSIZE?
< BUFSIZE (less than buffer size)
= 0 (first byte (slave address))
≠ 0 (from the second byte on)

*iic_pointer ← rb_data
iic_pointer++
iic_index++

U2TB ← 0x00FF
SWC9 ← 0
SWC9 ← 1

return
```

Note:
1. U2BRG count source × Waiting time of SDA2 digital delay or more
4.11 Slave Transmit Processing

![Flowchart of Slave Transmit Processing]

- **iic_index**: unsigned char rb_data: ACK/NACK data read from the U2RB register

- **temp.byte**: Set the next byte transmit data.

- **temp.byte.byte0**: Set data to release SDA2 pin at the ninth bit.

- **U2TB**: Set transmit data to the U2TB register (transmission started).

- **Wait releasing SDA2 pin (3)**: Release SDA2 pin.

- **U2SMR4**: Release SCL2 pin (SWC9 is 0).

- **S2TIC**: Disable UART2 transmit interrupt.

- **return**: After ninth bit received, set the SCL2 pin to low fixed.

**Note:**
1. U2BRG count source \( \times \) Waiting time of SDA2 digital delay or more
4.12 Slave Control Completed Processing

iic_slave_end()

(iic_end = 1) & (iic_index > 1)?
(iic_end = 1) and (iic_index > 1)
(mid-communication or no transmit/receive data)

(iic_end = 1) & (iic_index <= 1)
(mid-communication or no transmit/receive data)

UART2 initial setting
tuart2_init()

Disable UART2 special mode 1 (I2C mode).

iic_end = 0?
= 0 (mid-communication)

= 0 (other than mid-communication)

iic_buf_full = 1?
= 1 (within buffer size)

= 1 (buffer full)

temp.byte.byte1 ← iic_index

Set number of transmit/receive bytes.

temp.byte.byte1 ← iic_index - 1

iic_rw = 0?
= 0 (slave transmit)

= 0 (slave receive)

temp.byte.byte0 ← IIC_REN

Set status (receive completed).

temp.byte.byte0 ← IIC_TEN

Set status (transmit completed).

temp.byte.byte0 ← IIC_ERR

Set status (overrun error).

temp.byte.byte0 ← IIC_BUSY

Set status (mid-communication).

return(temp.all)
5. **Sample Program**

A sample program can be downloaded from the Renesas Electronics website.

6. **Reference Documents**

   R32C/118 Group User’s Manual: Hardware Rev.1.10
   The latest version can be downloaded from the Renesas Electronics website.

   Technical Update/Technical News
   The latest information can be downloaded from the Renesas Electronics website.

   C Compiler Manual
   R32C/100 Series C Compiler Package V.1.02
   C Compiler User’s Manual Rev.2.00
   The latest version can be downloaded from the Renesas Electronics website.

**Website and Support**

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
## Revision History

<table>
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<th>Date</th>
<th>Page</th>
<th>Description</th>
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<td>1.00</td>
<td>Aug 31, 2010</td>
<td>8</td>
<td>Modify: ROM size is 657 byte in Table3.2.</td>
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<td>17</td>
<td>Add: “Wait releasing SDA2 pin” in “4.7 UART2 Receive Interrupt Handling”</td>
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<td>18</td>
<td>Add: “Wait releasing SDA2 pin” in “4.9 UART2 Transmit Interrupt Handling”</td>
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<td>19</td>
<td>Add: “U2SMR4 ← 0xB0”, “Wait releasing SDA2 pin” in “4.10 Slave Receive Processing”</td>
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<td>20</td>
<td>Add: “U2SMR4 ← 0xB0”, “Wait releasing SDA2 pin” in “4.11 Slave Transmit Processing”</td>
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<td>1.01</td>
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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
     In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
     In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.
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