1. Abstract

The intelligent I/O interrupt has multiple interrupt request sources, such as a time measurement interrupt and a waveform generation interrupt. It bundles several interrupt requests sources and use them as one intelligent I/O interrupt. This document describes how to use the intelligent I/O interrupt.

2. Introduction

The application example described in this document applies to the following microcomputers (MCUs):

MCUs: R32C/116 Group, R32C/117 Group, R32C/118 Group, R32C/120 Group, and R32C/121 Group

This application note can be used with other R32C/100 Series MCUs which have the same special function registers (SFRs) as the above groups. Check the manuals for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.
3. **Intelligent I/O Interrupt**

3.1 **Explanation**

Figure 3.1 shows the Intelligent I/O Interrupt Block Diagram (i = 0 to 11). Figure 3.2 and Figure 3.3 show Bit Symbols for the Intelligent I/O Interrupt Request Register i (i = 0 to 11) and Bit Symbols for the Intelligent I/O Interrupt Enable Register i, respectively.

To use the intelligent I/O interrupt, the IRLT bit in the IIOiIE register should be set to 1 (interrupt requests used for interrupt) (i = 0 to 11).

The intelligent I/O interrupt has multiple request sources. When an interrupt request is generated with an intelligent I/O function, the corresponding bit in the IIOiIR register becomes 1 (interrupt requested). If the corresponding bit in the IIOiIC register is set to 1 (interrupt enabled), the IR bit in the corresponding IIOiIC register changes to 1 (interrupt requested).

![Intelligent I/O Interrupt Block Diagram](image)

**Figure 3.1 Intelligent I/O Interrupt Block Diagram (i = 0 to 11)**

1. Refer to Figures 3.2 and 3.3 for bits 1 to 7 in registers IIOiIR and IIOiIE and their respective interrupt request sources.

2. Bits 1 to 7 in the IIOiIR register do not become 0 even if an interrupt request is accepted. They should be set to 0 by a program.

3. The IRLT bit and the interrupt enable bit in the IIOiIE register should not be rewritten simultaneously.
3.2 Notes on the Intelligent I/O Interrupt

The IR bits in the IIOIIC register are set to 0 automatically if an interrupt is accepted (i = 0 to 11). However, bits in the IIOIIR register do not become 0 even if an interrupt is accepted. They should be set to 0 by either the AND or BCLR instruction within an interrupt handler.

Note that every generated interrupt request is ignored until these bits are set to 0.
4. Usage Example

4.1 Peripheral Function

This section describes an example of how to use the intelligent I/O interrupt using waveform generation. Table 4.1 lists the Group, Channel Number, and Function Assignment.

**Table 4.1 Group, Channel Number, and Function Assignment**

<table>
<thead>
<tr>
<th>Group</th>
<th>Channel</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Group 0</td>
<td>Channel 0</td>
<td>Waveform generation (single-phase waveform output mode)</td>
</tr>
<tr>
<td>Group 1</td>
<td>Channel 4</td>
<td>Waveform generation (single-phase waveform output mode)</td>
</tr>
</tbody>
</table>

To use both the group 0 waveform generation function channel 0 (PO00) interrupt and the group 1 waveform generation function channel 4 (PO14) interrupt, set both bits PO00E and PO14E in the IIO1IE register to 1. When the PO00 interrupt request is generated, the PO00E bit in the IIO1IR register becomes 1 and when the PO14R interrupt request is generated, the PO14R bit in the IIO1IR register becomes 1. When either the PO00R bit or the PO14R bit, or both bits become 1, the IR bit in the IIO1IC register becomes 1. When reading the IIO1IR register within an interrupt handler, the MCU determines the generated interrupt sources and executes the interrupt handler.

Figure 4.1 shows an Operation Example of Intelligent I/O Interrupt 1.
4.2 Settings

This section shows the setting procedure and setting values in registers IIO1IR, IIO1IE, and IIO1IC to execute the example in 4. “Usage Example”. Refer to the hardware user’s manuals for details of each register.

![Figure 4.2 Register Setting Procedure of Intelligent I/O Interrupt 1]

- **Start**
  - IIO1IR register ← 00h
  - Initialize interrupt request.
  - IIO1IE register IRLT bit ← 1
  - Use interrupt requests for interrupt.
  - IIO1IE register PO00E bit ← 1
  - Group 0 waveform generation function channel 0 interrupt enabled
  - PO14E bit ← 1
  - Group 1 waveform generation function channel 0 interrupt enabled
  - IIO1IC register Bits ILVL2 to ILVL0 IR bit ← 0
  - Interrupt priority level select bit
  - No interrupt requested

**End**

Note:
1. Do not set (2) and (3) simultaneously. Set the interrupt enable bits in the IIO1IE register to 1 after setting the IRLT bit to 1.

See Note 1
## 4.3 Program Flowchart

Figure 4.3 and Figure 4.4 show the main Function Flowchart and the Function Flowchart of Intelligent I/O Interrupt 1, respectively.

### Figure 4.3 main Function Flowchart

1. Disable maskable interrupts
2. Set intelligent I/O group 0 and group 1
3. Initialize IIO1IR register
   - Set registers IIO1IE and IIO1IC
4. Enable maskable interrupts
5. Base timer start (group 0 and group 1)

### Figure 4.4 Function Flowchart of Intelligent I/O Interrupt 1

1. PO00 or PO14 interrupt requested?
   - Yes
     - PO00 interrupt requested?
       - Yes
         - Clear PO00 interrupt request
         - PO00 interrupt handler
         - Invert P7_6
       - No
2. PO00 interrupt requested?
   - Yes
3. Clear PO00 interrupt request
4. PO00 interrupt handler
5. PO14 interrupt requested?
   - Yes
     - Clear PO14 interrupt request
8. PO14 interrupt handler
   - Invert P7_7
9. End interrupt handler
5. **Sample Program**

A sample program can be downloaded from the Renesas Electronics website.

6. **Reference Documents**

User’s Manuals
- R32C/116 Group User’s Manual: Hardware Rev.1.00
- R32C/117 Group User’s Manual: Hardware Rev.1.00
- R32C/118 Group User’s Manual: Hardware Rev.1.00
- R32C/120 Group User’s Manual: Hardware Rev.1.10
- R32C/121 Group User’s Manual: Hardware Rev.1.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
- R32C/100 Series C Compiler Package V.1.02 C Compiler User’s Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

**Website and Support**

Renesas Electronics website
http://www.renesas.com/

Inquiries
http://www.renesas.com/inquiry
# REVISION HISTORY

## R32C/100 Series

**How to Use Intelligent I/O Interrupt**

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Aug. 31, 2010</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.
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