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## H8/300L

### Hardware Interface Technique for Reset (HWreset)

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#### Introduction

This application note is to assist the product design engineers to understand the important of a reset circuitry within a total micro-controller-based system and to provide sample circuitry based on the H8/300L Super Low Power (SLP) series microcomputer, H8/38024F.

Resets provide a digital signal to the microcomputer that not only indicates the voltage level but also provides that the reset signal is delayed to allow the voltage to arrive at its nominal value. That delay also allows the power supply and board to fully stabilize prior to starting operation.

Reset signal generating for a microcomputer must be able to trigger from a variety of sources. Most notably, during a power failure situation, during power up and externally as a user demanded system reset.

#### Target Device

H8/300L Super Low Power series – H8/38024F microcomputer

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## 1. H8/38024F Microcomputer

### 1.1 Reset Sequence

Reset is the highest-priority exception. The internal state of the CPU and registers of the on-chip peripheral modules are initialized.

As soon as the /RES pin goes low, all processing is stopped and the chip enters the reset state.

To make sure the chip is reset properly, observe the following precautions [Refer to Figure 1.1]:

- At Power-On, hold the /RES pin low until the clock pulse generator output stabilizes. [Refer to AN: 02/12/001 as well]
- At Reset during operation, hold the /RES pin low for at least 10 system clock cycles.

Reset exception handling takes place as follows:

- The CPU internal state and the registers of on-chip peripheral modules are initialised with the I bit of the condition code register [CCR] set to '1'.
- The Program counter [PC] register is loaded from the reset exception handling vector address [H'0000 to H'0001], after which the program starts executing from the address indicated in Program counter register.

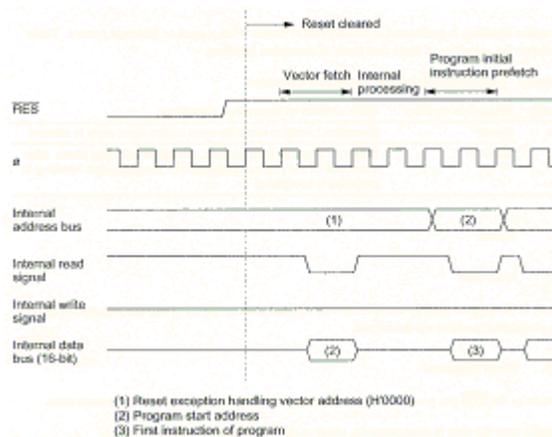


Figure 1.1 Reset Sequence

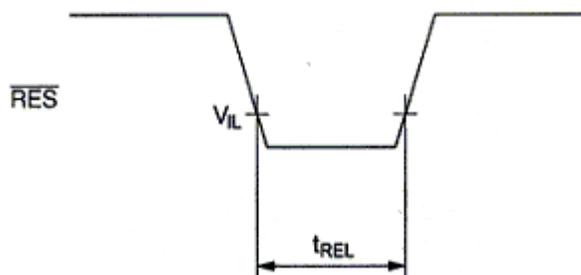


Figure 1.2 Reset Low Width

## 1.2 Operational Timing

The /RES pin is held low when the slope of VCC maintained at less than 0.1VCC value. This also retains the chip at the reset state. From Figure 1.2, the reset low width should be maintained for at least 10 system clock cycles.

## 1.3 Interrupt Immediately after Reset

After a reset, if an interrupt is to be accepted before the stack pointer [SP: R7] was initialized, PC and CCR would incorrectly pushed onto the stack and resulting in program runaway. In order to prevent this, all interrupts must be masked immediately after reset exception handling.

For this reason, the initial program instruction is always executed immediately after a reset. This instruction should initialize the stack pointer [eg. MOV #xxx: 16. SP].

## 2. Circuits Consideration

### 2.1 Typical design I

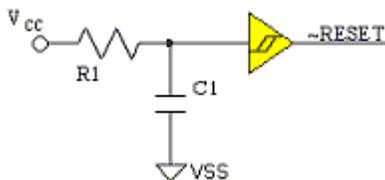


Figure 2.1 Reset circuit I

This circuit works beautifully in simulation, assuming that VCC voltage rises quickly and monotonically to its maximum value and stays there. However, in real world, power outages often occurs, and this would draw a large amount of current, which shorts out the power voltage. Power interruption drives power on reset circuitry crazy.

Consider what a power dropout does to the circuit in Figure 2.1 [indicated above]. Imagine that the RC time constant in the figure is 1 sec. Let VCC come up and stabilize at full voltage for perhaps 10 sec. Next apply an ac power interruption just long enough to drop VCC to 0V for about 100msec. However, this still would not be able to discharge the RC circuit. If the RC circuit does not discharge, reset does not activate, and the processor spins out of control, powered on but lost in space. Hence, for most systems, the simple RC-based power-on reset circuit is completely inadequate.

A good power-on-reset circuit must activate when power is currently good and has been good for some time and must completely and quickly deactivate upon any indication of poor power quality.

2.2 Typical design II

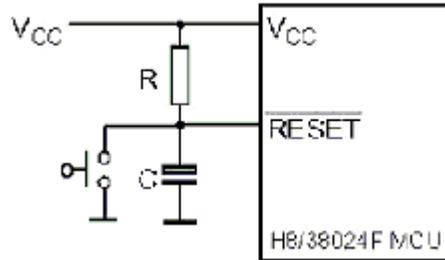
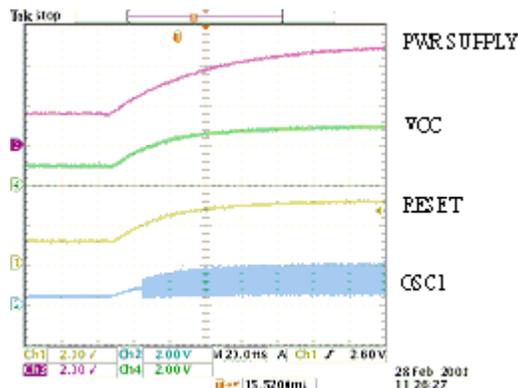


Figure 2.2 Reset Circuit II

Figure 2.2 represents another connection with push button for power-on reset. Upon power-on, the reset pin is held low for the duration indicated by the value of the RC constants and maintain until VCC reaches VCCmin. The push button is used to provide a manual way to reset the system and a discharging path for the capacitor. This is necessary when the system is out of control and a reset is the best way to recover the system to normal operation.

Below shows the various waveforms depicting the behaviour of the power supply, the VCC input, the reset signal and the main clock signal, OSC.

2.2.1 When the DC plug supplying the VCC input is connected/disconnected



The above waveform depicts the slow rising power supply signal measured at the DC plug when the power supply is switched on; while the power supply signal is gradually rising, the VCC pin of the microcomputer is also measured. We also noticed that the resetsignal also rises slowly while the clock signal oscillated before the power supply stabilizes. For H8/38024F microcomputer, it is specified that the Reset signal must be held low for at least ten system clock cycles to ensure proper operation subsequently. The rising time of these signals mentioned above is dependent on the capacitive load found in the printed circuit board at power up.

### 2.3 Typical design III

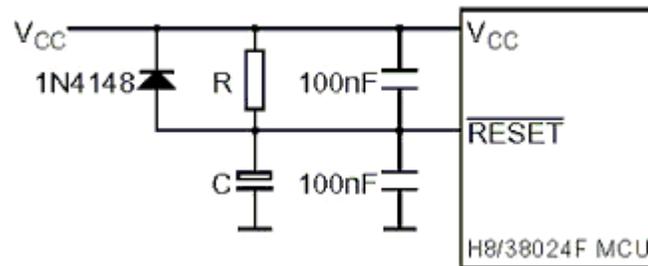


Figure 2.3 Reset Circuit III with a Discharge Diode

In Figure 2.3 above, the 1N4148 diode is used to rapidly discharge the C capacitor on power-down. This is very important, as a power-up reset pulse is needed after a short power-down (less than the time given by the RC constant) or after a power spike. The two 100nF capacitors allow the reset pin level to follow the voltage variations that appear on either VCC or VSS.

Note: The above-described designs do not protect against brownout situation where power does not drop to zero but merely dip below the minimum operating voltage.

### 2.4 Typical design IV

Figure 2.4 represents another connection which involves a supervisory IC such as those of Maxim's IC such as MAX809. This is believed to help to prevent oscillatory behavior at the detecting threshold without resorting to excessive hysteresis. In order to do this, we must delay the trailing edge of the reset pulse. As in the RC circuit described above, the reset pulse must hold for an interval after the supply voltage crosses the detector's threshold. This interval is called 'delay time' or the 'rest active-timeout period'. Unlike the RC circuit delay, however this one triggers when supply voltage crosses a precisely trimmed threshold in the detector. The delay should also be re-triggerable to prevent oscillation in the reset signal of the microcomputer. When a slowly rising supply causes multiple trigger events at detector threshold, each event should re-start the timeout

The Maxim part offers a guaranteed accuracy of  $\pm 2.6\%$  over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  range. The MAX809 also guarantees a minimum active-timeout reset period of 140ms.

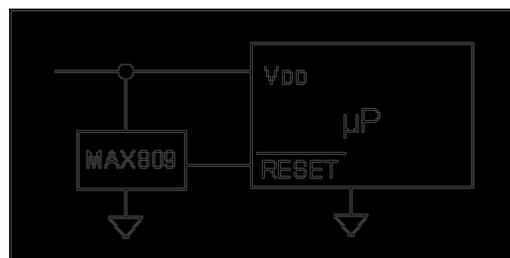


Figure 2.4 Reset Circuit IV with Maxim IC (MAX809)

### 3. Trouble Shooting

#### 3.1 Why the system does not operate properly upon Power-On?

Possibilities:

- VCC ramp rate is too slow;
- Slow VCC rise time which was too slow to cause a proper reset to occur;

/RES pin should be held low when system power is turned on or off;

#### 3.2 Why the system does not operate properly when it was powered-down and powered-On again?

Possibilities:

- VCC may not be given enough time to settle to 0V;
- VCC ramp rate is too slow;
- Slow VCC rise time which was too slow to cause a proper reset to occur;
- /RES pin should be held low when system power is turned on or off;

Other hardware peripherals or logics on the system may not be reset properly.

### 4. Conclusions

There are many approaches to implement a power-on reset circuit, some designers may implement designs as outlined in this application note, but some may implement with an external supervisory circuit due to the stringent requirement by their systems to ensure optimum operating condition at all time.

This application note provides some guidance on how to implement reset circuit to interface with the H8/38024F MCU and also pointers to take note while implementing the reset design in order to ensure proper operation of the system.

### Reference

1. H8/38024 Series, H8/38024F-ZTAT™ Hardware Manual
2. [www.ednmag.com](http://www.ednmag.com)
3. [www.embedded.com](http://www.embedded.com)

**Revision Record**

Rev.	Date	Description	
		Page	Summary
1.00	Sep.03	-	First edition issued

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