HARDWARE DESIGN GUIDE

TARGET DEVICE: RL78/F13, F14, F15

REV: 1.00

DATE: 2021. 9.30

MCU MARKETING DEPARTMENT
AUTOMOTIVE DIGITAL PRODUCTS MARKETING DIVISION
RENESAS ELECTRONICS CORPORATION

R01AN6057EJ0100

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INTRODUCTION

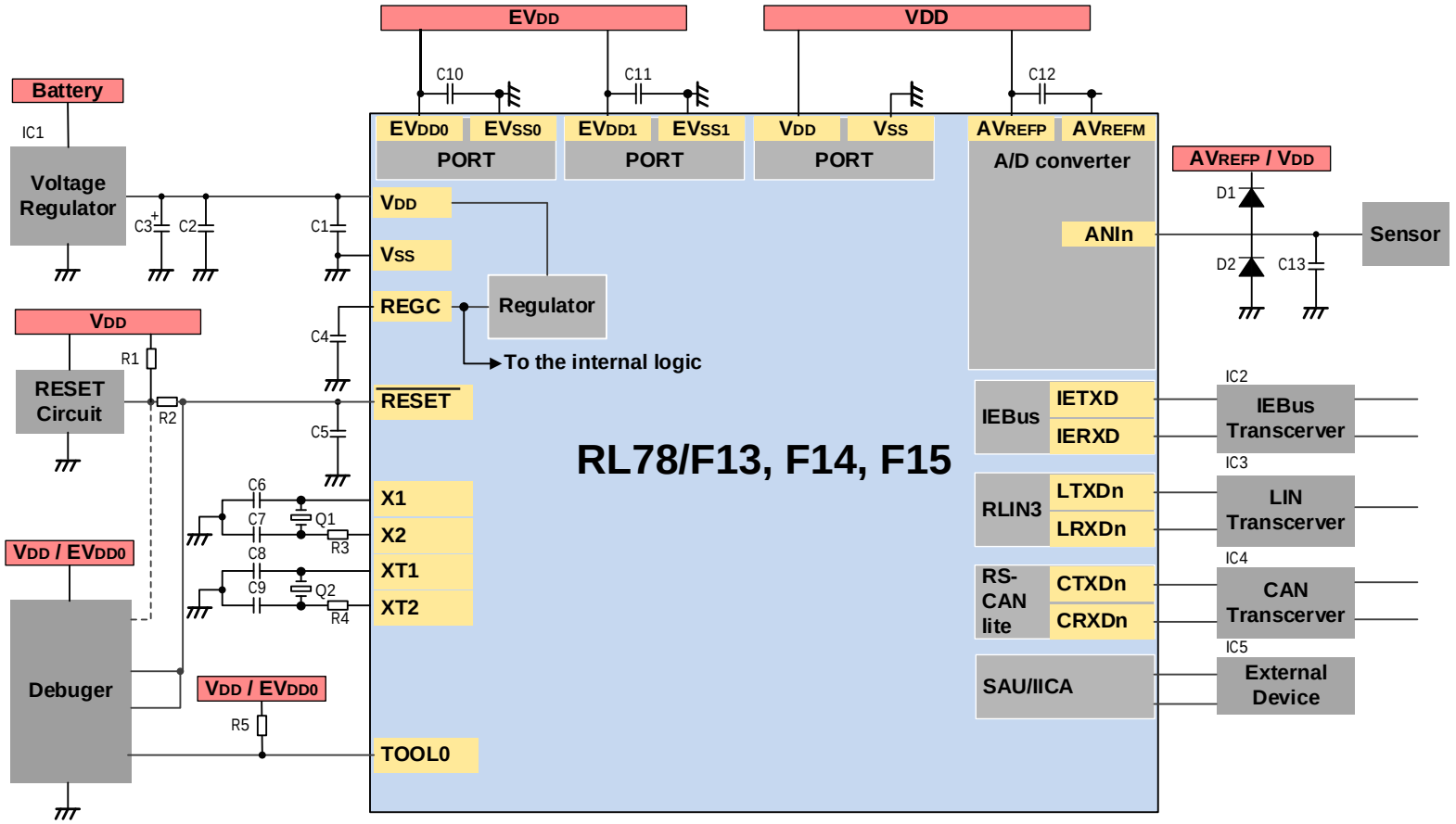
This document is intended to provide the hardware specific information and recommendations on RL78/F13, F14, F15 usage. It should be used in conjunction with the corresponding Hardware User's Manual (includes the electrical characteristics).

Target devices: RL78/F13, F14, F15

CONTENTS

TYPICAL CIRCUIT SCHEMATIC

Figure 1: Typical Circuit Schematic for the RL78/F13, F14, F15



Note 1: The above figure illustrates the major circuit schematic for the target device (RL78/F13, F14, F15). For unused pins, follow the section related to recommended connection of unused pins in each hardware user's manual.
2: Available functions depend on the product. For details, check each hardware user's manual.

MINIMUM EXTERNAL COMPONENTS LIST (1/2)

The following table shows the minimum external components list for the typical circuit schematic on Page 5.

Table 1: Minimum External Components List (1/2)

Category	Components	Value (Typ.)	Purpose	Remark	Supplement
Power supply	IC1	No recommended IC	Generating power supply for V_{DD}	Depends on the user system.	P.8, 9
	C1	0.1uF	Bypass capacitor	Reference value. Place it near the V_{DD} pin.	
	C2, C3	No recommended value	Stabilizing the output voltage of the voltage regulator	Follow the recommendation of the data sheet of the voltage regulator IC.	
	C4	0.47uF to 1.0uF	Stabilizing the internal regulator output voltage	Place it near the REGC pin.	P.10
	C10	0.1uF	Bypass capacitor	Reference value. Place it near the EV_{DD0} pin.	–
	C11	0.1uF	Bypass capacitor	Reference value. Place it near the EV_{DD1} pin.	
Reset	R1	1.0kΩ	Pull-up resistor	Depends on the external reset circuit.	P.11
	C5	0.1uF	Bypass capacitor	Reference value. Place it near the $\overline{\text{RESET}}$ pin.	
Oscillator circuit (Main System Clock)	Q1	1MHz to 20MHz	Generating clock signal source for the main system clock	Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant.	P.12,14,15
	C6, C7	No recommended value			
	R3	No recommended value			

MINIMUM EXTERNAL COMPONENTS LIST (2/2)

Table 2: Minimum External Components List (2/2)

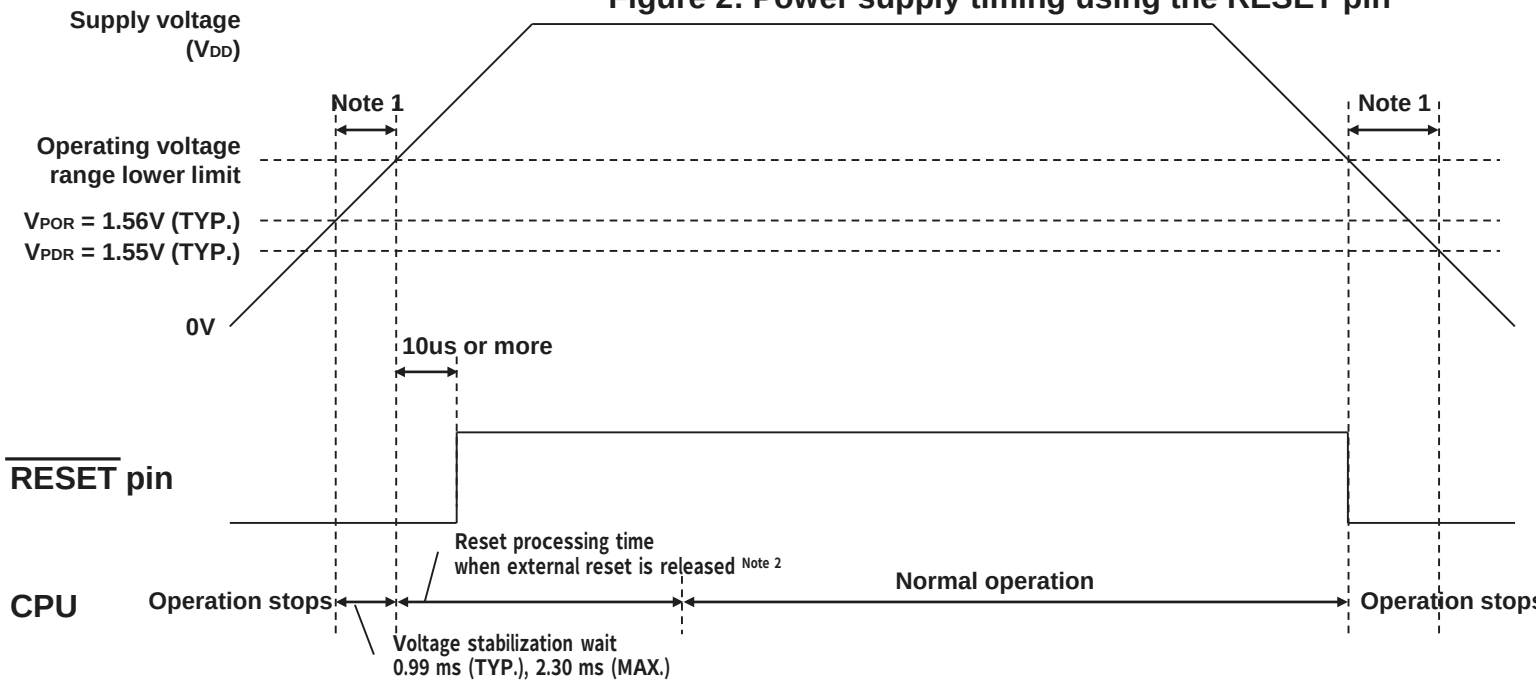
Category	Components	Value (Typ.)	Purpose	Remark	Supplement
Oscillator circuit (Subsystem Clock)	Q2	32.768kHz	Generating clock signal source for the subsystem clock	Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant.	P.13,14,15
	C8, C9	No recommended value			
	R4	No recommended value			
A/D converter	C12	0.1uF	Bypass capacitor	Reference value. Place it near the AV_{REFP} pin.	P.16,17,18
	D1, D2	$V_F \leq 0.3V$	Noise protection	Depends on the user system.	
	C13	100pF to 1000uF	Stabilizing the sampling operation	Depends on the user system.	
Debug	R2	10kΩ	Current limit between Reset circuit and Debugger	Depends on the external reset circuit.	P.19
	R5	1.0kΩ	Pull-up resistor	Be sure to pull up this pin externally when on-chip debugging is enabled (pulling it down is prohibited).	
IEBus	IC2	No recommended IC	IEBus transceiver	Depends on the user system.	–
LIN	IC3	No recommended IC	LIN transceiver	Depends on the user system.	–
CAN	IC4	No recommended IC	CAN transceiver	Depends on the user system.	–
SAU/IICA	IC5	No recommended IC	Controlling external device	Depends on the user system.	–

POWER SUPPLY TIMING (1/2)

Please note that power supply timing according to the following use case.

(1) When the externally input reset signal on the $\overline{\text{RESET}}$ pin is used.

Figure 2: Power supply timing using the $\overline{\text{RESET}}$ pin



Remark V_{POR}: POR power supply rise detection voltage
V_{PDR}: POR power supply fall detection voltage

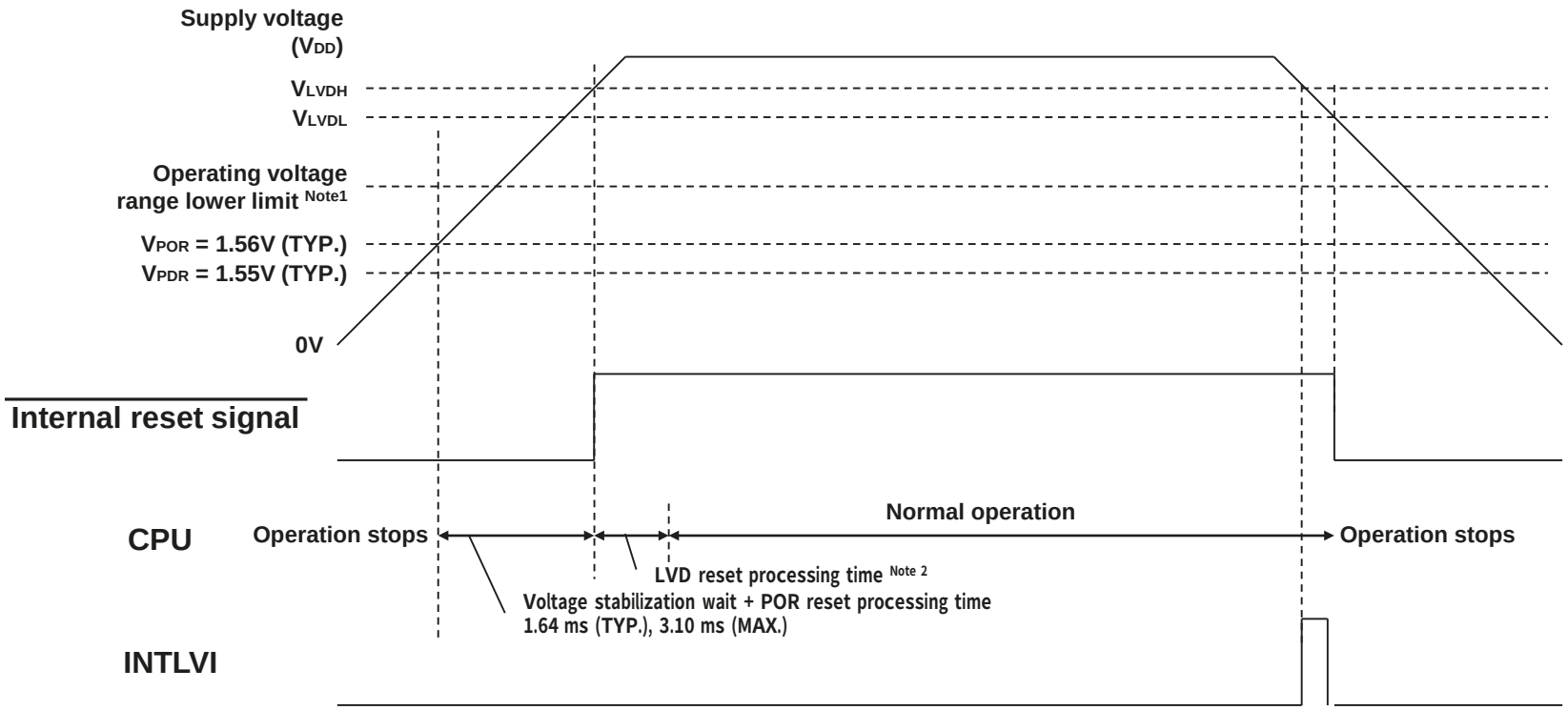
Note 1. After power is supplied, the reset state must be retained until the operating voltage becomes in the range defined in the AC characteristics in the ELECTRICAL SPECIFICATIONS of each Hardware User's Manual. This is done by controlling the externally input reset signal. After power supply is turned off, this LSI should be placed in the STOP mode, or in the reset state by utilizing the voltage detection circuit or externally input reset signal, before the voltage falls below the operating range. When restarting the operation, make sure that the operation voltage has returned within the range of operation.

Note 2. The time until normal operation starts includes the following reset processing time when the external reset is released (after the first release of POR) after the RESET signal is driven high (1) as well as the voltage stabilization wait time after VPOR (1.56 V, typ.) is reached. Reset processing time when the external reset is released is shown below.
After the first release of POR: 0.672 ms (typ.), 0.832 ms (max.) (when the LVD is in use)
0.399 ms (typ.), 0.519 ms (max.) (when the LVD is off)

POWER SUPPLY TIMING (2/2)

(2) When LVD is interrupt & reset mode (option byte 000C1/020C1H: LVIMDS1, LVIMDS0 = 1, 0)

Figure 3: Power supply timing using LVD



Remark V_{LVDH}, V_{LVDL}: LVD detection voltage
V_{POR}: POR power supply rise detection voltage
V_{PDR}: POR power supply fall detection voltage

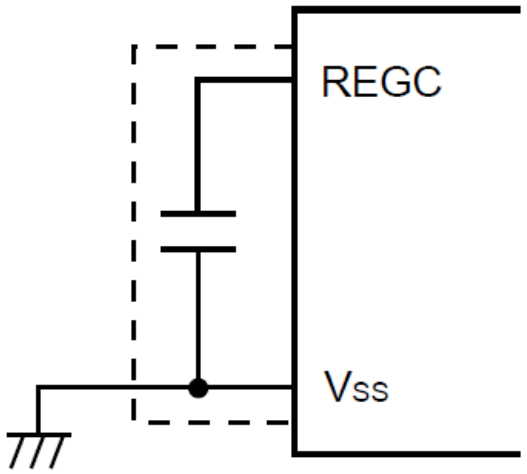
Note 1. The guaranteed range for operation is 2.7 V ≤ V_{DD} ≤ 5.5 V. Only proceed with normal operations after V_{DD} has reached or exceeded 2.7 V. If an operation may be generated at lower than 2.7 V when the supply voltage falls or power-on, use the reset function of the voltage detector, or input the low level to the RESET pin.

Note 2. LVD reset processing time: 0 to 0.0701 ms (MAX.)

REGC PIN

RL78/F13, F14, F15 contain a circuit for operating the device with a constant voltage. At this time, in order to stabilize the regulator output voltage, connect the REGC pin to Vss via a capacitor (0.47 to 1 uF). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.

Figure 4: REGC pin connection



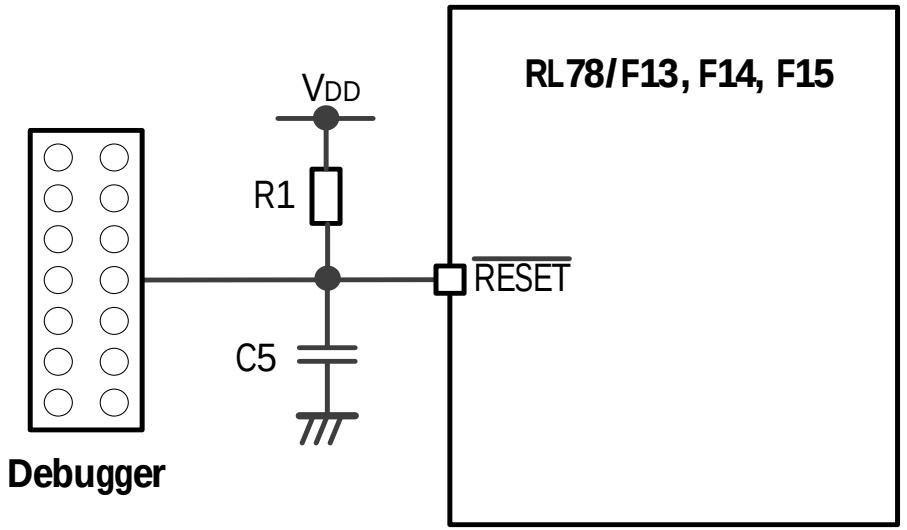
Caution Keep the wiring length as short as possible for the broken-line part in the above figure.

RESET PIN

RL78/F13, F14, F15 has the on-chip Power-on reset circuit (POR). Therefore, a specific external $\overline{\text{RESET}}$ circuit is not required, and the minimum requirement of the RESET circuit is a pull-up resistor R1 (1kΩ to 10kΩ) to V_{DD}. When using the hot plug-in, place a ceramic capacitor C5 (about 0.1 uF) close to the $\overline{\text{RESET}}$ pin to suppress noise to the $\overline{\text{RESET}}$ pin when the emulator is connected.

It depends on user system if an external RESET IC is necessary for a safety reason.

Figure 5: Minimum RESET pin connection

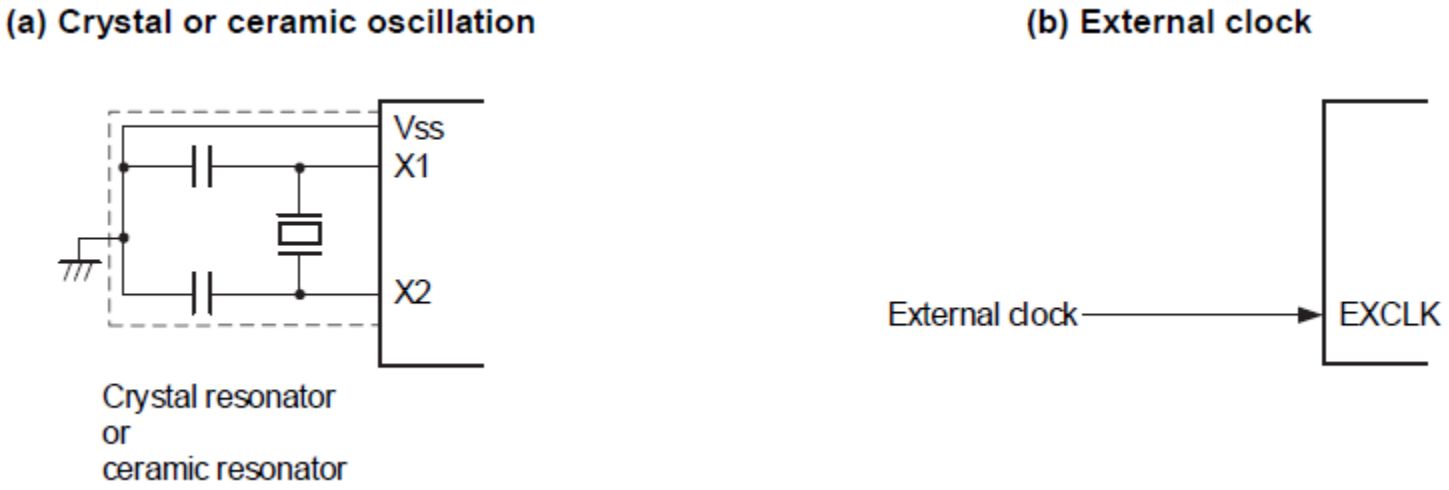


OSCILLATOR CIRCUIT: MAIN SYSTEM CLOCK

Typical circuit for the external oscillator circuit of the main system clock is illustrated below.

The X1 oscillator oscillates with a crystal resonator or ceramic resonator (1 to 20 MHz) connected to the X1 and X2 pins. An external clock can also be input. In this case, input the clock signal to the EXCLK pin.

Figure 6: Main system clock connection



OSCILLATOR CIRCUIT: SUBSYSTEM CLOCK

Typical circuit for the external oscillator circuit of the subsystem clock is illustrated below.

The XT1 oscillator oscillates with a crystal resonator (standard: 32.768 kHz) connected to the XT1 and XT2 pins.

An external clock can also be input. In this case, input the clock signal to the EXCLKS pin.

Figure 7: Subsystem clock connection

COMMON NOTE FOR OSCILLATOR CIRCUIT (1/2)

Cautions Customers are requested to consult the resonator manufacturer to select an appropriate resonator and to determine the proper oscillation constant.

When using the X1 oscillator and XT1 oscillator, wire as follows in the area enclosed by the broken lines in Figures 5 and 6 to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
- Do not cross the wiring with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.
- Always make the ground point of the oscillator capacitor the same potential as Vss. Do not ground the capacitor to a ground pattern through which a high current flows.
- Do not fetch signals from the oscillator.

The XT1 oscillator is a circuit with low amplification in order to achieve low-power consumption.
Note the following points when designing the circuit.

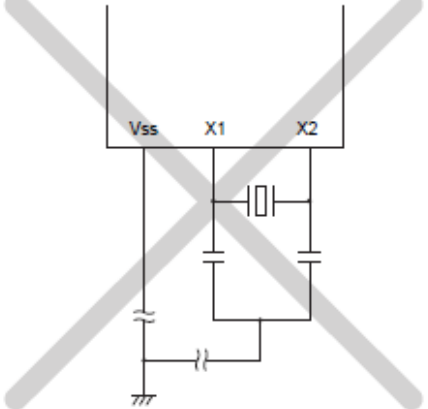
- Pins and circuit boards include parasitic capacitance. Therefore, perform oscillation evaluation using a circuit board to be actually used and confirm that there are no problems.
- Make the wiring between the XT1 and XT2 pins and the resonators as short as possible, and minimize the parasitic capacitance and wiring resistance. Note this particularly when the ultralow power consumption oscillation (AMPHS1, AMPHS0 = 1, 0) is selected.
- Configure the circuit of the circuit board, using material with little wiring resistance.
- Place a ground pattern that has the same potential as Vss as much as possible near the XT1 oscillator.
- Be sure that the signal lines between the XT1 and XT2 pins, and the resonators do not cross with the other signal lines. Do not route the wiring near a signal line through which a high fluctuating current flows.
- The impedance between the XT1 and XT2 pins may drop and oscillation may be disturbed due to moisture absorption of the circuit board in a high-humidity environment or dew condensation on the board. When using the circuit board in such an environment, take measures to damp-proof the circuit board, such as by coating.
- When coating the circuit board, use material that does not cause capacitance or leakage between the XT1 and XT2 pins.

COMMON NOTE FOR OSCILLATOR CIRCUIT (2/2)

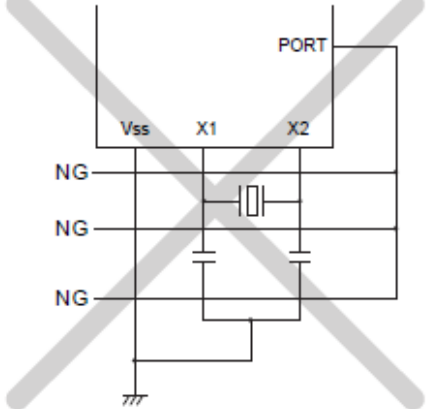
Please avoid the following PCB layout for the external OSC circuit.

Figure 8: Examples of Incorrect Resonator Connection

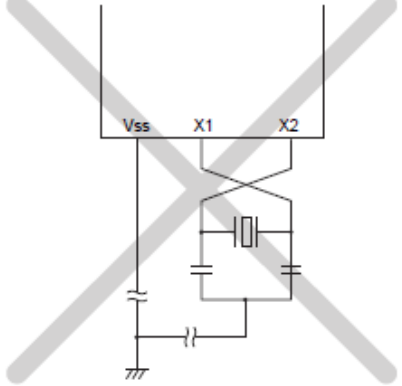
(a) Too long wiring



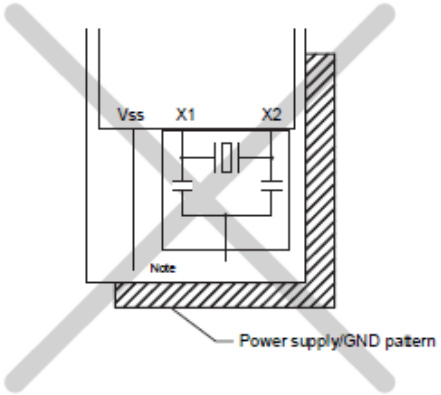
(b) Crossed signal line



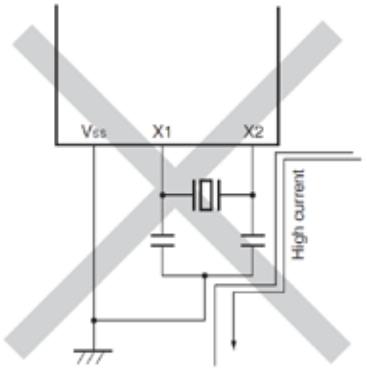
(c) The X1 and X2 signal line wires cross.



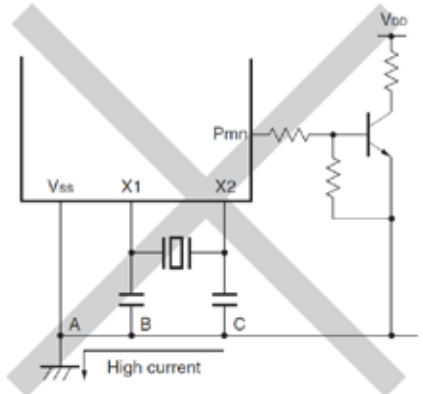
(d) A power supply/GND pattern exists under the X1 and X2 wires.



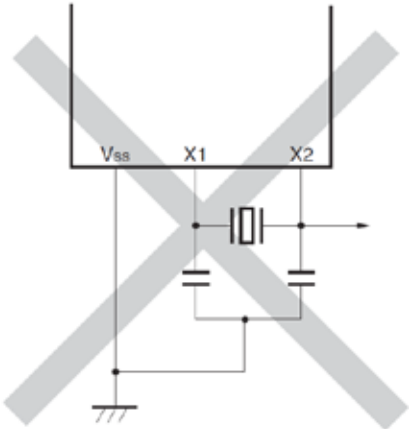
(e) Wiring near high alternating current



(f) Current flowing through ground line of oscillator (potential at points A, B, and C fluctuates)



(g) Signals are fetched



Caution When X2 and XT1 are wired in parallel, the crosstalk noise of X2 may increase with XT1, resulting in malfunctioning.

Remark When using the subsystem clock, replace X1 and X2 with XT1 and XT2, respectively. Also, insert resistors in series on the XT2 side.

NOTE FOR I/O PORT (1/3)

The general purpose I/O of RL78/F13, F14, F15 products have VDD-type I/O and EVDD-type I/O.

Note that port drive current capability are different according to I/O type.

Table 3: IOH and IOL characteristics on each Port type (1/5)

l Target Product: RL78/F13 (LIN) 20-/ 30- /32- /48- /64-pins product (Products with 64 KB or less code flash memory)

Port Type	Applicable General Purpose I/O	Port Characteristics (IOH and IOL)	
		Grade-L Products	Grade-K Products
VDD-type	P33, P34, P80-P87, P90, P91, P121-P124, P137	IOH2: -0.1 mA, IOL2: 0.4 mA	IOH2: -0.1 mA, IOL2: 0.4 mA
EVDD-type	P00, P10-P17, P30-P32, P40-P43, P50-P53, P60-P63, P70-P77, P92-P96, P120, P126, P127, P130, P140	IOH1: -5.0 mA, IOL1: 8.5mA	IOH1: -5.0 mA, IOL1: 8.5 mA

Conditions: Power supply voltage = 4.0V to 5.5V. For other conditions, refer to User's Manual: Hardware.
Note: P121 to P124 and P137 are input-only pins.
Remark: Some general purpose I/O may not be mounted depending on the product.

Table 4: IOH and IOL characteristics on each Port type (2/5)

l Target Product: RL78/F13 (LIN) 64-pins product (Products with 96 KB or more code flash memory), RL78/F13 (LIN) 80-pins product, RL78/F13 (CAN&LIN) 30-/ 32-/ 48-/ 64-/ 80-pins product

Port Type	Applicable General Purpose I/O	Port Characteristics (IOH and IOL)	
		Grade-L Products	Grade-K Products
VDD-type	P33, P34, P80-P87, P90-P95, P121-P124, P137	IOH2: -0.1 mA, IOL2: 0.4 mA	IOH2: -0.1 mA, IOL2: 0.4 mA
EVDD-type	P00-P02, P10-P17, P30-P32, P40-P47, P50-P57, P60-P67, P70-P77, P96, P97, P120, P125, P126, P130, P140	IOH1: -5.0 mA, IOL1: 8.5mA	IOH1: -5.0 mA, IOL1: 8.5 mA

Conditions: Power supply voltage = 4.0V to 5.5V. For other conditions, refer to User's Manual: Hardware.
Note: P121 to P124 and P137 are input-only pins.
Remark: Some general purpose I/O may not be mounted depending on the product.

NOTE FOR I/O PORT (2/3)

Table 5: IOH and IOL characteristics on each Port type (3/5)

l Target Product: RL78/F14 32-/ 48-/ 64-/ 80-pins product (Products with 96 KB or less code flash memory)

Port Type	Applicable General Purpose I/O	Port Characteristics (IOH and IOL)	
		Grade-L Products	Grade-K Products
VDD-type	P33, P34, P80-P87, P90, P91, P121-P124, P137	IOH2: -0.1 mA, IOL2: 0.4 mA	IOH2: -0.1 mA, IOL2: 0.4 mA
EVDD-type	P00, P10-P17, P30-P32, P40-P43, P50-P53, P60-P63, P70-P77, P92-P96, P120, P126, P127, P130, P140	IOH1: -5.0 mA, IOL1: 8.5mA	IOH1: -5.0 mA, IOL1: 8.5 mA

Conditions: Power supply voltage = 4.0V to 5.5V. For other conditions, refer to User's Manual: Hardware.
Note: P121 to P124 and P137 are input-only pins.
Remark: Some general purpose I/O may not be mounted depending on the product.

Table 6: IOH and IOL characteristics on each Port type (4/5)

l Target Product: RL78/F14 48-/ 64-/ 80-pins product (Products with 128 KB or more code flash memory), RL78/F14 100-pins product

Port Type	Applicable General Purpose I/O	Port Characteristics (IOH and IOL)	
		Grade-L Products	Grade-K Products
VDD-type	P33, P34, P80-P87, P90-P97, P100-P105, P121-P124, P137	IOH2: -0.1 mA, IOL2: 0.4 mA	IOH2: -0.1 mA, IOL2: 0.4 mA
EVDD-type	P00-P03, P10-P17, P30-P32, P40-P47, P50-P57, P60-P67, P70-P77, P106, P107, P120, P125-P127, P130, P140, P150-P157	IOH1: -5.0 mA, IOL1: 8.5mA	IOH1: -5.0 mA, IOL1: 8.5 mA

Conditions: Power supply voltage = 4.0V to 5.5V. For other conditions, refer to User's Manual: Hardware.
Note: P121 to P124 and P137 are input-only pins.
Remark: Some general purpose I/O may not be mounted depending on the product.

NOTE FOR I/O PORT (3/3)

Table 7: IOH and IOL characteristics on each Port type (5/5)

l Target Product: RL78/F15 48-/ 64-/ 80-/ 100-/ 144-pins product

Port Type	Applicable General Purpose I/O	Port Characteristics (IOH and IOL)	
		Grade-L Products	Grade-K Products
VDD-type	P33, P34, P80-P87, P90-P97, P100-P105, P121-P124, P137	IOH2: -0.1 mA, IOL2: 0.4 mA	IOH2: -0.1 mA, IOL2: 0.4 mA
EVDD-type	P00-P07, P10-P17, P20-P27, P30-P32, P35-P37, P40-P47, P50-P57, P60-P67, P70-P77, P106, P107, P110-P117, P120, P125-P127, P130-P136, P140-P147, P150-P157, P160-P167	IOH1: -5.0 mA, IOL1: 8.5mA	IOH1: -5.0 mA, IOL1: 8.5 mA

Conditions: Power supply voltage = 4.0V to 5.5V. For other conditions, refer to User's Manual: Hardware.
Note: P121 to P124 and P137 are input-only pins.
Remark: Some general purpose I/O may not be mounted depending on the product.

RECOMMENDED CONNECTION OF UNUSED PINS

Table 8: Recommended Connection of Unused Pins

Port Type	Pin Name	Recommended Connection of Unused Pins
VDD-type	P121 to P124, P137 (Input-only pin)	Independently connect to V_{DD} or V_{SS} via a resistor.
	All VDD-type pins except P121 to P124 and P137	Input: Independently connect to V_{DD} or V_{SS} via a resistor. [Reference resistance value: Pull up with 20 kΩ resistor] Output: Leave open.
	RESET	Connect to V_{DD} directly or via a resistor.
EVDD-type	P40 **Note**	Input: Independently connect to EV_{DD} via a resistor. [Reference resistance value: 1.0 kΩ] Output: Leave open.
	P130 (Output-only pin)	Leave open.
	All EVDD-type pins except P140 and P130	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. [Reference resistance value: 10 kΩ] Output: Leave open.

Note: TOOL0 (On-chip debugger/Flash memory programmer interface pin) function is assigned to P40. When using TOOL0 function on the board, select an input mode and connect to EV_{DD} via a resistor (1.0 kΩ).

PERIPHERAL I/O REDIRECTION FUNCTION

The peripheral I/O pin of RL78/F13, F14, F15 products can be assigned by PIORx register.

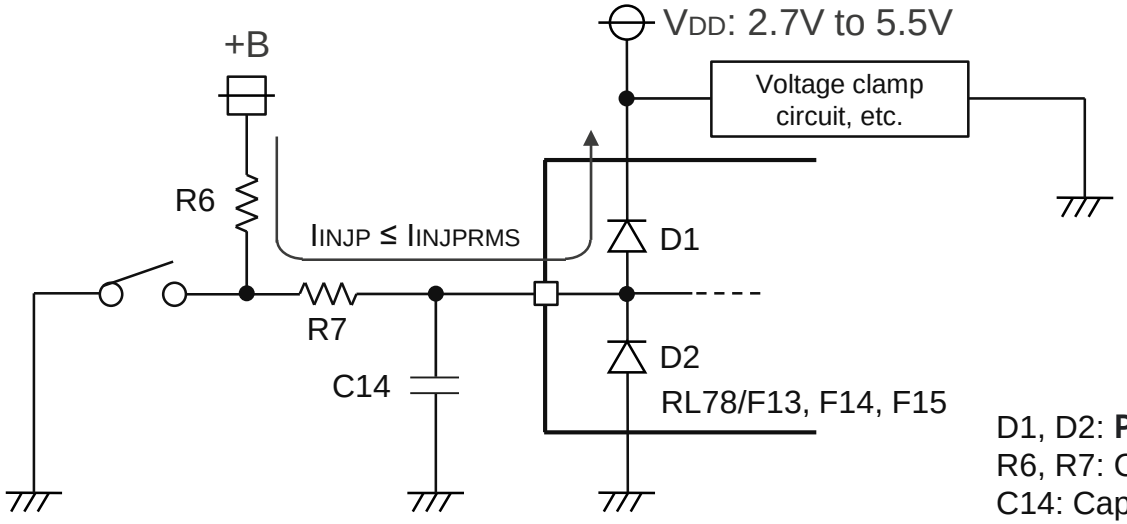
Note that multiple peripheral I/O pin assignments change depending on the bit of the PIORx register settings.

Table 9: PIOR register assignment list

PIORx Register	Assignable Peripheral I/O Functions							
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PIOR0	TI07	TI06	TI05	TI04	TI03	TI02	TI01	TI00
PIOR1	TO07	TO06	TO05	TO04	TO03	TO02	TO01	TO00
PIOR2	TI17	TI16	TI15	TI14	TI13	TI12	TI11	TI10
PIOR3	TO17	TO16	TO15	TO14	TO13	TO12	TO11	TO10
PIOR4	-	CRXD0, CTXD0	LRXD1, LTXD1	LRXD0, LTXD0	SI11/SDA11, SO11, SSI11 SCK11/SCL11.	SI10/SDA10/RXD1, SO10/TXD1, SSI10, SCK10/SCL10	SI01/SDA01, SO01, SSI01, SCK01/SCL01	SI00/SDA00/RXD0, SO00/TXD0, SSI00, SCK00/SCL00
PIOR5	-	-	-	-	INTP3	INTP2	-	KR0 to KR7
PIOR6	SNZOUT7	SNZOUT6	SNZOUT5	SNZOUT4	SNZOUT3	SNZOUT2	SNZOUT1	SNZOUT0
PIOR7	-	-	-	-	TRDIOD0	-	TRDIOB0	TRDIOA0/TRDCLK0
PIOR8	-	-	-	-	-	-	-	RTC1HZ
PIOR9	IERXD, IETXD	CRXD1, CTXD1	-	-	-	-	SCK21, SI21, SO21	SCK20, SI20/RXD2, SO20/TXD2
PIOR10	TI27	TI26	TI25	TI24	TI23	TI22	TI21	TO20
PIOR11	TO27	TO26	TO25	TO24	TO23	TO22	TO21	TO20

INJECTED CURRENT INPUT

Figure 9: Example of injected current input circuit



D1, D2: **Parasitic diode**
R6, R7: Current Limit resistor
C14: Capacitance for suppressing switching noise

Item	Symbol	Port-Type	Conditions	Injected Current Specifications (MAX.)
Positive injected current ($V_{IN} \geq V_{DD}$)	$I_{INJPRMP}$	EVDD-type	P40, P130 (Output-only)	Prohibition
			All EVDD-type pins except P40, P70 to P74, P120, P125 and P130	0.4 mA (per pin), 4 mA (Total of all pins)
			P70 to P74, P120, P125	0.15 mA (per pin), 1 mA (Total of all pins)
		VDD-type	All VDD-type pins except P33, P34, P81 to P84, P121 to P124 and P137	
			P33, P34, P121 to P124, P137	Prohibition
			P81 to P84	0.15 mA (per pin), 0.15 mA (Total of all pins)

Note. These specifications are not tested on sorting and are specified based on the device characterization.

CAUTION FOR A/D CONVERTER (1/3)

- **Input range of ANIn pins**

  Observe the rated range of the ANIn pins input voltage. If a voltage higher than V_{DD} and AV_{REFP} and less than V_{SS} and AV_{REFM} (even in the range of absolute maximum ratings) is input to an analog input channel, the converted value of that channel becomes undefined. In addition, the converted values of the other channels may also be affected.

  When internal reference voltage (1.45 V) is selected reference voltage source for the + side of the A/D converter, do not input a voltage higher than the internal reference voltage to a pin selected by the ADS register. However, it is no problem that a voltage higher than the internal reference voltage is input to a pin not selected by the ADS register.

- **Noise countermeasures**

  To maintain the 10-bit resolution, attention must be paid to noise input to the AV_{REFP}, V_{DD}, ANIn pins.

  <1> Connect a capacitor with a low equivalent resistance and a good frequency response to the power supply.

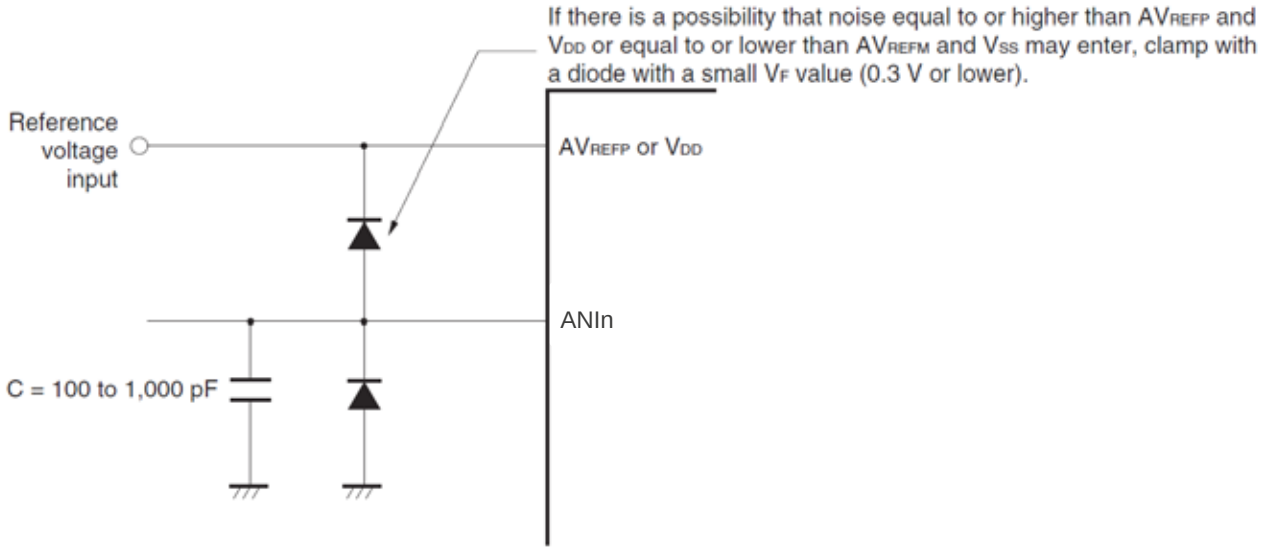
  <2> The higher the output impedance of the analog input source, the greater the influence. To reduce the noise, connecting external capacitor as shown in Figure 9 (next page) is recommended.

  <3> Do not switch these pins with other pins during conversion.

  <4> The accuracy is improved if the HALT mode is set immediately after the start of conversion.

CAUTION FOR A/D CONVERTER (2/3)

Figure 10: Analog input pin connection



- **Analog input pins (ANIn)**

  <1> The analog input pins (ANIn) are shared with input port pins.

  Do not change the output values for the shared port-pin functions while A/D conversion of the signals on the ANIn pins is selected and conversion is in progress, since doing so may lower the precision of the results of conversion.

  <2> When a pin adjacent to one on which A/D conversion is in progress is used as a digital I/O port pin, coupling may lead to noise that causes the results of A/D conversion to differ from the expected values. Be sure to prevent the input or output of pulses on such pins while conversion is in progress.

CAUTION FOR A/D CONVERTER (3/3)

- **Input impedance of analog input (ANIn) pins**

  This A/D converter charges a sampling capacitor for sampling during sampling time.

  Therefore, only a leakage current flows when sampling is not in progress, and a current that charges the capacitor flows during sampling. Consequently, the input impedance fluctuates depending on whether sampling is in progress, and on the other states.

  To make sure that sampling is effective, however, it is recommended to keep the output impedance of the analog input source to within 1 kΩ, and to connect a capacitor of about 100 pF to the ANIn pins (see Figure 10).

- **Internal equivalent circuit**

  The equivalent circuit of the analog input block is shown below.

Figure 11: Internal Equivalent Circuit on ANIn pin

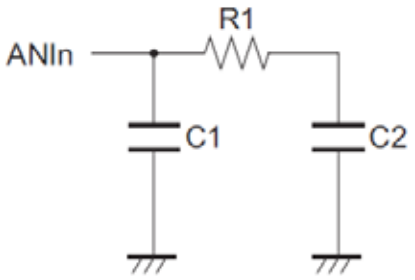


Table 10: Resistance and Capacitance Values of Equivalent Circuit (Reference Values)

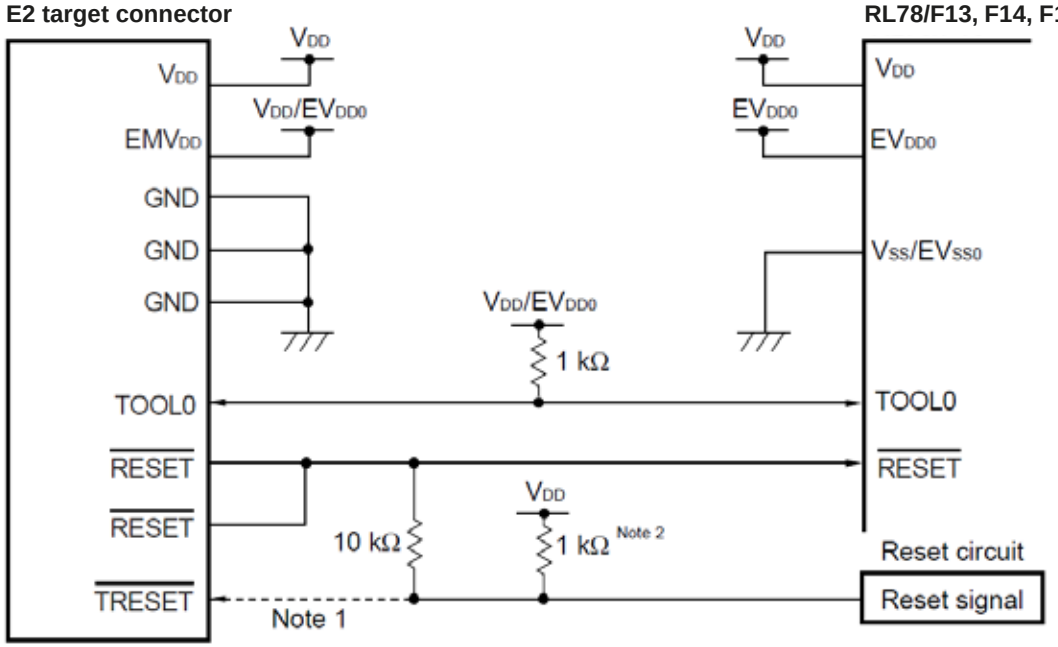
AV_{REFP}, V_{DD}	ANIn Pins	R1 [kΩ]	C1 [pF]	C2 [pF]
3.6 V ≤ V_{DD} ≤ 5.5 V	ANI0 to ANI23	14	8	2.5
	ANI24 to ANI30	18	8	7.0
2.7 V ≤ V_{DD} < 3.6 V	ANI0 to ANI23	39	8	2.5
	ANI24 to ANI30	53	8	7.0

Remark The resistance and capacitance values shown in Table are not guaranteed values.

DEBUG CIRCUIT

RL78/F13, F14, F15 uses the V_{DD}, EV_{DD0}, $\overline{RESET}$, TOOL0, and V_{SS} pins to communicate with the host machine via an E2 on-chip debugging emulator. Serial communication is performed by using a single-line UART that uses the TOOL0 pin. For detail, refer "E1/E20/E2 Emulator, E2 Emulator Lite Addional Document for User's Manual (Notes on Connection of RL78)" (Document No. R20UT1994EJ).

Figure 12: Connection Example of E2 On-chip Debugging Emulator and RL78/F13, F14, F15



Note 1. Connecting the dotted line is not necessary during flash programming.
Note 2. If the reset circuit on the target system does not have a buffer and generates a reset signal only with resistors and capacitors, this pull-up resistor is not necessary.

Caution This circuit diagram is assumed that the reset signal outputs from an N-ch O.D. buffer (output resistor: 100 Ω or less)

RELATED DOCUMENTS

Document Name	Document No.
RL78/F13, F14 User’s Manual: Hardware	R01UH0368E
RL78/F15 User’s Manual: Hardware	R01UH0559E
E1/E20/E2Emulator, E2 Emulator Lite Additional Document for User’s Manual (Notes on Connection of RL78)	R20UT1994E

REVISION HISTORY

Revision	Page	Items	Date
1.0	-	New Release	2021.09.30