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RENESAS

H8SX Family

DTC Block Transfer

Introduction

This application note describes using the data transfer controller (DTC) function to transfer five blocks of data, each comprising two bytes, and outputting the transferred data to I/O ports (P1 and P2).

The DTC block transfer function makes it possible to transfer data while bypassing the CPU. When a block area is specified as the transfer destination data area (or transfer source data area), the address register specified as the block area is restored to its initial state after transfer of each block completes.

Target Devices

- H8SX/1663 Group
- H8SX/1622 Group
- H8SX/1638 Group
- H8SX/1648 Group, H8SX/1648A Group, H8SX/1648L Group, H8SX/1648G Group, H8SX/1648H Group
- H8SX/1658R Group
- H8SX/1668R Group

Preface

This application note was prepared using the H8SX/1668R Group, one of the devices on which operation has been confirmed, as the basis.

This program can be used with other H8SX Family MCUs that have the same internal I/O registers as the devices on which operation has been confirmed. Check the latest version of the manual for any additions and modifications to functions.

Careful evaluation is recommended before using this application note.

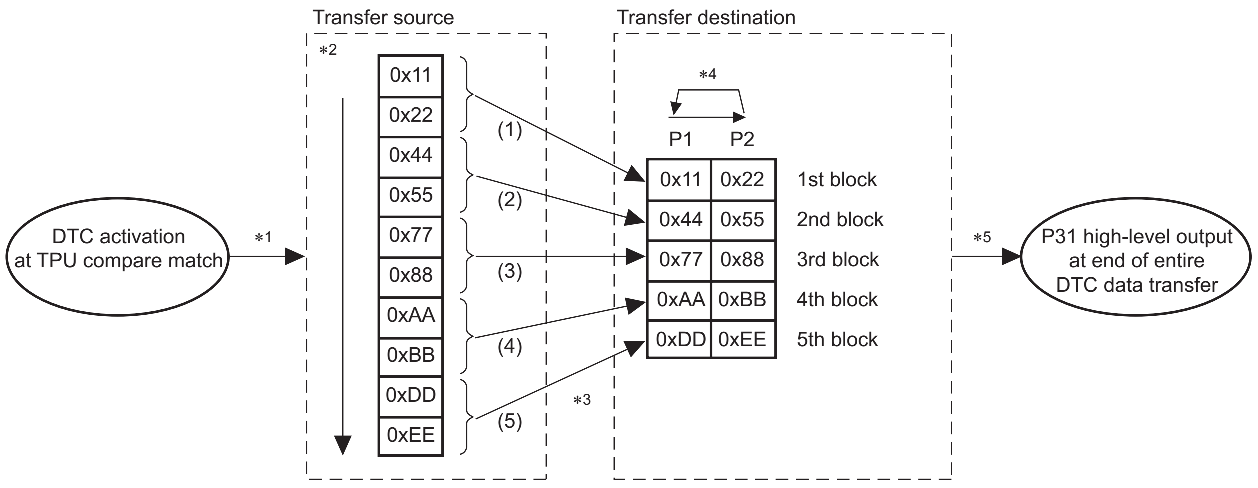
Contents

1. Specifications

The specifications of this application note cover using the data transfer controller (DTC) function to transfer five blocks of data, each comprising two bytes, and outputting the transferred data to I/O ports.

Figure 1 shows an overview of the operations described in this application note. The detailed specifications for the operations described in this application note are listed below.

- The 16-bit timer pulse unit (TPU) compare match A interrupt is set as the DTC activation source.
- The TPU period is set to 10 μsec.
- The DTC transfer data size is set to byte.
- The DTC total transfer size is set to 10 bytes (2 bytes × 5 blocks).
- After when the entire DTC data transfer completes, P31 is set to high level in the DTC transfer end interrupt handling routine.



Notes: 1. The compare match period is 10 μsec.
2. Incrementing of the transfer source address.
3. Transfer of 2-byte blocks of data are each 10 μsec. in sequence 1. to 5.
4. Transfer destination address specified as block area.
5. DTC transfer end interrupt generated after end of entire DTC data transfer.

Figure 1 Operation Overview

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description	
Operating frequency	Input clock:	12.5 MHz
	System clock (Iϕ):	50 MHz (12.5 MHz multiplied by 4)
	Peripheral module clock (Pϕ):	25 MHz (12.5 MHz multiplied by 2)
	External bus module clock (Bϕ):	50 MHz (12.5 MHz multiplied by 4)
Operating voltage	3.3V	
Operating mode	Mode 7 (MD3 = 0, MD2 = 1, MD1 = 1, MD0 = 1, MD_CLK = 0)	
Integrated development environment	High-performance Embedded Workshop Version 4.04.01.001	
C/C++ compiler	Renesas Technology H8 Family, H8S Family, and H8SX Family (V.6.02.00)	
Compile options	-cpu=H8SXA:24,-optimize=1	
Optimizing linkage editor	Renesas Technology Optimizing Linkage Editor (V.9.03.00)	
Linker options	-start = PResetPRG,PIntPRG/0400, P,C,C$DSEC,C$BSEC,D/0800, CDTCV/03560, B,R/0FF2000, S/0FFBE00	

3. Functions Used

3.1 Data Transfer Controller (DTC)

To use the DTC, the transfer data must be stored in the data area (RAM). When the DTC is activated, the transfer data is read from the data area (RAM) and transferred to the DTC's internal resource. After data transfer completes, the transfer data in the DTC's internal resource is written back to the data area (RAM). By preparing transfer data in the data area, it is possible to perform data transfer using any number of channels specified by the user. The supported transfer modes are normal transfer mode, repeat transfer mode, and block transfer mode. The transfer source address used by the DTC is specified in the source address register (SAR), and the transfer destination address is specified in the destination address register (DAR). After each transfer, SAR and DAR are independently incremented or decremented, or they remain fixed. The DTC transfer modes are shown in table 2.

Table 2 DTC Transfer Modes

Transfer Mode	Size of Data Transferred at One Transfer Request	Memory Address Increment or Decrement	Transfer Count
Normal	1 byte/word/longword	Incremented/decremented by 1, 2, or 4, or fixed	1 to 65536
Repeat*1	1 byte/word/longword	Incremented/decremented by 1, 2, or 4, or fixed	1 to 256*3
Block*2	Block size specified by CRAH (1 to 256 bytes/words/longwords)	Incremented/decremented by 1, 2, or 4, or fixed	1 to 65536

Notes: 1. Either source or destination is specified to repeat area.
2. Either source or destination is specified to block area.
3. After transfer of the specified transfer count, initial state is recovered to continue the operation.

3.2 Block Transfer Mode

In block transfer mode, one activation source causes one block of data to be transferred. Either the transfer source or the transfer destination is designated as a block area by the DTC transfer mode select (DTS) bit in the DTC mode register (MRB). The block size can be 1 to 256 bytes (or 1 to 256 words or 1 to 256 longwords). When the transfer of one block ends, the block size counter (CRAL) and address register (SAR when DTS = 1 or DAR when DTS = 0) specified as the block area are restored to their initial state. The other address register is consecutively incremented or decremented, or left fixed. From 1 to 65,536 transfers can be specified. An interrupt request to the CPU can be generated when transfer of the specified number of blocks ends. Table 3 lists the register functions in block transfer mode, and figure 2 shows the memory map in block transfer mode.

Table 3 Register Function in Block Transfer Mode

Register	Function	Written Back Value
SAR	Source address	DTS = 0: Incremented/decremented/fixed* DTS = 1: SAR initial value
DAR	Destination address	DTS = 0: DAR initial value DTS = 1: Incremented/decremented/fixed*
CRAH	Block size storage	CRAH
CRAL	Block size counter	CRAH
CRB	Block transfer counter	CRB – 1

Note: * Transfer information writeback is skipped.

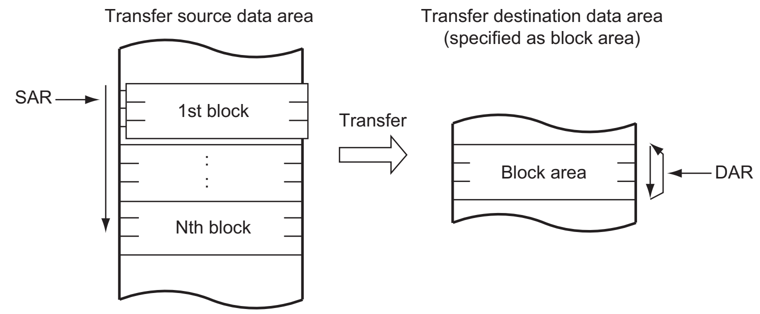


Figure 2 Memory Map in Block Transfer Mode
(When Transfer Destination is Specified as Block Area)

3.3 DTC Vector Table and Arrangement in Memory

Figure 3 shows the arrangement of the DTC vector table in memory (RAM). In this application note, the DTC transfer data is specified in short address mode, so the DTC mode register (MRA), SAR, MRB, DAR, DTC, DTC transfer counter register A (CRA), and DTC transfer counter register B (CRB) are arranged in order, starting from address H'FF5000.

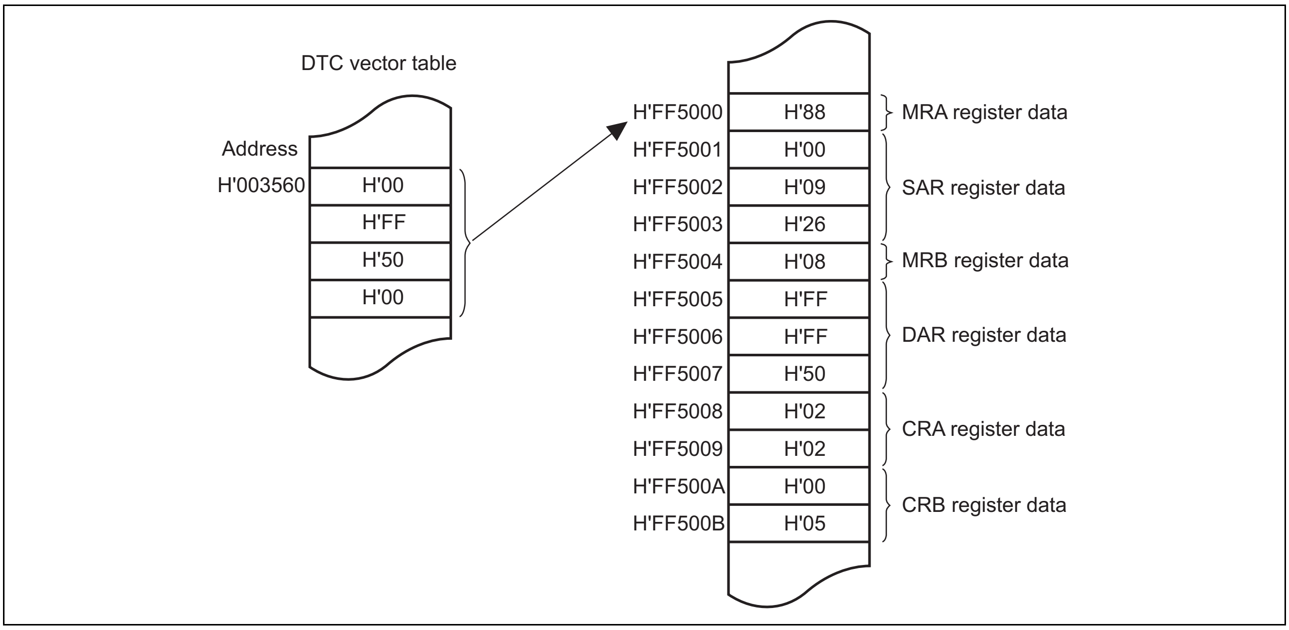
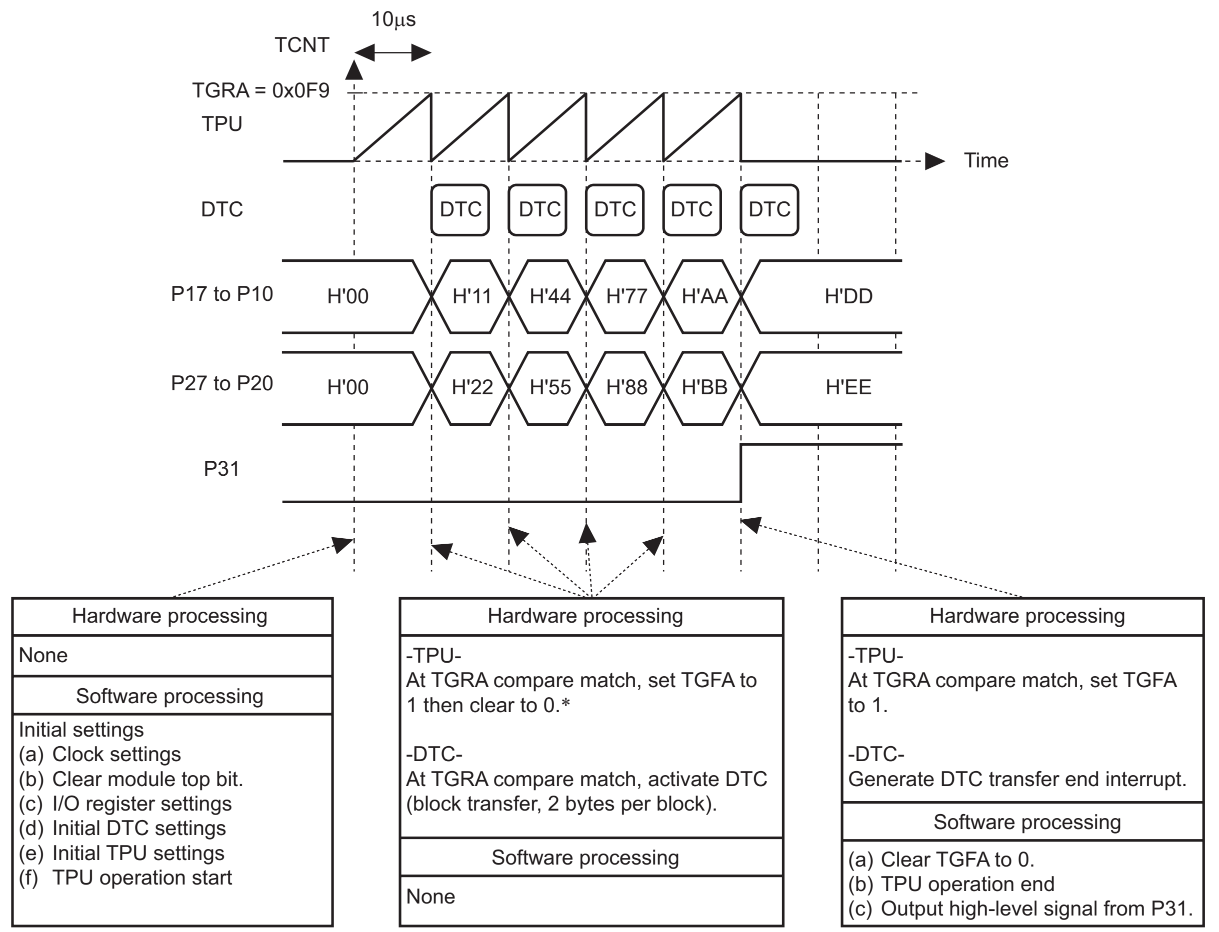


Figure 3 DTC Vector Table and Arrangement in Memory (Example of This Application Note)

4. Operation

Figure 4 shows the operation described in this application note.



Note: * TGFA is set to 1 when TCNT_0 = TGRA.
At this point, the DISEL bit in MRB of the DTC is cleared to 0, clearing the flag.

Figure 4 Operation

5. Software Description

5.1 Structures

Table 4 List of Structures

Type	Type	Variable Name	Type	Variable Name	No. of Bits	Description	Used by Functions
struct dtc_tag	union	R_mrasar	unsigned char	R_mra	8	MRA setting value	blkmn
			unsigned long	R_sar	32	SAR setting value	blkmn
	union	R_mrbdar	unsigned char	R_mrb	8	MRB setting value	blkmn
			unsigned long	R_dar	32	DAR setting value	blkmn
	unsigned short	R_cra	—	—	16	CRA setting value	blkmn
	unsigned short	R_crb	—	—	16	CRB setting value	blkmn

5.2 Symbolic Constants

Table 5 List of Symbolic Constants

Constant Name	Setting Value	Description	Used by Functions
TRINF	(*(volatile struct dtc_tag*)0xFF5000)	DTC register data start address (H'FF5000)	blkmn

5.3 ROM Variables

Table 6 List of ROM Variables

Type	Variable Name	Setting Value	Description	Used by Functions
const unsigned char	PATTBL[5][2]	H'11 , H'22 H'44 , H'55 H'77 , H'88 H'AA , H'BB H'DD , H'EE	Transfer data	blkmn
const unsigned long	dtcad	(unsigned long) &TRINF.R_mrasar.R_mra	DTC register data start address (H'FF500)	blkmn

5.4 List of Functions

Table 7 List of Functions

Function Name	Description
PowerON_Reset	• Initial settings function Initializes status pointer (SP), sets interrupt mask bits, sets uninitialized/initialized data, calls main function.
main	• Main function Calls block transfer initial settings function and starts TPU operation.
blkmn	• Block transfer initial settings function Makes clock settings, MSTP settings, I/O port output settings, TPU initial settings, and DTC initial settings.
INT_TGI0A_TPU0	• DTC transfer end interrupt function (activation source: TPU compare match A) Clears flag, stops TPU operation, and determines end of DTC block transfer.

5.5 Functions

5.5.1 PowerON_Reset Function

(1) Functional Overview

The PowerON_Reset function initializes the status pointer (SP) and uses embedded functions and standard library functions to set interrupt mask bits and set uninitialized/initialized data. Then it calls the main function.

(2) Arguments

None

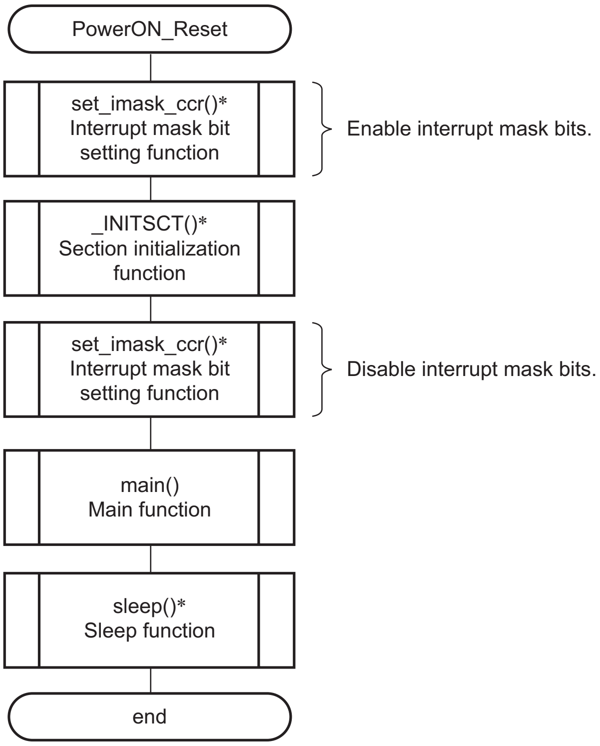
(3) Returned values

None

(4) Description of internal I/O registers used

None

(5) Flowchart



Notes: * • set_imask_ccr function: Embedded function
• _INITSCT function: Standard library function
• sleep function: Embedded function
For details, see 7., Reference Documents, Development Environment Manual.

Figure 5 Flowchart (PowerON_Reset)

5.5.2 main Function

(1) Functional Overview

The main function calls the block transfer initial settings function to make initial settings for DTC block transfer and starts TPU operation, which activates the DTC.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal registers used by this function are shown below. Note that the setting values shown are those used in this application note and differ from the initial values.

- Mode Control Register (MDCR) - Number of bits: 16, Address: H'FFFDC0

Bit	Bit Name	Set Value	R/W	Descriptions
15	MDS7	0	R	This pin indicates a value set with the mode pin (MD3)
11	MDS3	0	R	Mode Select 3 to 0
10	MDS2	1	R	These bits indicate the operating mode selected by the mode pins (MD2 to MD0).
9	MDS1	0	R	
8	MDS0	0	R	When MDCR is read, the signal levels input on pins MD2 to MD0 are latched into these bits.

- Timer Start Register (TSTR) - Number of bits: 8, Address: H'FFFFBC

Bit	Bit Name	Set Value	R/W	Descriptions
0	CST0	1	R/W	This bit select operation or stoppage for TCNT. 1: TCNT_0 performs count operation

(5) Flowchart

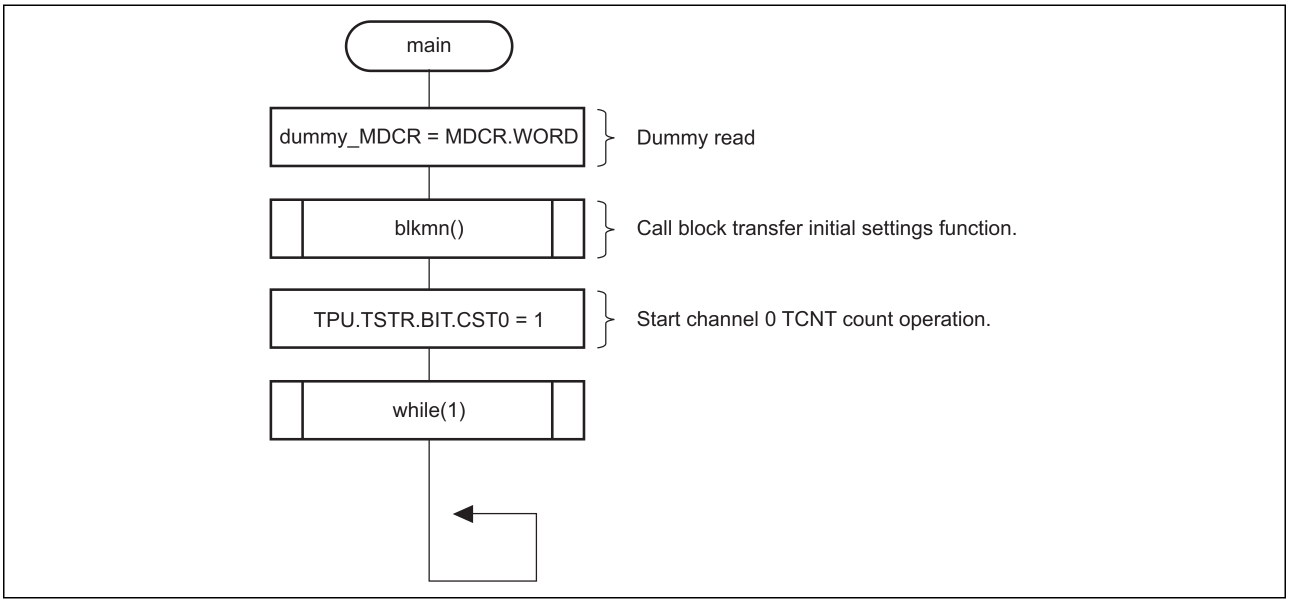


Figure 6 Flowchart (main Function)

5.5.3 blkmn Function

(1) Functional Overview

The blkmn function makes system clock settings, I/O port register initial settings, DTC initial settings, and TPU initial settings.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal registers used by this function are shown below. Note that the setting values shown are those used in this application note and differ from the initial values.

- System Clock Control Register (SCKCR) - Number of bits: 16, Address: H'FFFDC4

Bit	Bit Name	Set Value	R/W	Descriptions
10 9 8	ICK2 ICK1 ICK0	0 0 0	R/W R/W R/W	System Clock (Iϕ) Select These bits select the frequency of the system clock provided to the CPU, EXDMAC, DMAC, and DTC. The ratio to the input clock is as follows: 000: × 4
6 5 4	PCK2 PCK1 PCK0	0 0 1	R/W R/W R/W	Peripheral Module Clock (Pϕ) Select These bits select the frequency of the peripheral module clock. The ratio to the input clock is as follows: 001: × 2
2 1 0	BCK2 BCK1 BCK0	0 0 0	R/W R/W R/W	External Bus Clock (Bϕ) Select These bits select the frequency of the external bus clock. The ratio to the input clock is as follows: 000: × 4

- System Control Register (SYSCR) - Number of bits: 16, Address: H'FFFDC2

Bit	Bit Name	Set Value	R/W	Descriptions
1	DTCMD	1	R/W	DTC Mode Select Selects DTC operating mode. 1: DTC is in short address mode

- Module Stop Control Register A (MSTPCRA) - Number of bits: 16, Address: H'FFFDC8
MSTPCRA controls the module stop state. Setting a bit to 1 makes the corresponding module enter the module stop state, and clearing the bit to 0 clears the module stop state.

Bit	Bit Name	Set Value	R/W	Descriptions
12	MSTPA12	0	R/W	Data transfer controller (DTC)
0	MSTPA0	0	R/W	16-bit timer pulse unit (TPU channels 5 to 0)

- Data Direction Register (P1DDR) - Number of bits: 8, Address: H'FFFB80
- Data Direction Register (P2DDR) - Number of bits: 8, Address: H'FFFB81
- Data Direction Register (P3DDR) - Number of bits: 8, Address: H'FFFB82

  Function: The DDRs are 8-bit write-only registers whose bits specify the input or output status of the corresponding ports. Reading the DDRs has no effect and returns an undefined value. When the general I/O port function is selected, the corresponding pin functions as an output port when a bit in the DDRs is set to 1 and as an input port when cleared to 0.

  Setting values: P1DDR H'0xFF
  : P2DDR H'0xFF
  : P3DDR H'0x02

- Data Register (P1DR) - Number of bits: 8, Address: H'FFFF50
- Data Register (P2DR) - Number of bits: 8, Address: H'FFFF51
- Data Register (P3DR) - Number of bits: 8, Address: H'FFFF52

  Function: The DRs are 8-bit readable/writable registers that store output data for pins used as general output ports.

  Setting values: P1DR H'0x00
  : P2DR H'0x00
  : P3DR H'0x00

- DTC Vector Base Register (DTCVBR) - Number of bits: 32, Address: H'FFFD80

  Function: DTCVBR is a 32-bit register that specifies the base address for vector table address calculation. Bits 31 to 28 and bits 11 to 0 are fixed at 0 and writing to them has no effect. The initial value of DTCVBR is H'00000000.

  Setting value: H'00003000

- DTC Control Register (DTCCR) - Number of bits: 8, Address: H'FFFF30

Bit	Bit Name	Set Value	R/W	Descriptions
4	RRS	0	R/W	DTC Transfer Information Read Skip Enable Controls the vector address read and transfer information read. A DTC vector number is always compared with the vector number for the previous activation. If the vector numbers match and this bit is set to 1, the DTC data transfer is started without reading a vector address and transfer information. If the previous DTC activation is a chain transfer, the vector address read and transfer information read are always performed. 0: Transfer read skip is not performed.
3	RCHNE	0	R/W	Chain Transfer Enable After DTC Repeat Transfer Enables/disables the chain transfer while transfer counter (CRAL) is 0 in repeat transfer mode. In repeat transfer mode, the CRAH value is written to CRAL when CRAL is 0. Accordingly, chain transfer may not occur when CRAL is 0. If this bit is set to 1, the chain transfer is enabled when CRAH is written to CRAL. 0: Disables the chain transfer after repeat transfer

- DTC Source Address Register (SAR) - Number of bits: 32, Address: H'FF5001
  Function: SAR is a 32-bit register that designates the source address of data to be transferred by the DTC.
  SAR cannot be accessed directly by the CPU.
  Setting value: H'0009A6

- DTC Destination AddressRegister (DAR) - Number of bits: 32, Address: H'FF5005
  Function: DAR is a 32-bit register that designates the destination address of data to be transferred by the DTC. In short address mode, the lower 24 bits of DAR are valid and bits 31 to 24 are ignored. In this case, the upper eight bits are filled with the value specified by bit 23. DAR cannot be accessed directly by the CPU.
  Setting value: H'FFFF50

- DTC Mode Register A (MRA) - Number of bits: 8, Address: H'FF5000
  MRA selects DTC operating mode. MRA cannot be accessed directly by the CPU.

Bit	Bit Name	Set Value	R/W	Descriptions
7	MD1	1	R/W	Specify DTC transfer mode.
6	MD0	0	R/W	10: Block transfer mode
5	Sz1	0	R/W	Specify the size of data to be transferred.
4	Sz0	0	R/W	00: Byte-size transfer
3	SM1	1	R/W	Specify an SAR operation after a data transfer.
2	SM0	0	R/W	10: SAR is incremented after a transfer

- DTC Mode Register B (MRB) - Number of bits: 8, Address: H'FF5004
  MRB selects DTC operating mode. MRB cannot be accessed directly by the CPU.

Bit	Bit Name	Set Value	R/W	Descriptions
7	CHNE	0	R/W	DTC Chain Transfer Enable 0: Disables the chain transfer
6	CHNS	0	R/W	DTC Chain Transfer Select 0: Chain transfer every time
5	DISEL	0	R/W	DTC Interrupt Select When this bit is set to 1, a CPU interrupt request is generated every time after a data transfer ends.
4	DTS	0	R/W	DTC Transfer Mode Select 0: Specifies the destination as repeat or block area
3 2	DM1 DM0	1 0	R/W R/W	Destination Address Mode 1 and 0 Specify a DAR operation after a data transfer. 10: DAR is incremented after a transfer

- DTC Transfer Counter Register A (CRA) - Number of bits: 16, Address: H'FF5008
  Function: CRA is a 16-bit register that specifies the number of data transfers to be performed by the DTC. In block transfer mode, CRA is divided into two parts: the upper eight bits (CRAH) and the lower eight bits (CRAL). CRAH holds the block size, and CRAL functions as a block-size counter. CRA cannot be accessed directly by the CPU.
  Setting value: H'0202

- DTC Transfer Counter Register B (CRB) - Number of bits: 16, Address: H'FF500A
  Function: CRB is a 16-bit register that specifies the number of data transfers to be performed by the DTC in block transfer mode. It functions as a 16-bit transfer counter (1 to 65,536) and is decremented at each data transfer. When the counter value reaches H'0000, the DTCEn bit corresponding to the activation source is cleared and then an interrupt request to the CPU is generated. CRB cannot be accessed directly by the CPU.
  Setting value: H'0005

- DTC Enable Register (DTCERB) - Number of bits: 16, Address: H'FFFF22

Bit	Bit Name	Set Value	R/W	Descriptions
13	DTCERB13	1	R/W	DTC Activation Enable 15 to 0 Setting this bit to 1 specifies a relevant interrupt source to a DTC activation source. Activation source: TGI0A

- Timer Start Register (TSTR) - Number of bits: 8, Address: H'FFFFBC

Bit	Bit Name	Set Value	R/W	Descriptions
0	CST0	0	R/W	This bit selects operation or stoppage for TCNT. 0: TCNT0 count operation is stopped

- Timer Status Register (TSR) - Number of bits: 8, Address: H'FFFFC5

Bit	Bit Name	Set Value	R/W	Descriptions
7	TCFD	1	R	Count Direction Flag 1: TCNT counts up

- Timer Mode Register (TMDR) - Number of bits: 8, Address: H'FFFFC1

Bit	Bit Name	Set Value	R/W	Descriptions
3	MD3	0	R/W	Modes 3 to 0
2	MD2	0	R/W	Set the timer operating mode.
1	MD1	0	R/W	0000: Normal operation
0	MD0	0	R/W	

- Timer Control Register (TCR) - Number of bits: 8, Address: H'FFFFC0

Bit	Bit Name	Set Value	R/W	Descriptions
7	CCLR2	0	R/W	TCNT Counter Clear Source Select
6	CCLR1	0	R/W	001: TCNT cleared at TGRA compare match/input capture
5	CCLR0	1	R/W	
4	CKEG1	0	R/W	Input Clock Edge Select
3	CKEG0	0	R/W	00: Count at falling edge of internal clock
2	TPSC2	0	R/W	TCNT Counter Clock Select
1	TPSC1	0	R/W	000: Internal clock, count on Pϕ/1
0	TPSC0	0	R/W	

- Timer I/O Control Register (TIOR) - Number of bits: 8, Address: H'FFFFC2

Bit	Bit Name	Set Value	R/W	Descriptions
3	IOA3	0	R/W	TIOCA0 Pin Function
2	IOA2	0	R/W	0000: Output disabled
1	IOA1	0	R/W	
0	IOA0	0	R/W	

- Timer Synchronization Register (TSYR) - Number of bits: 8, Address: H'FFFFBD

Bit	Bit Name	Set Value	R/W	Descriptions
0	SYNC0	0	R/W	Timer Synchronization 0 This bit select whether operation is independent of or synchronized with other channels. 0: TCNT_0 operate independently. (TCNT presetting/clearing is unrelated to other channels.)

- Timer Interrupt Enable Register (TIER) - Number of bits: 8, Address: H'FFFFC4

Bit	Bit Name	Set Value	R/W	Descriptions
0	TGIEA	1	R/W	TGR Interrupt Enable A 1: Interrupt requests (TGIA) by TGFA bit enabled

- Timer General Register A_0 (TGRA_0) - Number of bits: 16, Address: H'FFFFC8
  Function: TGRA_0 is a 16-bit readable/writable register what functions as both an output compare and an input capture register. It cannot be accessed in 8-bit units. Always access TGRA_0 in 16-bit units.
  Setting value: H'00F9
- Timer Counter (TCNT) - Number of bits: 16, Address: H'FFFFC6
  Function: TCNT is a 16-bit readable/writable counter. There are six TCNT counters, one for each channel. TCNT is initialized to H'0000 after a reset or in hardware standby mode. It cannot be accessed in 8-bit units. Always access TCNT in 16-bit units.
  Setting value: H'0000

(5) Flowchart

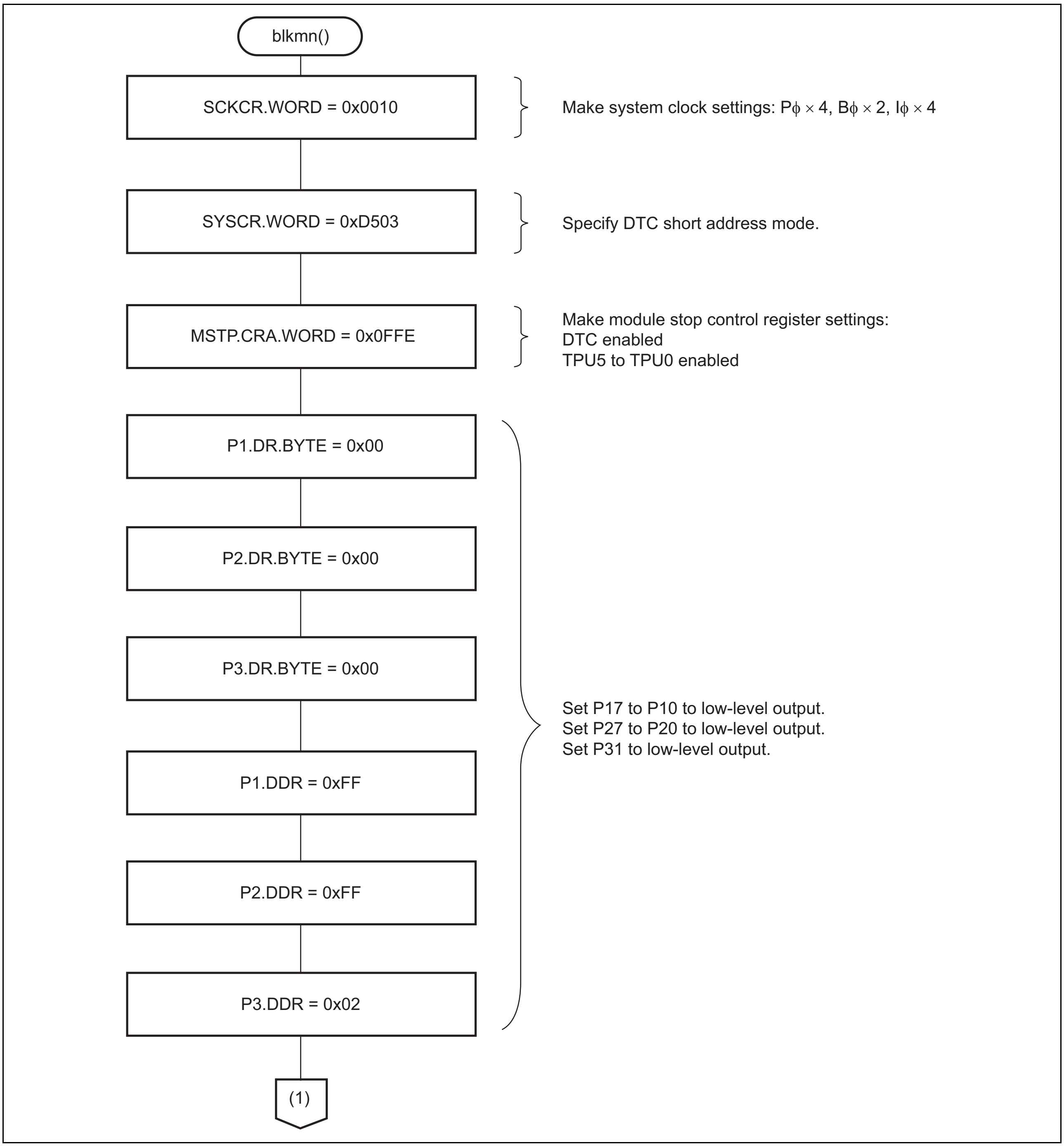
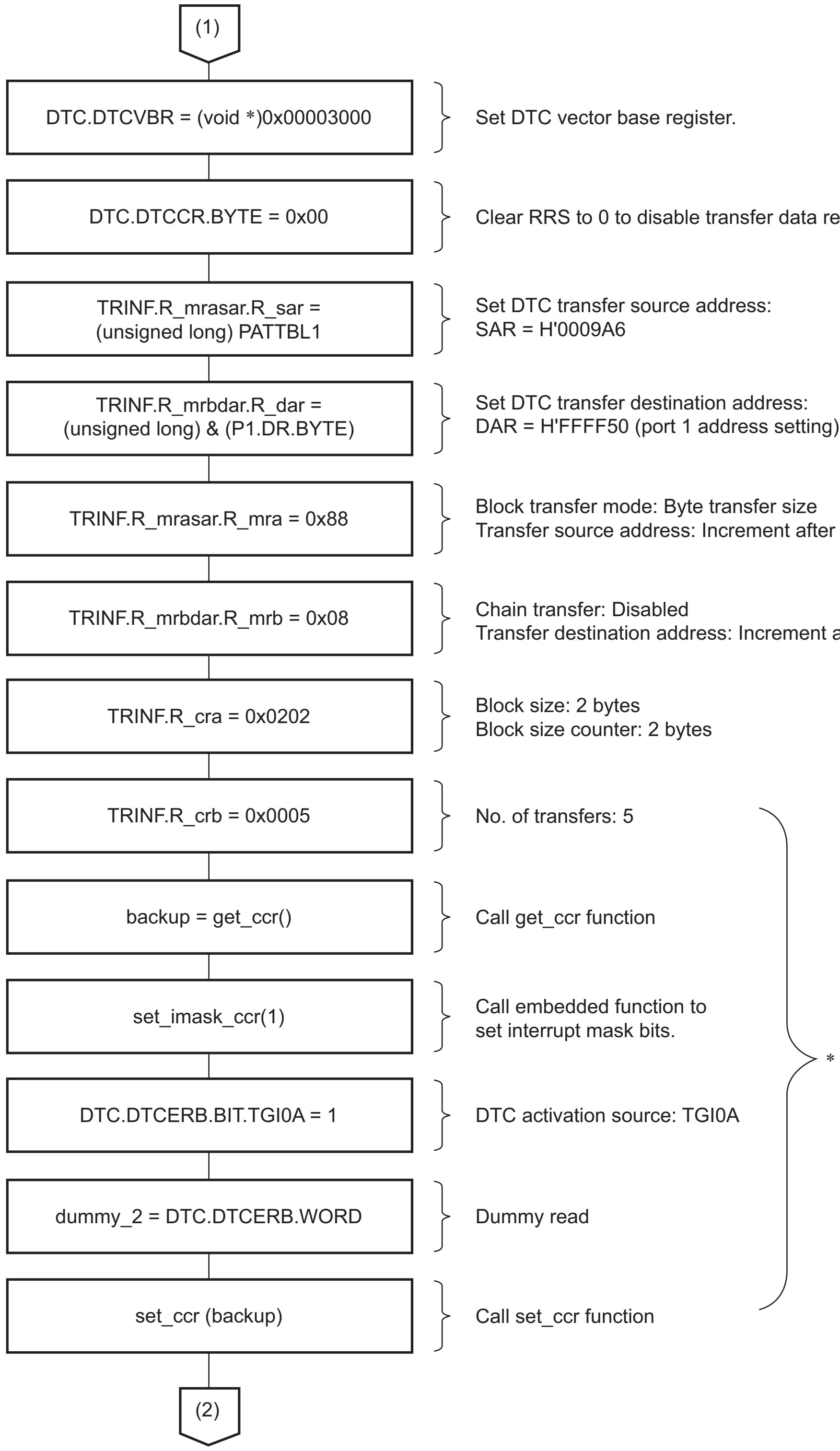


Figure 7 Flowchart (blkmn Function-1.)



Note: * See 6, Notes.

Figure 8 Flowchart (blkmn Function-2.)

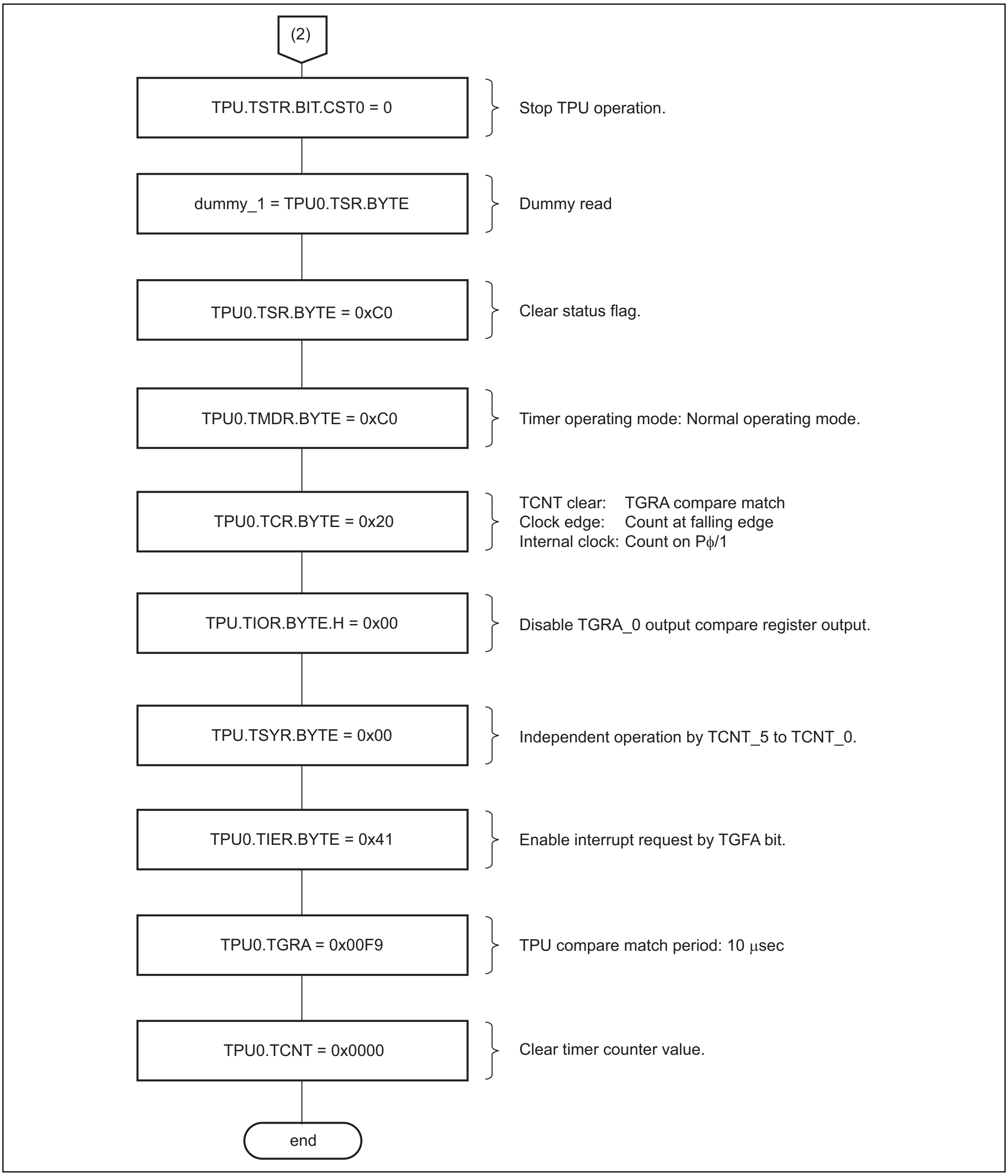


Figure 9 Flowchart (blkmn Function-3.)

5.5.4 DTC End Interrupt Function

(1) Functional Overview

The DTC end interrupt function disables TGI0A compare match output as the activation source for DTC block transfers.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal registers used by this function are shown below. Note that the setting values shown are those used in this application note and differ from the initial values.

- Timer Status Register (TSR) - Number of bits: 8, Address: H'FFFFC5

Bit	Bit Name	Set Value	R/W	Descriptions
0	TGFA	0	R/W	Output Compare Flag A Status flag that indicates the occurrence of TGRA compare match. [Clearing conditions] When DTC is activated by a TGIA interrupt while the DISEL bit in MRB of DTC is 0

- Timer Start Register (TSTR) - Number of bits: 8, Address: H'FFFFBC

Bit	Bit Name	Set Value	R/W	Descriptions
0	CST0	0	R/W	This bit selects operation or stoppage for TCNT. 0: TCNT0 count operation is stopped

(5) Flowchart

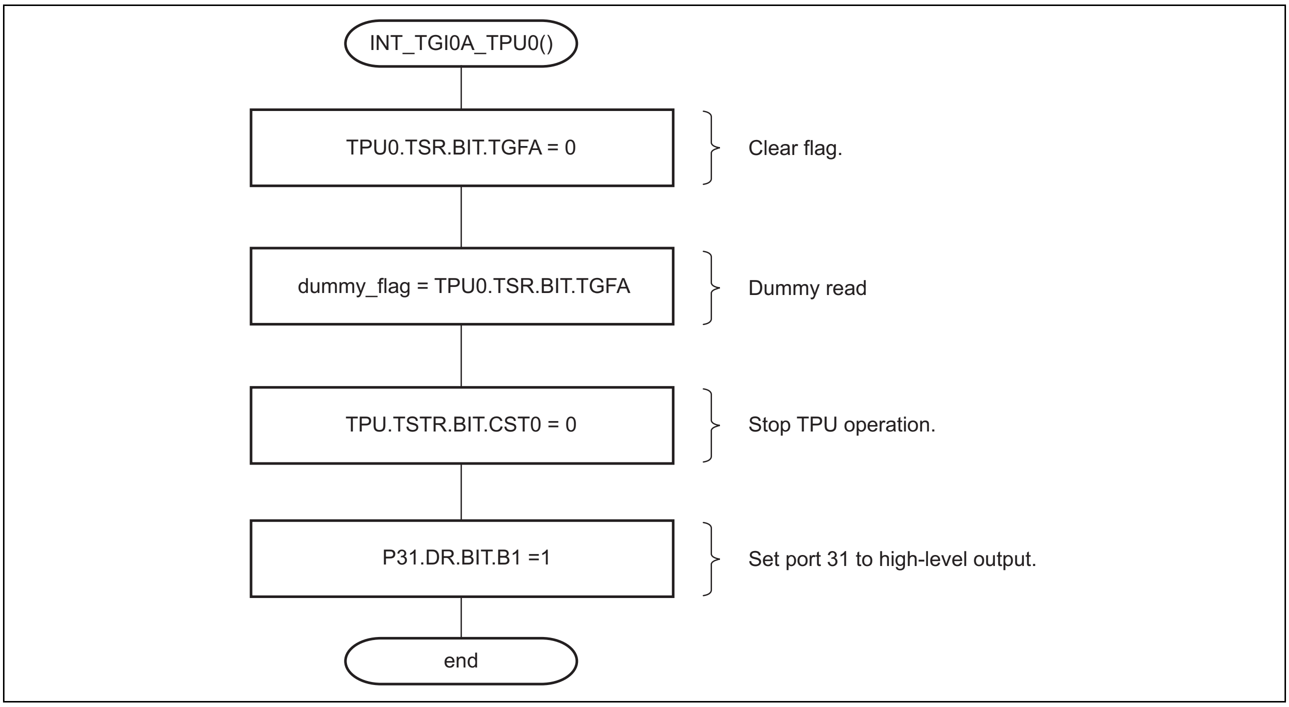


Figure 10 Flowchart (DTC End Interrupt)

6. Notes

When a conflict occurs between an overwrite (setting to 1 or 0) of the DTC enable register (DTCER) and the generation of a DTC activation source interrupt, activation of the DTC and interrupt exception processing by the CPU may both occur at the same time. In some cases, two interrupts may be generated at once. If there is a possibility of conflict between an overwrite of DTCER and generation of a DTC activation source interrupt, mask the interrupt when writing to DTCER. For details, see the relevant hardware manual or technical news/technical update.

7. Reference Documents

- Hardware Manuals
  H8SX/1668R Group Hardware Manual
  H8SX/1658R Group Hardware Manual
  H8SX/1663 Group Hardware Manual
  H8SX/1648, H8SX/1648A, H8SX/1648L, H8SX/1648G, H8SX/1648H Group Hardware Manual
  H8SX/1638 Group Hardware Manual
  H8SX/1622 Group Hardware Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Development Environment Manual
  H8S/300, H8/300 Series C/C++ Compiler Package User's Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
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