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Application Note

16

H8S/2655 Interface Volume

Application Note

Renesas Microcomputer

Renesas Electronics
www.renesas.com

Rev.1.0 1998.09

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Preface

The H8S/2600 Series comprises Hitachi's original high-performance 16-bit microcomputers with a high-speed H8S/2600 CPU core, upward-compatible with the H8/300 and H8/300H CPUs, and peripheral functions ideally suited to embedded systems for industrial applications.

In addition to the CPU, these microcomputers include RAM, a DMA controller, a bus controller, timers, and an SCI on a single chip, allowing them to be used in a wide range of application systems, both large and small.

This H8S/2655 Application Note (Interface Volume) includes examples of interfaces between the H8S/2655 and peripheral chips, and is intended as a reference manual for use during the user's hardware design process.

The operation of the sample tasks in this Application Note has been checked, but correct operation must be reconfirmed before using any of these examples in an actual application system.

Contents

Section 1 Using the H8S/2655 Application Note

1.1 Organization of Interface Examples

This volume explains how to interface the H8S/2655 to peripheral chips (such as ROM and RAM). Each example in the interface volume is organized as shown in figure 1.1.

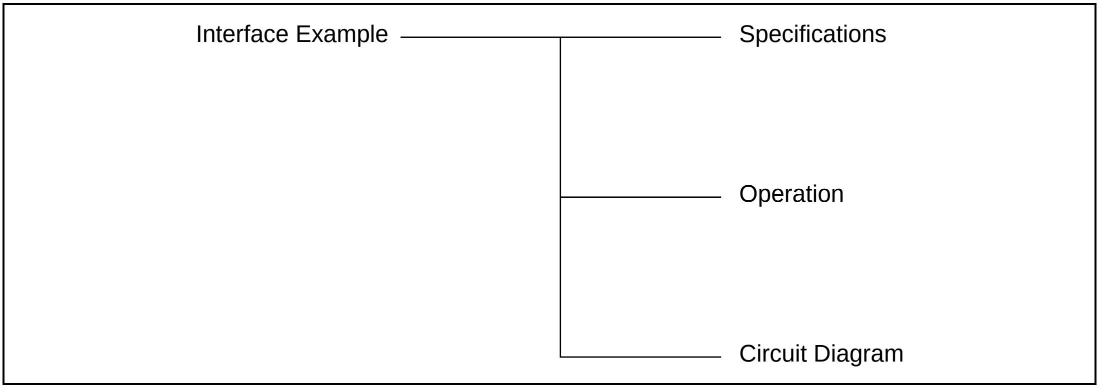


Figure 1.1 Organization of Interface Examples

Specifications: The name of the peripheral chip to be connected, a memory map, and other circuit specifications

Operation: Description of circuit operation, using timing charts

Circuit Diagram: A circuit diagram of the interface to the peripheral chip

Section 2 Bus Control Functions

2.1 Bus Controller

In the H8S/2655, the operating mode is selected from modes 1 to 7 by means of the mode pins. The address space is 64 kbytes in modes 1 to 3 (normal modes) and 16 Mbytes in modes 4 to 7 (advanced modes).

The bus controller manages the advanced mode 16-Mbyte space as eight areas, in 128-kbyte or 2-Mbyte units. The areas are numbered 0 to 7, in low-to-high address order, and the access data bus width and number of access states can be set independently for each area. It is also possible to extend bus cycles by inserting wait states in order to interface to low-speed external devices.

Settings for the access data bus width, number of access states, and so on, can be made by software in the bus width control register (ABWCR), access state control register (ASTCR), and other registers in the bus controller. The functions of these registers are shown below.

2.1.1 Bus Width Control Register (ABWCR)

ABWCR is an 8-bit readable/writable register that designates each area as either an 8-bit data bus access space or a 16-bit data bus access space. Bit 0 corresponds to area 0, and settings for areas 0 to 7 are made in bits 0 to 7. Clearing a bit to 0 designates the corresponding area as a 16-bit data bus access space, while setting a bit to 1 designates the corresponding area as an 8-bit data bus access space.

ABWCR	ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0
Modes 1–3, 5–7								
Initial value	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Mode 4								
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

0: Corresponding area is designated as 16-bit data bus access space.
1: Corresponding area is designated as 8-bit data bus access space.

2.1.2 Access State Control Register (ASTCR)

ASTCR is an 8-bit readable/writable register that designates each area as either a 2-state access space or a 3-state access space. Bit 0 corresponds to area 0, and settings for areas 0 to 7 are made in bits 0 to 7. Clearing a bit to 0 designates the corresponding area as a 2-state access space, while setting a bit to 1 designates the corresponding area as a 3-state access space. With a DRAM or pseudo-SRAM interface (set with bits RMTS2–RMTS0 in BCRH), the basic number of access states is 4, so ASTCR selects enabling or disabling of wait state insertion for the corresponding DRAM space.

ASTCR	AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0
Initial value	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- 0: Corresponding area is designated as 2-state access space. (Wait state insertion in DRAM/pseudo-SRAM space access is disabled.)
- 1: Corresponding area is designated as 3-state access space. (Wait state insertion in DRAM/pseudo-SRAM space access is enabled.)

2.1.3 Wait Control Registers H and L (WCRH, WCRL)

WCRH and WCRL are 8-bit readable/writable registers that select the number of program wait states for each area. Two bits are used to make the setting for one area.

1. WCRH

WCRH	W71	W70	W61	W60	W51	W50	W41	W40
Initial value	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Area 7		Area 6		Area 5		Area 4	

1. WCRL

WCRL	W31	W30	W21	W20	W11	W10	W01	W00
Initial value	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	Area 3		Area 2		Area 1		Area 0	

Wn1	Wn0	Description
0	0	Program wait not inserted in access to corresponding external space area
	1	1 program wait state inserted in access to corresponding external space area
1	0	2 program wait states inserted in access to corresponding external space area
	1	3 program wait states inserted in access to corresponding external space area

2.1.4 Bus Control Register H (BCRH)

BCRH is an 8-bit readable/writable register that selects enables or disables idle cycle insertion, and selects the memory to be connected to area 0 and areas 2 to 5.

BCRH	ICIS1	ICIS0	BRSTRM	BRSTS1	BRSTS0	RMTS2	RMTS1	RMTS0
Initial value	1	1	0	1	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<table>
<tr><th>RMTS2</th><th>RMTS1</th><th>RMTS0</th><th>Area 5</th><th>Area 4</th><th>Area 3</th><th>Area 2</th></tr>
<tr><td rowspan="4">0</td><td rowspan="2">0</td><td>0</td><td colspan="4">Ordinary space</td></tr>
<tr><td>1</td><td colspan="3">Ordinary space</td><td>DRAM space</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td colspan="2">Ordinary space</td><td colspan="2">DRAM space</td></tr>
<tr><td>1</td><td colspan="4">DRAM space</td></tr>
<tr><td rowspan="4">1</td><td rowspan="2">0</td><td>0</td><td colspan="4">Ordinary space</td></tr>
<tr><td>1</td><td colspan="3">Ordinary space</td><td>Pseudo-SRAM space</td></tr>
<tr><td rowspan="2">1</td><td>0</td><td colspan="2">Ordinary space</td><td colspan="2">Pseudo-SRAM space</td></tr>
<tr><td>1</td><td colspan="4">Pseudo-SRAM space</td></tr>
</table>

Valid only for burst ROM interface

BRSTS0	Description
0	Burst cycle comprises 1 state
1	Burst cycle comprises 2 states

Valid only for burst ROM interface

BRSTS1	Description
0	Max. 4 words in burst access
1	Max. 8 words in burst access

BRSTRM	Description
0	Area 0 is basic bus interface space
1	Area 0 is burst ROM interface space

ICIS0	Description
0	Idle cycle not inserted in case of consecutive read and write cycles in external space
1	Idle cycle inserted in case of consecutive read and write cycles in external space

ICIS1	Description
0	Idle cycle not inserted in case of consecutive read cycles in different external space areas
1	Idle cycle inserted in case of consecutive read cycles in different external space areas

2.1.5 Bus Control Register L (BCRL)

BCRL is an 8-bit readable/writable register that enables or disables external bus release, performs selection of the area partition unit, $\overline{\text{LCAS}}$ signal selection, and DMAC single address transfer selection, enables or disables the write data buffer function, and enables or disables $\overline{\text{WAIT}}$ pin input.

BCRL	BRLE	BREQOE	EAE	LCASS	DDS	ASS	WDBE	WAITE
Initial value	0	0	1	1	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

WAITE	Description
0	Wait input by $\overline{\text{WAIT}}$ pin disabled ($\overline{\text{WAIT}}$ pin can be used as I/O port)
1	Wait input by $\overline{\text{WAIT}}$ pin enabled

WDBE	Description
0	Write data buffer function not used
1	Write data buffer function used

ASS	Description
0	Area partition unit is 128 kbytes
1	Area partition unit is 2 Mbytes

DDS	Description
0	Full access always executed when performing DMAC single address transfer involving DRAM/pseudo-SRAM space
1	Burst access also possible when performing DMAC single address transfer involving DRAM/pseudo-SRAM space

LCASS	Description
0	$\overline{\text{LCAS}}$ pin used for $\overline{\text{LCAS}}$ signal in 2-CAS DRAM interface ($\overline{\text{BREQO}}$ output and $\overline{\text{WAIT}}$ input cannot be used)
1	$\overline{\text{LWR}}$ pin used for $\overline{\text{LCAS}}$ signal in 2-CAS DRAM interface (RAS down mode cannot be used)

EAE	Description
0	Addresses H'01000–H'01FFFF are on-chip ROM
1	Addresses H'01000–H'01FFFF are external address space (mode 6) or a reserved area (mode 7)

BREQOE	Description
0	$\overline{\text{BREQO}}$ output disabled ($\overline{\text{BREQO}}$ can be used as I/O port)
1	$\overline{\text{BREQO}}$ output enabled

BRLE	Description
0	External bus release disabled ($\overline{\text{BREQ}}$, $\overline{\text{BACK}}$, and $\overline{\text{BREQO}}$ can be used as I/O ports)
1	External bus release enabled

2.1.6 Memory Control Register (MCR)

MCR is an 8-bit readable/writable register that selects the DRAM strobe control method, number of precharge cycles, access mode, address multiplexing shift size, and the number of wait states inserted during refreshing, when areas 2 to 5 are designated as DRAM interface space.

When areas 2 to 5 are designated as pseudo-SRAM interface space, MCR selects the number of precharge cycles and the access mode.

MCR	TPC	BE	RCDM	CW2	MXC1	MXC0	RLW1	RLW0
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Valid only for DRAM interface

RLW1	RLW0	Description (CAS-before-RAS refresh cycle)
0	0	No wait state inserted
	1	1 wait state inserted
1	0	2 wait states inserted
	1	3 wait states inserted

Valid only for DRAM interface

MXC1	MXC0	Shift Size	8-Bit Access	16-Bit Access
0	0	8-bit shift	Row address = A_{23}–A_8	Row address = A_{23}–A_9
	1	9-bit shift	Row address = A_{23}–A_9	Row address = A_{23}–A_{10}
1	0	10-bit shift	Row address = A_{23}–A_{10}	Row address = A_{23}–A_{11}
	1	—	—	—

Valid only for DRAM interface

CW2	Description
0	2-CAS method selected ($\overline{\text{CASH}}$, $\overline{\text{CASL}}$, $\overline{\text{WE}}$ signals enabled)
1	2-WE method selected ($\overline{\text{CAS}}$, $\overline{\text{UWE}}$, $\overline{\text{LUE}}$ signals enabled)

Valid only for DRAM interface

RCDM	Description
0	RAS up mode (If DRAM access is interrupted, RAS signal remains low while waiting for next DRAM access)
1	RAS down mode (If DRAM access is interrupted, RAS signal is returned to high level)

Valid only for DRAM and pseudo-SRAM interfaces

BE	Description
0	Burst disabled (always full access)
1	Burst access enabled (For DRAM space access, fast page mode) (For pseudo-SRAM space access, static column mode)

Valid only for DRAM and pseudo-SRAM interfaces

TPC	Description
0	1-state precharge cycle is inserted
1	2-state precharge cycle is inserted

2.1.7 DRAM Control Register (DRAMCR)

DRAMCR is an 8-bit readable/writable register that selects the DRAM or pseudo-SRAM refresh mode and refresh counter clock and controls the refresh timer.

DRAMCR	RFSHE	RCW	RMODE	CMF	CMIE	CKS2	CKS1	CKS0
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

CKS2	CKS1	CKS0	Description (Selection of clock for input to RTCNT from internal clocks)
0	0	0	Count operation stopped
		1	Count uses ϕ/2
	1	0	Count uses ϕ/8
		1	Count uses ϕ/32
1	0	0	Count uses ϕ/128
		1	Count uses ϕ/512
	1	0	Count uses ϕ/2048
		1	Count uses ϕ/4096

CMIE	Description
0	Interrupt request (CMI) by CMF flag disabled
1	Interrupt request (CMI) by CMF flag enabled

CMF	Description
Clear to 0	0 can be written to CMF flag after reading CMF = 1
Set to 1	CMF flag is set to 1 when RTCNT = RTCOR

RMODE	DRAM Interface	Pseudo-SRAM Interface
0	CAS-before-RAS refreshing	Auto-refreshing
1	Self-refreshing	Self-refreshing

RCW	Description (CAS-before-RAS Refreshing)
0	Wait state insertion disabled (For pseudo-SRAM interface, clear to 0)
1	1 wait state inserted

RFSHE	Description
0	Refresh control not performed
1	Refresh control performed

2.1.8 Refresh Timer Counter (RTCNT)

RTCNT is an 8-bit readable/writable up-counter that counts up using the internal clock selected by bits CKS2–CKS0 in DRAMCR.

If refresh control is selected (RFSHE = 1), when RTCNT matches RTCOR the CMF flag is set to 1 and a refresh cycle is started. At the same time, RTCNT is cleared to H'00.

RTCNT								
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

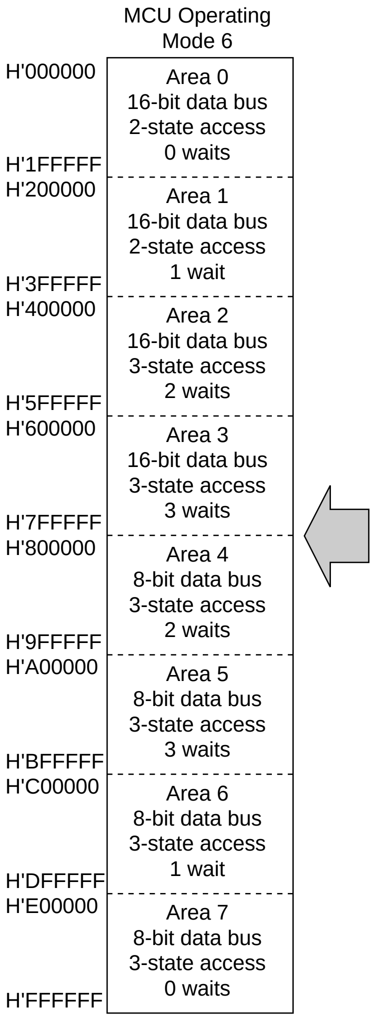
2.1.9 Refresh Time Control Register (RTCOR)

RTCOR is an 8-bit readable/writable register that sets the period for compare match operations with RTCNT.

RTCOR								
Initial value	1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

2.2 Sample Bus Controller Settings

For the area map used in the interface examples in this Application Note, settings for each area are made in the various bus controller registers as shown in figure 2.2.1.



Registe Name	Set Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ABWCR	H'F4	1	1	1	1	0	0	0	0
ASTCR	H'75	1	1	1	1	1	1	0	0
WCRH	H'1B	0	0	0	1	1	0	1	1
WCRL	H'B4	1	0	1	1	0	1	0	0

Figure 2.2.1 Area Map

Examples of the register settings used for area designation in the interface examples in this Application Note are shown below.

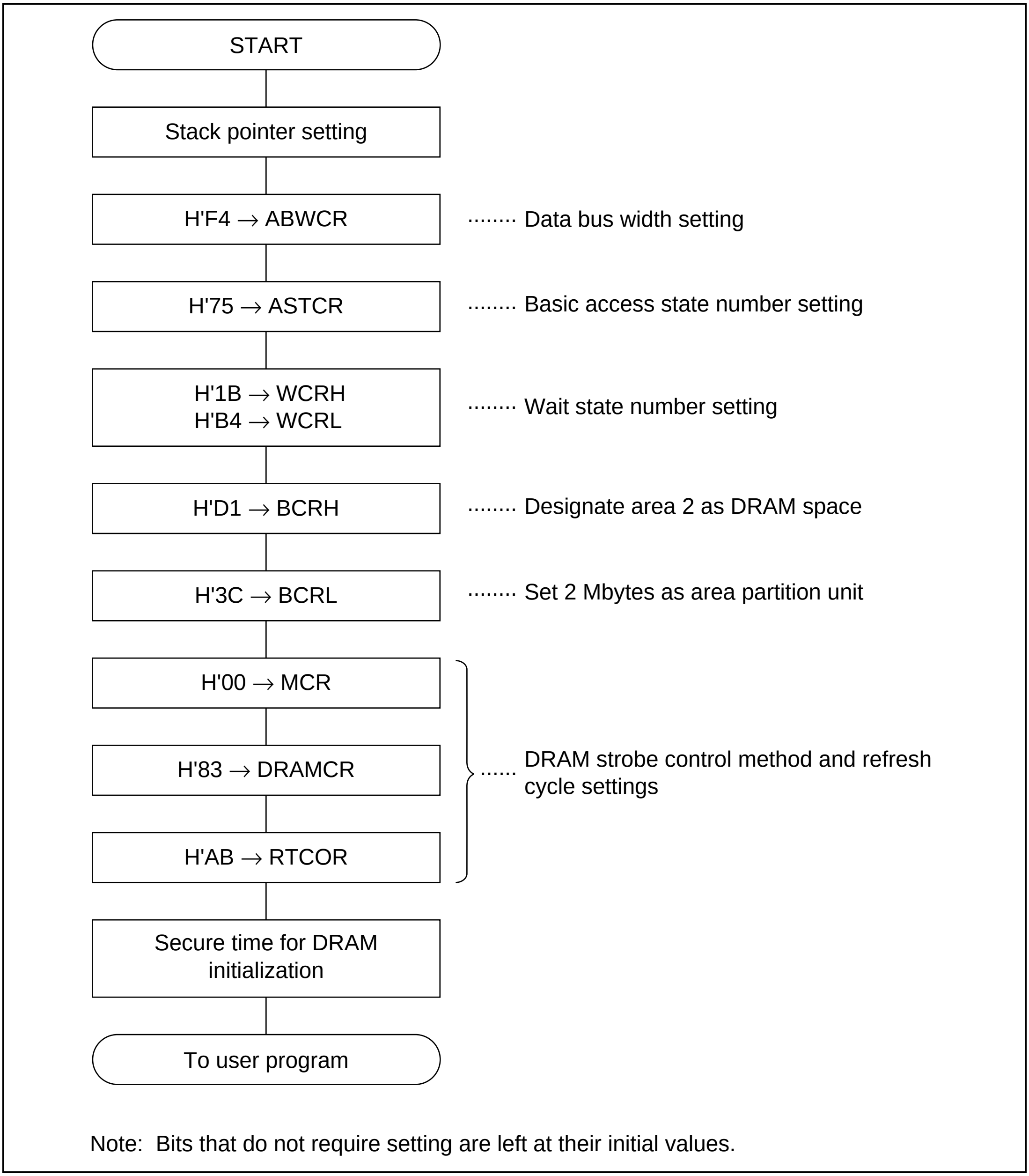


Figure 2.2.2 Sample Register Settings for Area Designation

3.1 EPROM (HN27C101AG-10) Interface Using 8-Bit Bus Mode

EPROM (HN27C101AG-10) Interface	MCU: H8S/2655	Functions Used: Mode 5 (8-Bit Bus Mode)

Specifications

1. Figure 3.1.1 (a) shows an example of the connection between an H8S/2655 and ×8-bit configuration EPROM (HN27C101AG-10). The H8S/2655 is set to mode 5 8-bit bus mode, and the EPROM is allocated to area 0.

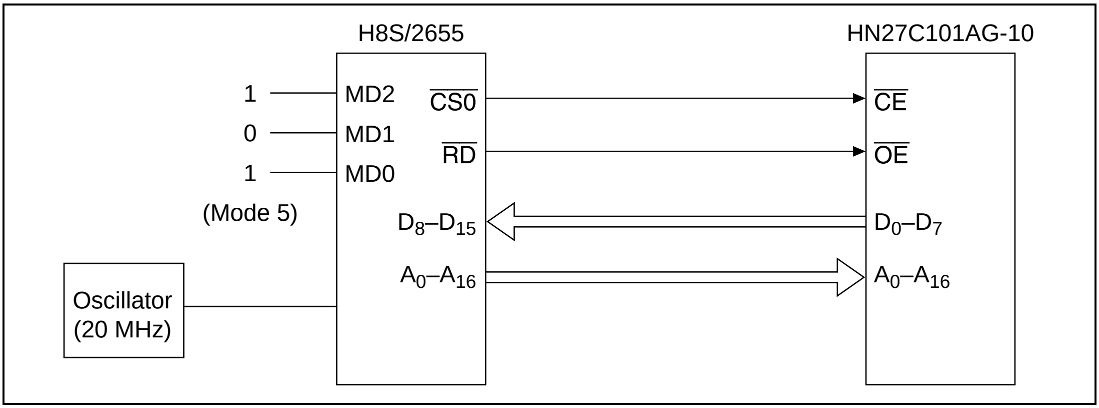


Figure 3.1.1 (a) Example of Connection between H8S/2655 and EPROM

2. Figure 3.1.1 (b) shows the memory map. When the 16-Mbyte address space is divided into areas in 2-Mbyte units, the EPROM area is H'00 0000–H'01 FFFF.

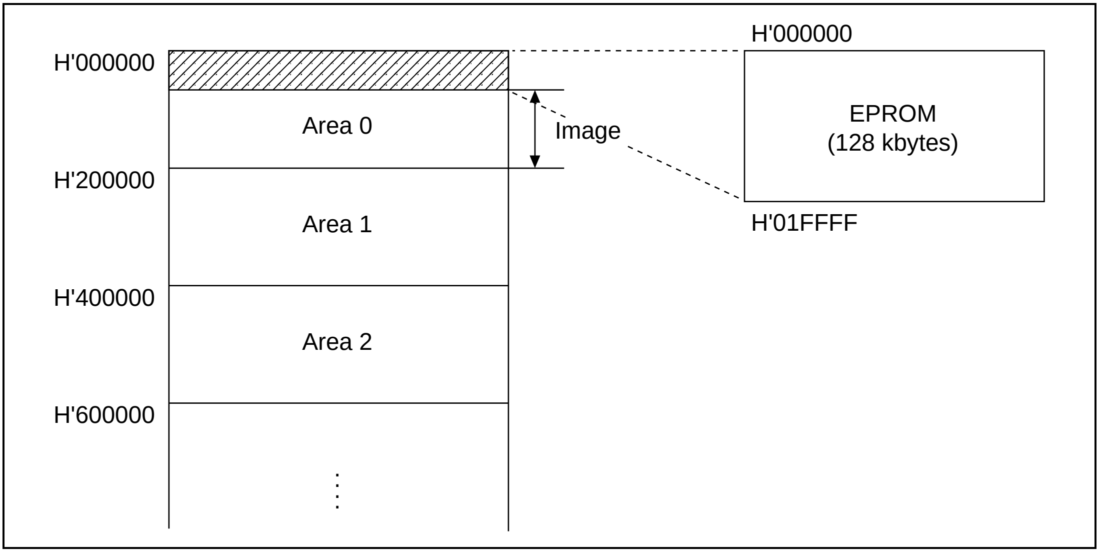


Figure 3.1.1 (b) Memory Map

3. Table 3.1.1 (a) shows the bus controller settings.

Table 3.1.1 (a) Bus Controller Settings

Name	Abbrev.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Setting
Bus width control register	ABWCR	ABW7 *	ABW6 *	ABW5 *	ABW4 *	ABW3 *	ABW2 *	ABW1 *	ABW0 1	Area 0: 8-bit access space
Access state control register	ASTCR	AST7 *	AST6 *	AST5 *	AST4 *	AST3 *	AST2 *	AST1 *	AST0 1	Area 0: 3-state access space
Wait control register H	WCRH	W71 *	W70 *	W61 *	W60 *	W51 *	W50 *	W41 *	W40 *	—
Wait control register L	WCRL	W31 *	W30 *	W21 *	W20 *	W11 *	W10 *	W01 0	W00 0	Area 0: No program wait inserted
Bus control register H	BCRH	ICIS1 *	ICIS0 *	BRSTRM 0	BRSTS1 *	BRSTS0 *	RMTS2 *	RMTS1 *	RMTS0 *	Area 0: Basic bus interface
Bus control register L	BCRL	BRLE *	BREQOE *	EAE *	LCASS *	DDS *	ASS 1	WDBE *	WAITE *	Area partition unit: 2 Mbytes (16 Mbytes)
Memory control register	MCR	TPC *	BE *	RCDM *	CW2 *	MXC1 *	MXC0 *	RLW1 *	RLW0 *	—
DRAM control register	DRAMCR	RFSHE *	RCW *	RMODE *	CMF *	CMIE *	CKS2 *	CKS1 *	CKS0 *	—
Refresh time constant register	RTCOR	*	*	*	*	*	*	*	*	—

*: Don't care

Operation

The calculations used to check whether the AC characteristics are satisfied in EPROM access are shown below. The t_{cyc} value, unspecified min value, and unspecified max value are as follows.

- t_{cyc}: 50 ns (20 MHz oscillator (= ϕ))
- Unspecified min value: 0 ns
- Unspecified max value: min value

In the times obtained based on ϕ, the reference timing is shown in [ ].

For the timing values, see 2. AC Characteristics below.

1. Read Access

   Figure 3.1.1 (c) shows the EPROM read timing chart.

   Confirm that the following AC characteristics are satisfied.

Item		Symbol
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}

a. H8S/2655 t_{RDS}

i. When address is critical

- Setup time calculation [$T_{1\text{-}1}$ rise]

  $3\ t_{cyc} - t_{AD\ (max)} - t_{ACC\ (max)} = 30\ ns \geq 15\ ns\ (t_{RDS})$

ii. When CS is critical

- Setup time calculation [$T_{1\text{-}1}$ rise]

  $3\ t_{cyc} - t_{CSD1\ (max)} - t_{CE\ (max)} = 30\ ns \geq 15\ ns\ (t_{RDS})$

iii. When RD is critical

- Setup time calculation [$T_{1\text{-}1}$ rise]

  $2.5\ t_{cyc} - t_{RSD1\ (max)} - t_{OE\ (max)} = 45\ ns \geq 15\ ns\ (t_{RDS})$

b. H8S/2655 t_{RDH}

i. Hold time calculation [$T_{1\text{-}1}$ rise]

  $t_{AD\ (min)} + t_{OH\ (min)} = 0\ ns \geq 0\ ns\ (t_{RDH})$

2. AC Characteristics

a. H8S/2655

Item	Symbol	Min	Max	Unit
Address delay time	t_{AD}	—	20	ns
$\overline{\text{CS}}$ delay time 1	t_{CSD1}	—	20	ns
$\overline{\text{RD}}$ delay time 1	t_{RSD1}	—	20	ns
$\overline{\text{RD}}$ delay time 2	t_{RSD2}	—	20	ns
Read data setup time	t_{RDS}	15	—	ns
Read data hold time	t_{RDH}	0	—	ns

b. HN27C101AG-10

Item	Symbol	Min	Max	Unit
Access time	t_{ACC}	—	100	ns
Output delay time from $\overline{\text{CE}}$	t_{CE}	—	100	ns
Output delay time from $\overline{\text{OE}}$	t_{OE}	—	60	ns
Data output hold time	t_{OH}	0	—	ns

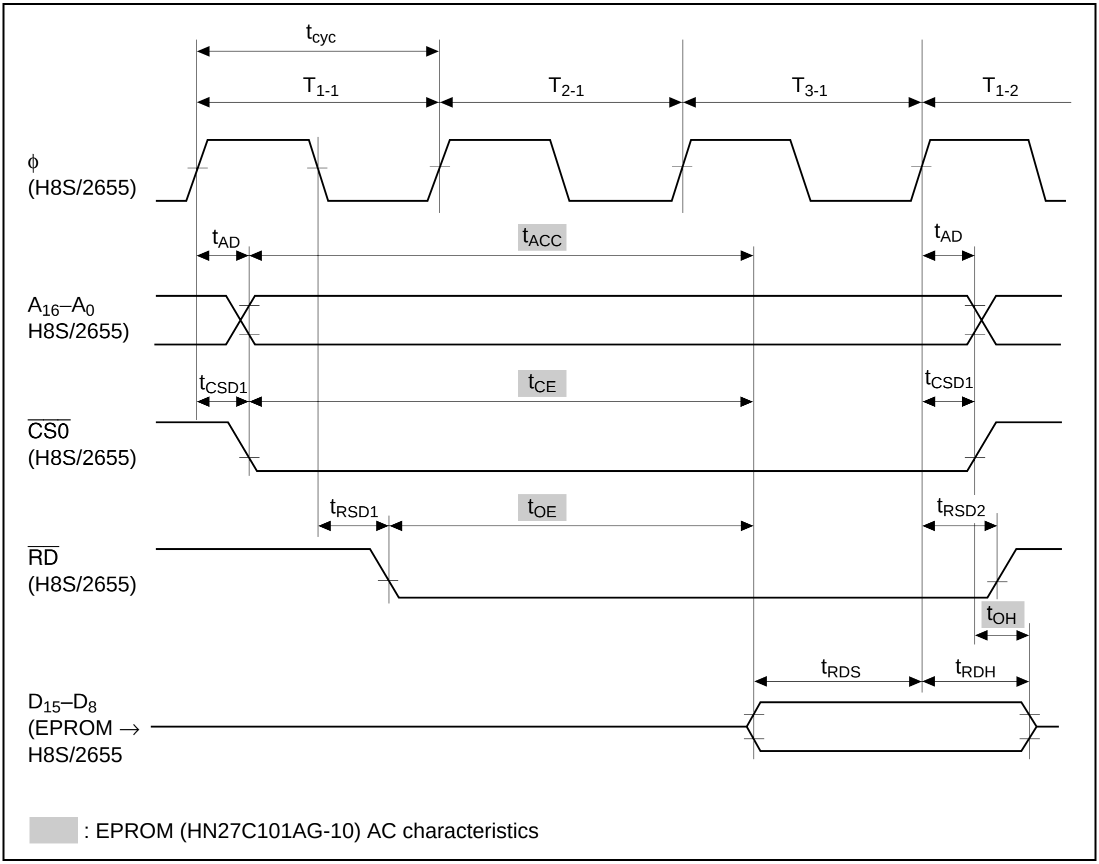


Figure 3.1.1 (c) EPROM Read Timing Chart

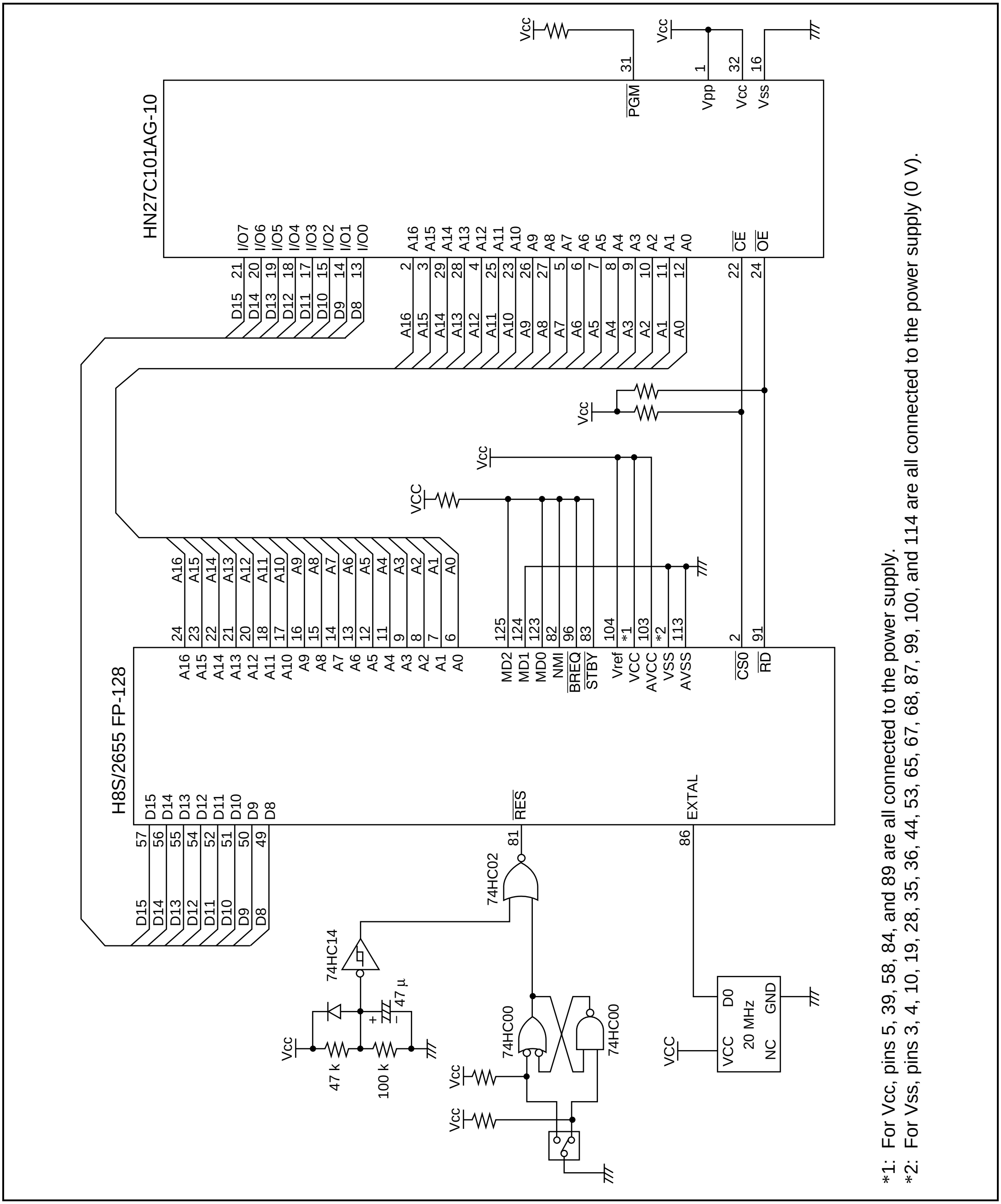


Figure 3.1.1 (d) HN27C101AG-10 Interface

3.2 EPROM (HN27C101AG-10) Interface Using 16-Bit Bus Mode

EPROM (HN27C101AG-10) Interface	MCU: H8S/2655	Functions Used: Mode 4 (16-Bit Bus Mode)

Specifications

1. Figure 3.1.2 (a) shows an example of the connection between an H8S/2655 and ×8-bit configuration EPROMs (HN27C101AG-10s). The H8S/2655 is set to mode 4 16-bit bus mode, and the EPROMs are allocated to area 0.

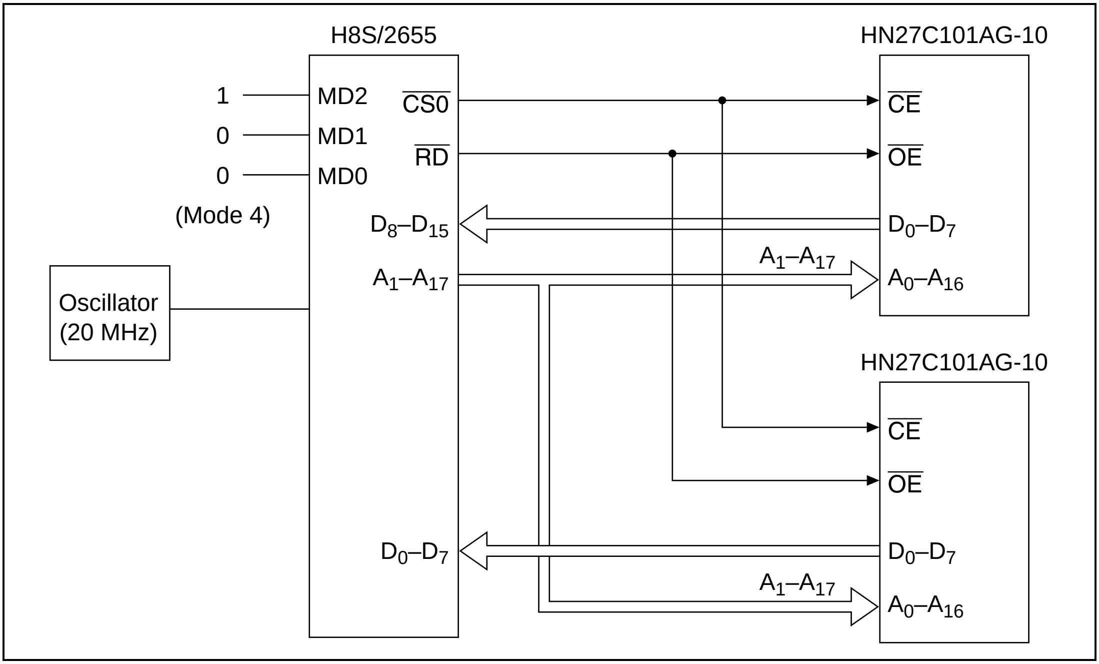


Figure 3.1.2 (a) Example of Connection between H8S/2655 and EPROMs

2. Figure 3.1.2 (b) shows the memory map. When the 16-Mbyte address space is divided into areas in 2-Mbyte units, the EPROM area is H'00 0000–H'03 FFFF.

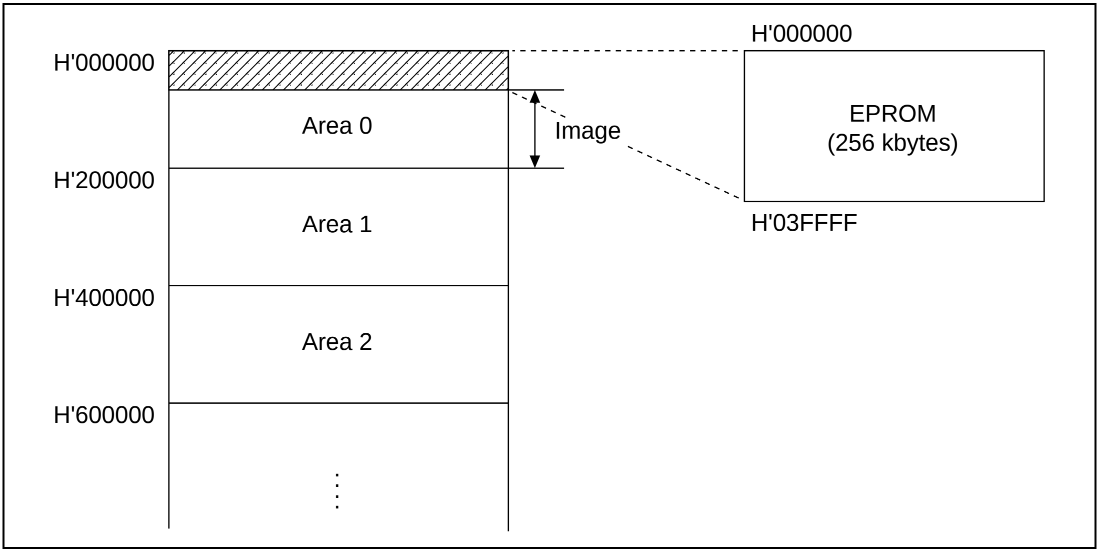


Figure 3.1.2 (b) Memory Map

3. Table 3.1.2 (a) shows the bus controller settings.

Table 3.1.2 (a) Bus Controller Settings

Name	Abbrev.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Setting
Bus width control register	ABWCR	ABW7 *	ABW6 *	ABW5 *	ABW4 *	ABW3 *	ABW2 *	ABW1 *	ABW0 0	Area 0: 16-bit access space
Access state control register	ASTCR	AST7 *	AST6 *	AST5 *	AST4 *	AST3 *	AST2 *	AST1 *	AST0 1	Area 0: 3-state access space
Wait control register H	WCRH	W71 *	W70 *	W61 *	W60 *	W51 *	W50 *	W41 *	W40 *	—
Wait control register L	WCRL	W31 *	W30 *	W21 *	W20 *	W11 *	W10 *	W01 0	W00 0	Area 0: No program wait inserted
Bus control register H	BCRH	ICIS1 *	ICIS0 *	BRSTRM 0	BRSTS1 *	BRSTS0 *	RMTS2 *	RMTS1 *	RMTS0 *	Area 0: Basic bus interface
Bus control register L	BCRL	BRLE *	BREQOE *	EAE *	LCASS *	DDS *	ASS 1	WDBE *	WAITE *	Area partition unit: 2 Mbytes (16 Mbytes)
Memory control register	MCR	TPC *	BE *	RCDM *	CW2 *	MXC1 *	MXC0 *	RLW1 *	RLW0 *	—
DRAM control register	DRAMCR	RFSHE *	RCW *	RMODE *	CMF *	CMIE *	CKS2 *	CKS1 *	CKS0 *	—
Refresh time constant register	RTCOR	*	*	*	*	*	*	*	*	—

*: Don't care

Operation

The calculations used to check whether the AC characteristics are satisfied in EPROM access are shown below. The t_{cyc} value, unspecified min value, and unspecified max value are as follows.

- t_{cyc}: 50 ns (20 MHz oscillator (= ϕ))
- Unspecified min value: 0 ns
- Unspecified max value: min value

In the times obtained based on ϕ, the reference timing is shown in [ ].

For the timing values, see 2. AC Characteristics below.

1. Read Access

   Figure 3.1.2 (c) shows the EPROM read timing chart.

   Confirm that the following AC characteristics are satisfied.

Item		Symbol
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}

a. H8S/2655 t_{RDS}

i. When address is critical

- Setup time calculation [T_{1-1} rise]

  $3\ t_{cyc} - t_{AD\ (max)} - t_{ACC\ (max)} = 30\ ns \geq 15\ ns\ (t_{RDS})$

ii. When CS is critical

- Setup time calculation [T_{1-1} rise]

  $3\ t_{cyc} - t_{CSD1\ (max)} - t_{CE\ (max)} = 30\ ns \geq 15\ ns\ (t_{RDS})$

iii. When RD is critical

- Setup time calculation [T_{1-1} rise]

  $2.5\ t_{cyc} - t_{RSD1\ (max)} - t_{OE\ (max)} = 45\ ns \geq 15\ ns\ (t_{RDS})$

b. H8S/2655 t_{RDH}

i. Hold time calculation [T_{1-1} rise]

  $t_{AD\ (min)} + t_{OH\ (min)} = 0\ ns \geq 0\ ns\ (t_{RDH})$

2. AC Characteristics

a. H8S/2655

Item	Symbol	Min	Max	Unit
Address delay time	t_{AD}	—	20	ns
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	ns
$\overline{RD}$ delay time 1	t_{RSD1}	—	20	ns
$\overline{RD}$ delay time 2	t_{RSD2}	—	20	ns
Read data setup time	t_{RDS}	15	—	ns
Read data hold time	t_{RDH}	0	—	ns

b. HN27C101AG-10

Item	Symbol	Min	Max	Unit
Access time	t_{ACC}	—	100	ns
Output delay time from $\overline{CE}$	t_{CE}	—	100	ns
Output delay time from $\overline{OE}$	t_{OE}	—	60	ns
Data output hold time	t_{OH}	0	—	ns

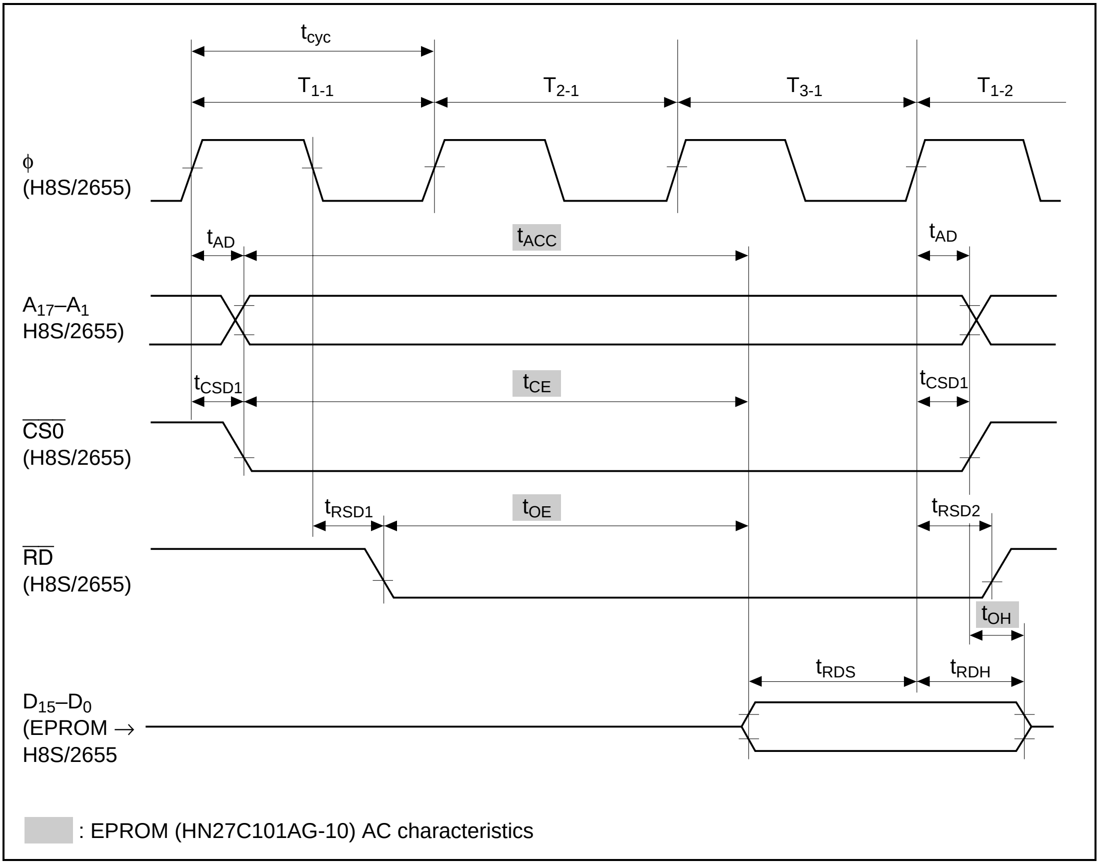


Figure 3.1.2 (c) EPROM Read Timing Chart

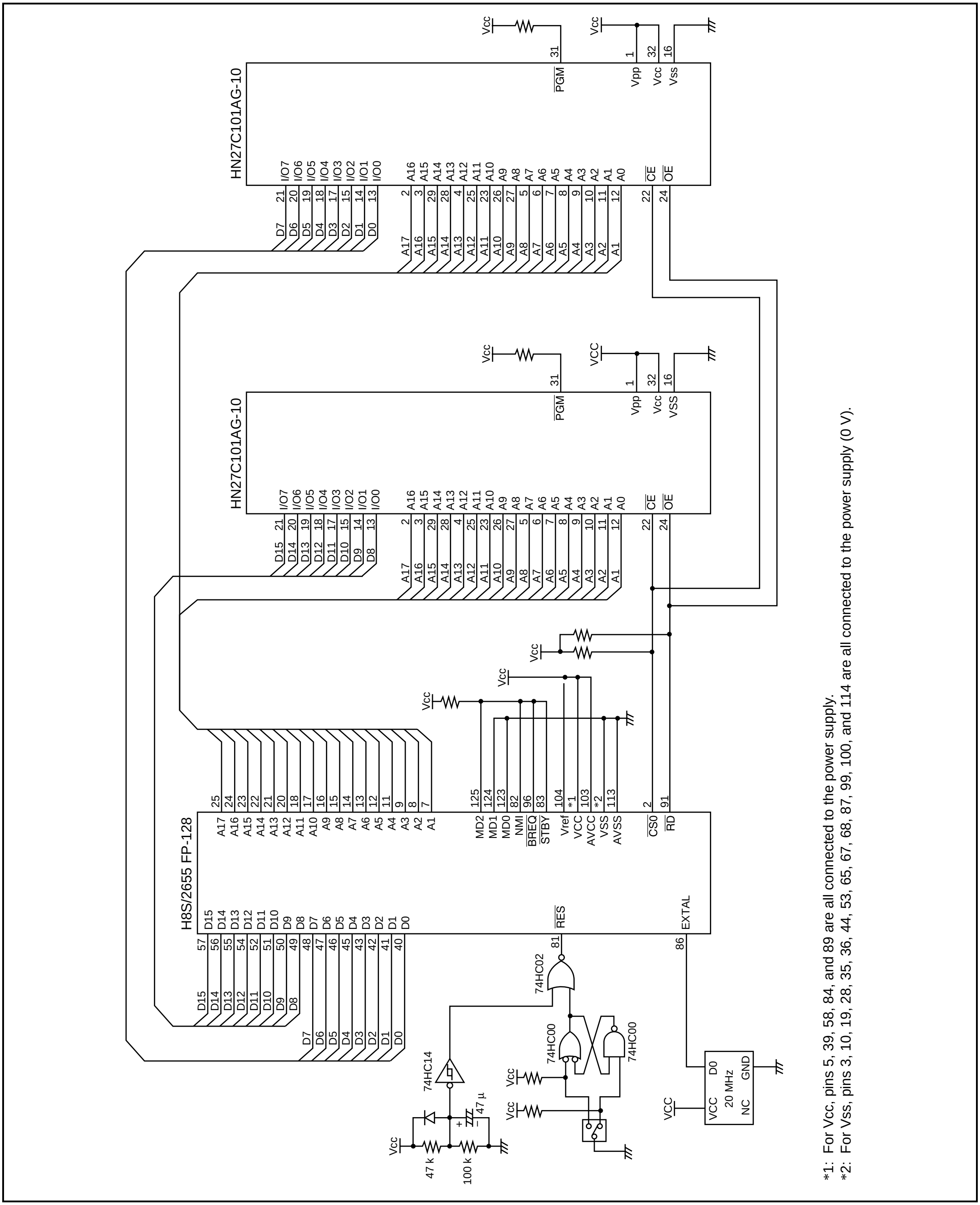


Figure 3.1.2 (d) HN27C101AG-10 Interface

3.3 SRAM (HM678127UH-12) Interface Using 8-Bit Bus Mode

SRAM (HM678127UH-12) Interface	MCU: H8S/2655	Functions Used: Mode 5 (8-Bit Bus Mode)

Specifications

1. Figure 3.2.1 (a) shows an example of the connection between an H8S/2655 and ×8-bit configuration SRAM (HM678127UH-12). The H8S/2655 is set to mode 5 8-bit bus mode, and the SRAM is allocated to area 1.

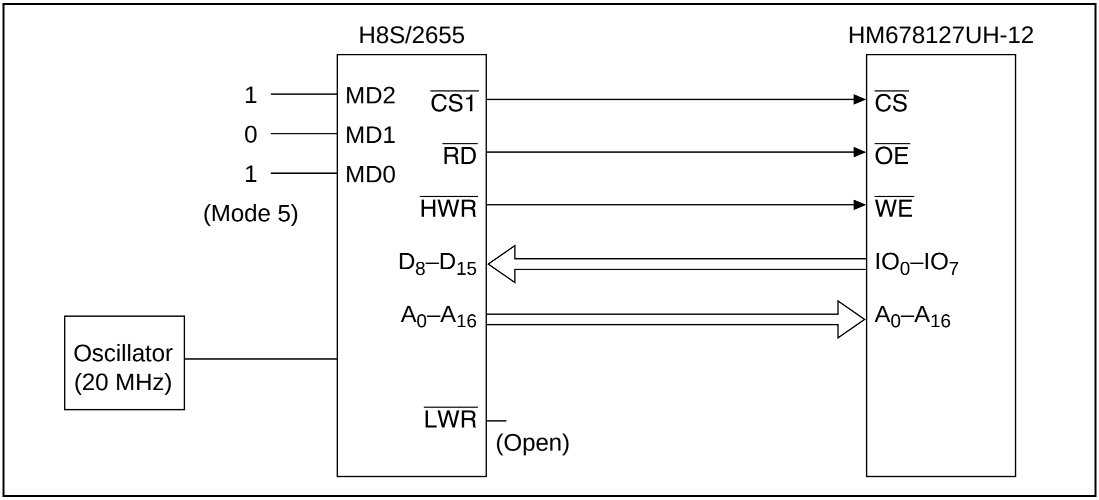


Figure 3.2.1 (a) Example of Connection between H8S/2655 and SRAM

2. Figure 3.2.1 (b) shows the memory map. When the 16-Mbyte address space is divided into areas in 2-Mbyte units, the SRAM area is H'20 0000–H'21 FFFF.

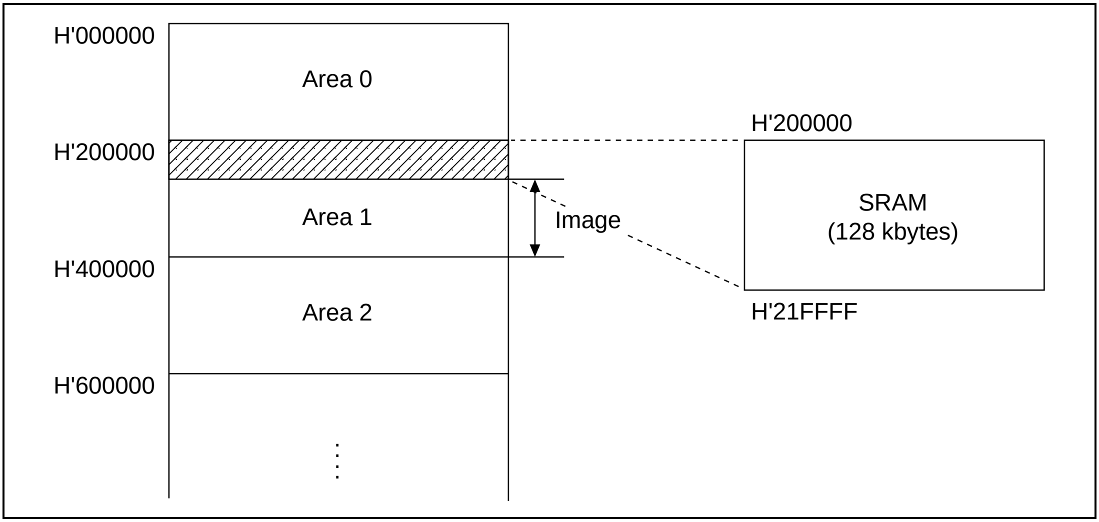


Figure 3.2.1 (b) Memory Map

3. Table 3.2.1 (a) shows the bus controller settings.

Table 3.2.1 (a) Bus Controller Settings

Name	Abbrev.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Setting
Bus width control register	ABWCR	ABW7 *	ABW6 *	ABW5 *	ABW4 *	ABW3 *	ABW2 *	ABW1 1	ABW0 *	Area 1: 8-bit access space
Access state control register	ASTCR	AST7 *	AST6 *	AST5 *	AST4 *	AST3 *	AST2 *	AST1 0	AST0 *	Area 1: 2-state access space
Wait control register H	WCRH	W71 *	W70 *	W61 *	W60 *	W51 *	W50 *	W41 *	W40 *	—
Wait control register L	WCRL	W31 *	W30 *	W21 *	W20 *	W11 0	W10 0	W01 *	W00 *	Area 1: No program wait inserted
Bus control register H	BCRH	ICIS1 *	ICIS0 *	BRSTRM *	BRSTS1 *	BRSTS0 *	RMTS2 *	RMTS1 *	RMTS0 *	—
Bus control register L	BCRL	BRLE *	BREQOE *	EAE *	LCASS *	DDS *	ASS 1	WDBE *	WAITE *	Area partition unit: 2 Mbytes (16 Mbytes)
Memory control register	MCR	TPC *	BE *	RCDM *	CW2 *	MXC1 *	MXC0 *	RLW1 *	RLW0 *	—
DRAM control register	DRAMCR	RFSHE *	RCW *	RMODE *	CMF *	CMIE *	CKS2 *	CKS1 *	CKS0 *	—
Refresh time constant register	RTCOR	*	*	*	*	*	*	*	*	—

*: Don't care

Operation

The calculations used to check whether the AC characteristics are satisfied in SRAM access are shown below. The t_{cyc} value, unspecified min value, and unspecified max value are as follows.

- t_{cyc}: 50 ns (20 MHz oscillator (= ϕ))
- Unspecified min value: 0 ns
- Unspecified max value: min value

In the times obtained based on ϕ, the reference timing is shown in [ ].

For the timing values, see 2. AC Characteristics below.

1. Read/Write Access

   Figure 3.2.1 (c) shows the SRAM read/write timing chart.

   Confirm that the following AC characteristics are satisfied.

Item		Symbol
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}
SRAM (HM678127UH-12)	Input data setting time	t_{DW}
	Input data hold time	t_{DH}
	Address setup time	t_{AS}
	Address hold time	t_{WR}
	Write pulse width	t_{WP}
	Chip select time	t_{CW}

a. Read

i. H8S/2655 t_{RDS}

i-1 When address is critical

- Setup time calculation [T_{1-1} cycle rise]

  $2\ t_{cyc} - (t_{AD\ (max)} + t_{AA\ (max)}) = 68\ ns \geq 15\ ns\ (t_{RDS})$

i-2 When CS is critical

- Setup time calculation [T_{1-1} cycle rise]

  $2\ t_{cyc} - (t_{CSD1\ (max)} + t_{ACS\ (max)}) = 68\ ns \geq 15\ ns\ (t_{RDS})$

i-3 When RD is critical

- Setup time calculation [T_{1-1} cycle rise]

  $2\ t_{cyc} - (0.5\ t_{cyc} + t_{RSD1\ (max)} + t_{OE\ (max)}) = 49\ ns \geq 15\ ns\ (t_{RDS})$

ii. H8S/2655 t_{RDH}

- Hold time calculation [T_{1-2} cycle rise]

  $t_{AD\ (min)} + t_{OH\ (min)} = 4$ ns ≥ 0 ns (t_{RDH})

b. Write

i. SRAM t_{DW} and t_{DH}

- Input data setting time calculation [T_{1-1} cycle fall]

  $0.5\ t_{cyc} + 0.5\ t_{cyc} + t_{WRD2\ (min)} - t_{WDD\ (max)} = 20$ ns ≥ 6 ns (t_{DW})
- Input data hold time calculation

  $t_{WDH\ (min)} = 15$ ns ≥ 0 ns (t_{DH})

ii. SRAM t_{WP} and t_{CW}

- Write pulse width calculation

  $t_{WSW1\ (min)} = 30$ ns ≥ 10 ns (t_{WP})
- Chip select time calculation [T_{1-1} cycle rise]

  $2\ t_{cyc} - t_{CSD1\ (max)} + t_{CSD1\ (min)} = 80$ ns ≥ 10 ns (t_{CW})

iii. SRAM t_{AS} and t_{WR}

- Address setup time calculation

  $t_{ASC\ (min)} = 10$ ns ≥ 0 ns (t_{AS})
- Address hold time calculation

  $t_{AH\ (min)} = 15$ ns ≥ 0 ns (t_{WR})

2. AC Characteristics

a. H8S/2655

Item	Symbol	Min	Max	Unit
Address delay time	t_{AD}	—	20	ns
Address setup time	t_{ASC}	$0.5 - Xt_{cyc} - 5$	—	ns
Address hold time	t_{AH}	$0.5 - Xt_{cyc} - 10$	—	ns
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	ns
$\overline{RD}$ delay time 1	t_{RSD1}	—	20	ns
$\overline{RD}$ delay time 2	t_{RSD2}	—	20	ns
Read data setup time	t_{RDS}	15	—	ns
Read data hold time	t_{RDH}	0	—	ns
$\overline{WR}$ delay time 2	t_{WRD2}	—	20	ns
$\overline{WR}$ pulse width 1	t_{WSW1}	$1.0 - Xt_{cyc} - 20$	—	ns
Write data delay time	t_{WDD}	—	30	ns
Write data hold time	t_{WDH}	$0.5 - Xt_{cyc} - 10$	—	ns

b. HM678127UH-12

Item	Symbol	Min	Max	Unit
Address access time	t_{AA}	—	12	ns
Chip select access time	t_{ACS}	—	12	ns
Output enable access time	t_{OE}	—	6	ns
Output hold time	t_{OH}	4	—	ns
Chip select time	t_{CW}	10	—	ns
Address setup time	t_{AS}	0	—	ns
Write pulse time	t_{WP}	10	—	ns
Address hold time	t_{WR}	0	—	ns
Input data setting time	t_{DW}	6	—	ns
Input data hold time	t_{DH}	0	—	ns

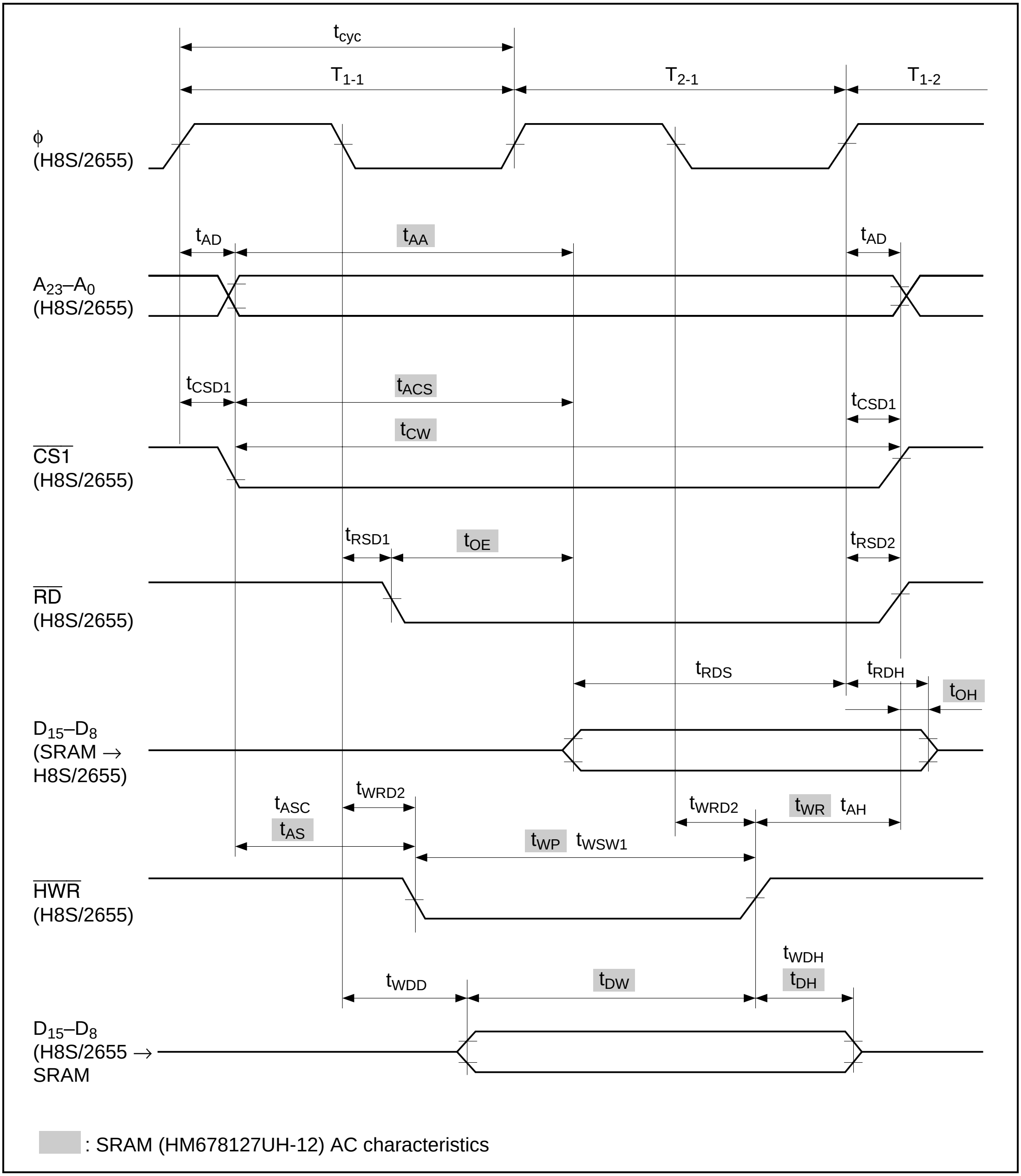


Figure 3.2.1 (c) SRAM Read/Write Timing Chart

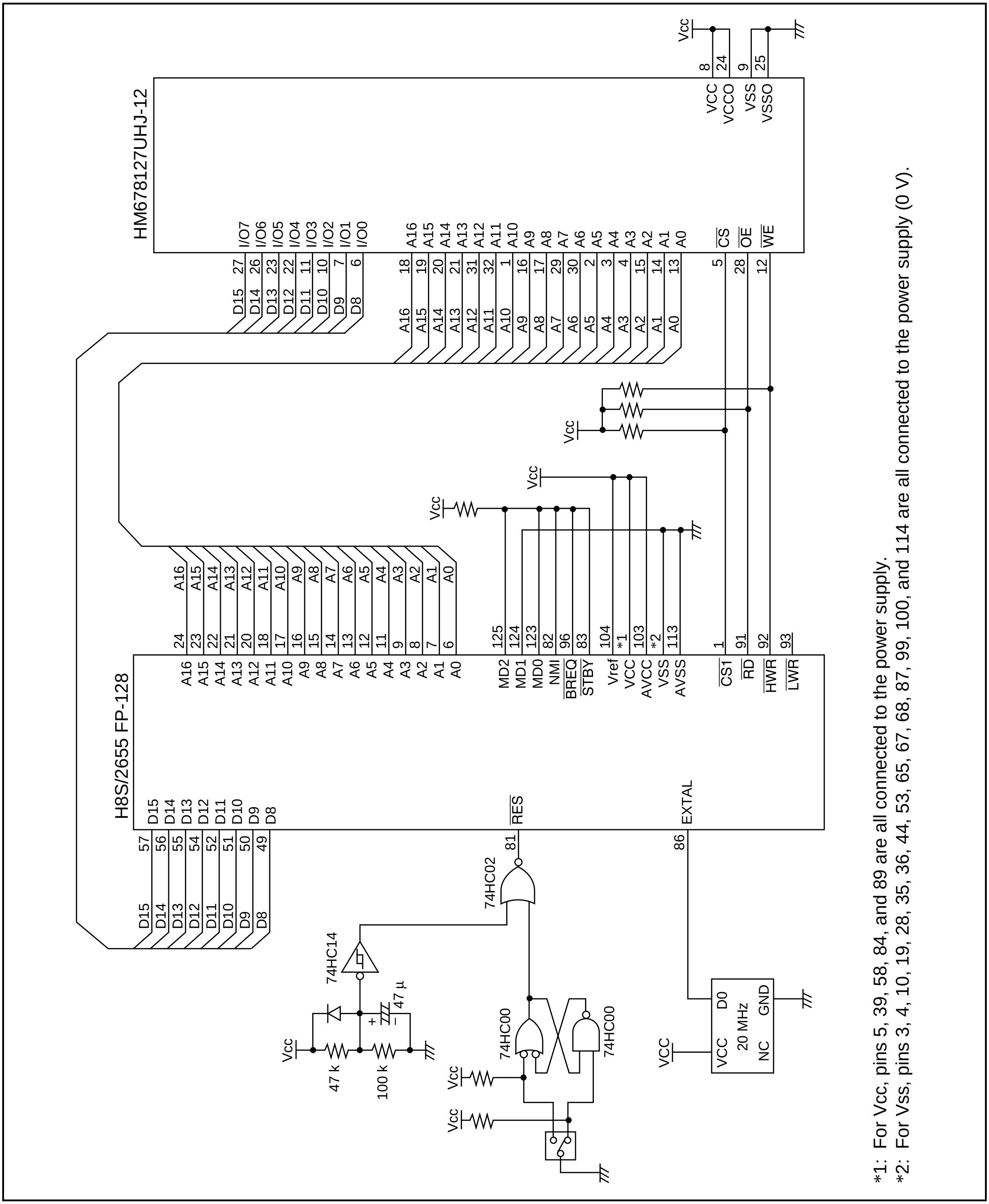


Figure 3.2.1 (d) HM678127UHJ-12 Interface

3.4 SRAM (HM678127UH-12) Interface Using 16-Bit Bus Mode

SRAM (HM678127UH-12) Interface	MCU: H8S/2655	Functions Used: Mode 4 (16-Bit Bus Mode)

Specifications

1. Figure 3.2.2 (a) shows an example of the connection between an H8S/2655 and ×8-bit configuration SRAMs (HM678127UH-12s). The H8S/2655 is set to mode 4 16-bit bus mode, and the SRAMs are allocated to area 1.

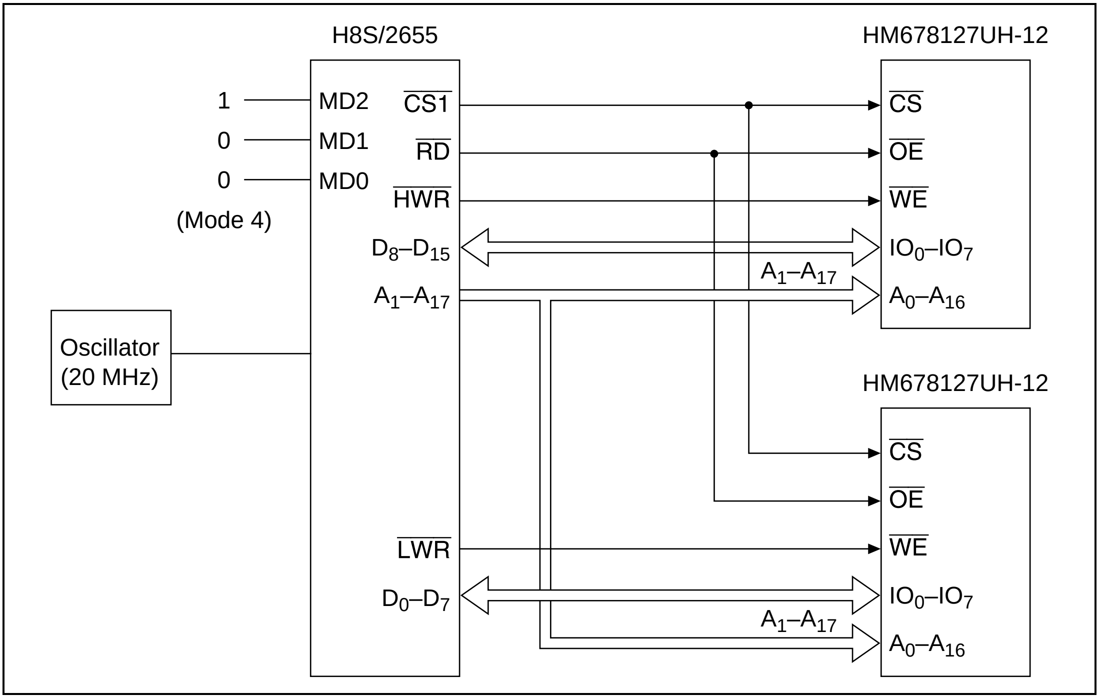


Figure 3.2.2 (a) Example of Connection between H8S/2655 and SRAMs

2. Figure 3.2.2 (b) shows the memory map. When the 16-Mbyte address space is divided into areas in 2-Mbyte units, the SRAM area is H'20 0000–H'23 FFFF.

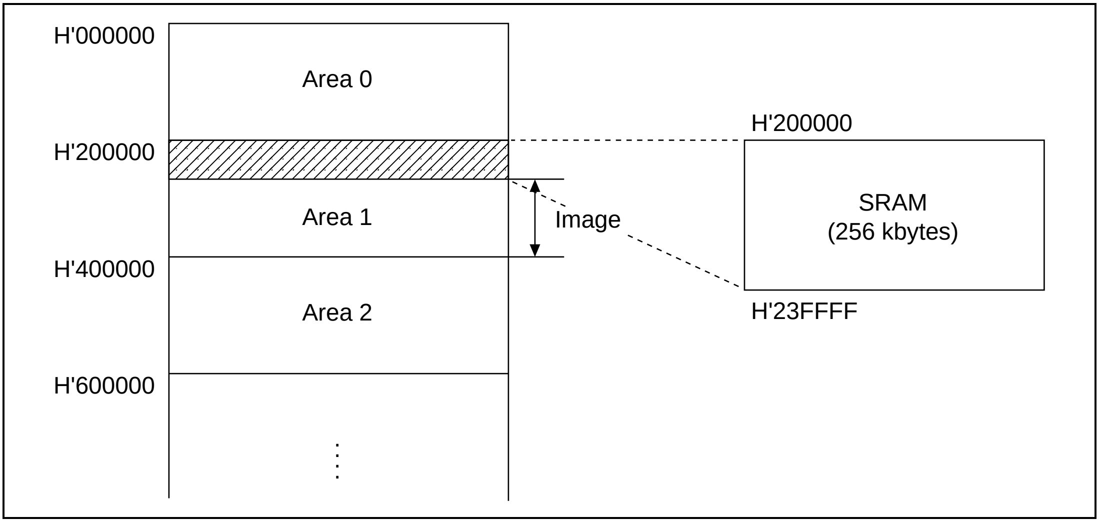


Figure 3.2.2 (b)   Memory Map

3. Table 3.2.2 (a) shows the bus controller settings.

Table 3.2.2 (a) Bus Controller Settings

Name	Abbrev.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Setting
Bus width control register	ABWCR	ABW7 *	ABW6 *	ABW5 *	ABW4 *	ABW3 *	ABW2 *	ABW1 0	ABW0 *	Area 1: 16-bit access space
Access state control register	ASTCR	AST7 *	AST6 *	AST5 *	AST4 *	AST3 *	AST2 *	AST1 0	AST0 *	Area 1: 2-state access space
Wait control register H	WCRH	W71 *	W70 *	W61 *	W60 *	W51 *	W50 *	W41 *	W40 *	—
Wait control register L	WCRL	W31 *	W30 *	W21 *	W20 *	W11 0	W10 0	W01 *	W00 *	Area 1: No program wait inserted
Bus control register H	BCRH	ICIS1 *	ICIS0 *	BRSTRM *	BRSTS1 *	BRSTS0 *	RMTS2 *	RMTS1 *	RMTS0 *	—
Bus control register L	BCRL	BRLE *	BREQOE *	EAE *	LCASS *	DDS *	ASS 1	WDBE *	WAITE *	Area partition unit: 2 Mbytes (16 Mbytes)
Memory control register	MCR	TPC *	BE *	RCDM *	CW2 *	MXC1 *	MXC0 *	RLW1 *	RLW0 *	—
DRAM control register	DRAMCR	RFSHE *	RCW *	RMODE *	CMF *	CMIE *	CKS2 *	CKS1 *	CKS0 *	—
Refresh time constant register	RTCOR	*	*	*	*	*	*	*	*	—

*: Don’t care

Operation

The calculations used to check whether the AC characteristics are satisfied in SRAM access are shown below. The t_{cyc} value, unspecified min value, and unspecified max value are as follows.

- t_{cyc}: 50 ns (20 MHz oscillator (= ϕ))
- Unspecified min value: 0 ns
- Unspecified max value: min value

In the times obtained based on ϕ, the reference timing is shown in [ ].

For the timing values, see 2. AC Characteristics below.

1. Read/Write Access

   Figure 3.2.2 (c) shows the SRAM read/write timing chart.

   Confirm that the following AC characteristics are satisfied.

Item		**Symbol**
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}
SRAM (HM678127UH-12)	Input data setting time	t_{DW}
	Input data hold time	t_{DH}
	Address setup time	t_{AS}
	Address hold time	t_{WR}
	Write pulse width	t_{WP}
	Chip select time	t_{CW}

a. Read

i. Confirm H8S/2655 t_{RDS} and t_{RDH}.

i-1 When address is critical

- Setup time calculation [T_{1-1} cycle rise]

  $2\ t_{cyc} – (t_{AD\ (max)} + t_{AA\ (max)}) = 68\ ns \geq 15\ ns\ (t_{RDS})$

i-2 When CS is critical

- Setup time calculation [T_{1-1} cycle rise]

  $2\ t_{cyc} – (t_{CSD1\ (max)} + t_{ACS\ (max)}) = 68\ ns \geq 15\ ns\ (t_{RDS})$

i-3 When RD is critical

- Setup time calculation [T_{1-1} cycle rise]

  $2\ t_{cyc} – (0.5\ t_{cyc} + t_{RSD1\ (max)} + t_{OE\ (max)}) = 49\ ns \geq 15\ ns\ (t_{RDS})$

ii. H8S/2655 t_{RDH}

- Hold time calculation [$T_{1\text{-}2}$ cycle rise]

  $t_{AD\ (min)} + t_{OH\ (min)} = 4$ ns ≥ 0 ns (t_{RDH})

b. Write

i. SRAM t_{DW} and t_{DH}

- Input data setting time calculation [$T_{1\text{-}1}$ cycle fall]

  $0.5\ t_{cyc} + 0.5\ t_{cyc} + t_{WRD2\ (min)} - t_{WDD\ (max)} = 20$ ns ≥ 6 ns (t_{DW})
- Input data hold time calculation

  $t_{WDH\ (min)} = 15$ ns ≥ 0 ns (t_{DH})

ii. SRAM t_{WP} and t_{CW}

- Write pulse width calculation

  $t_{WSW1\ (min)} = 30$ ns ≥ 10 ns (t_{WP})
- Chip select time calculation [$T_{1\text{-}1}$ cycle rise]

  $2\ t_{cyc} - t_{CSD1\ (max)} + t_{CSD1\ (min)} = 80$ ns ≥ 10 ns (t_{CW})

iii. SRAM t_{AS} and t_{WR}

- Address setup time calculation

  $t_{ASC\ (min)} = 10$ ns ≥ 0 ns (t_{AS})
- Address hold time calculation

  $t_{AH\ (min)} = 15$ ns ≥ 0 ns (t_{WR})

2. AC Characteristics

a. H8S/2655

Item	Symbol	Min	Max	Unit
Address delay time	t_{AD}	—	20	ns
Address setup time	t_{ASC}	$0.5 - Xt_{cyc} - 15$	—	ns
Address hold time	t_{AH}	$0.5 - Xt_{cyc} - 10$	—	ns
$\overline{\text{CS}}$ delay time 1	t_{CSD1}	—	20	ns
$\overline{\text{RD}}$ delay time 1	t_{RSD1}	—	20	ns
$\overline{\text{RD}}$ delay time 2	t_{RSD2}	—	20	ns
Read data setup time	t_{RDS}	15	—	ns
Read data hold time	t_{RDH}	0	—	ns
$\overline{\text{WR}}$ delay time 2	t_{WRD2}	—	20	ns
$\overline{\text{WR}}$ pulse width 1	t_{WSW1}	$1.0 - Xt_{cyc} - 20$	—	ns
Write data delay time	t_{WDD}	—	30	ns
Write data hold time	t_{WDH}	$0.5 - Xt_{cyc} - 10$	—	ns

b. HM678127UH-12

Item	Symbol	Min	Max	Unit
Address access time	t_{AA}	—	12	ns
Chip select access time	t_{ACS}	—	12	ns
Output enable access time	t_{OE}	—	6	ns
Output hold time	t_{OH}	4	—	ns
Chip select time	t_{CW}	10	—	ns
Address setup time	t_{AS}	0	—	ns
Write pulse time	t_{WP}	10	—	ns
Address hold time	t_{WR}	0	—	ns
Input data setting time	t_{DW}	6	—	ns
Input data hold time	t_{DH}	0	—	ns

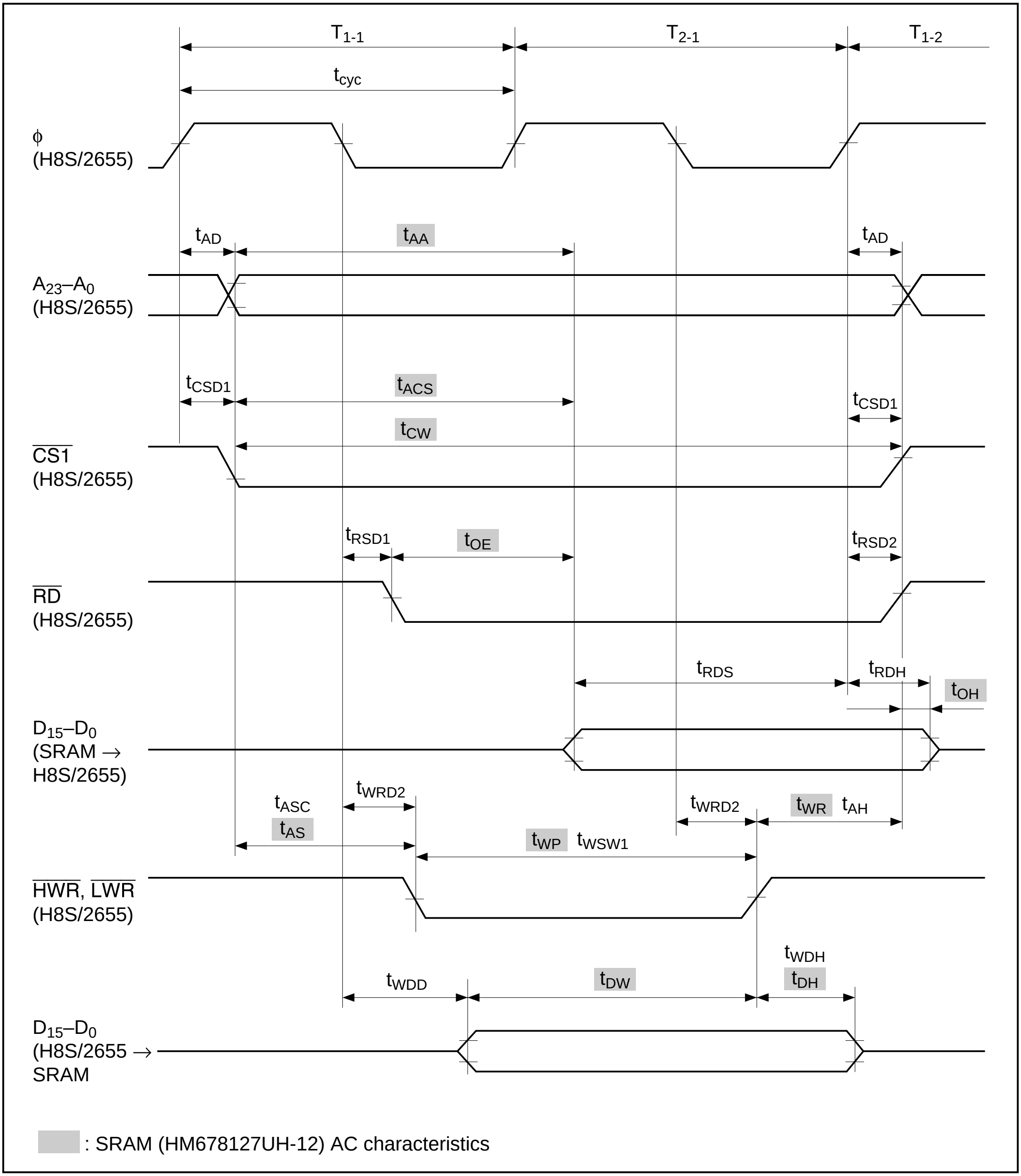


Figure 3.2.2 (c) SRAM Read/Write Timing Chart

RENESAS

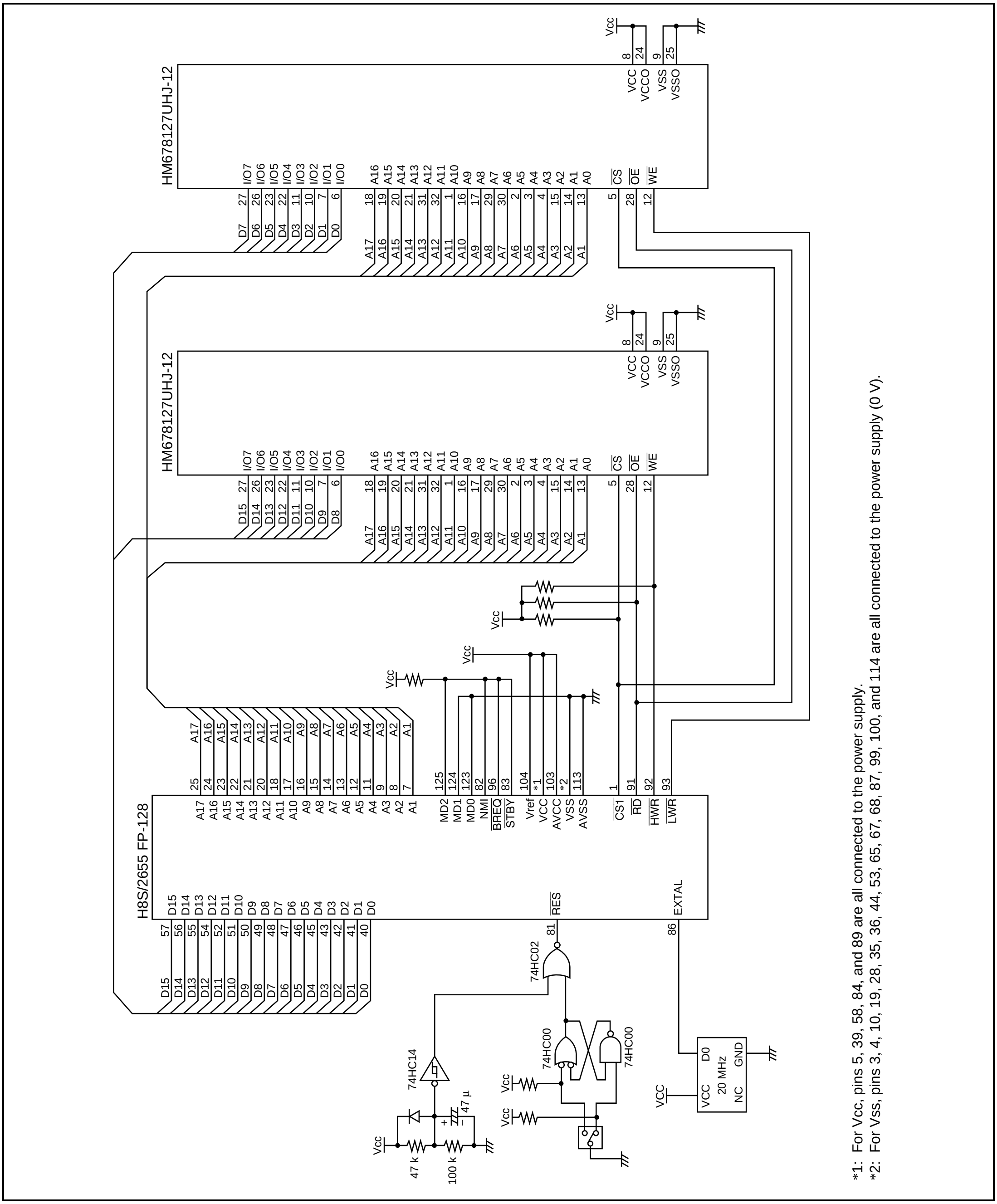


Figure 3.2.2 (d) HM678127UHJ-12 Interface

3.5 SRAM (HM628128B-8) Interface Using 8-Bit Bus Mode

SRAM (HM628128B-8) Interface	MCU: H8S/2655	Functions Used: Mode 5 (8-Bit Bus Mode)

Specifications

1. Figure 3.2.3 (a) shows an example of the connection between an H8S/2655 and ×8-bit configuration SRAM (HM628128B-8). The H8S/2655 is set to mode 5 8-bit bus mode, and the SRAM is allocated to area 1.

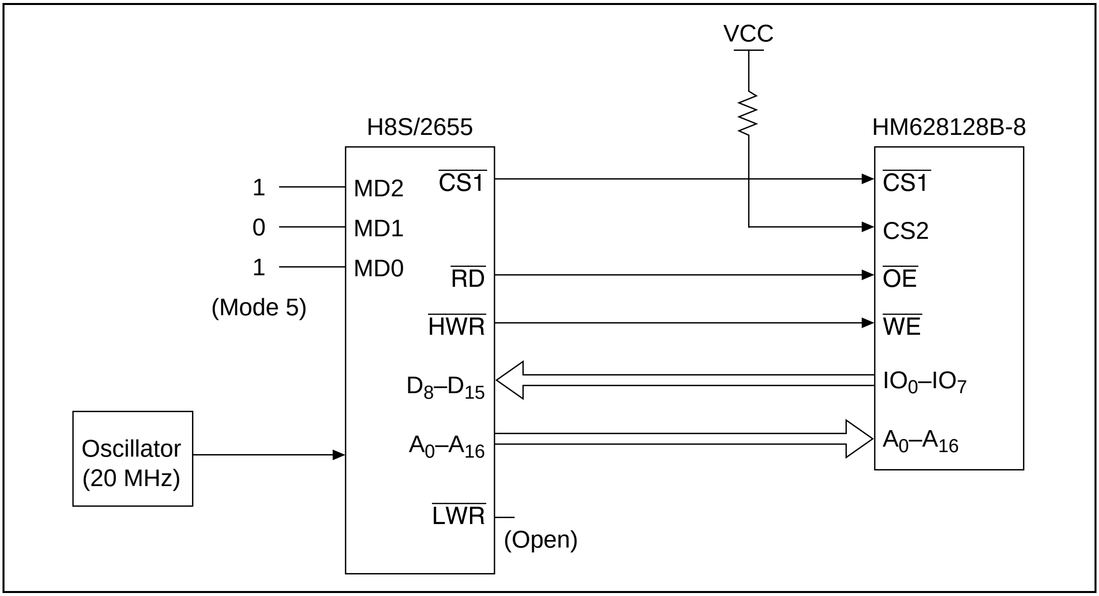


Figure 3.2.3 (a) Example of Connection between H8S/2655 and SRAM

2. Figure 3.2.3 (b) shows the memory map. When the 16-Mbyte address space is divided into areas in 2-Mbyte units, the SRAM area is H'20 0000–H'21 FFFF.

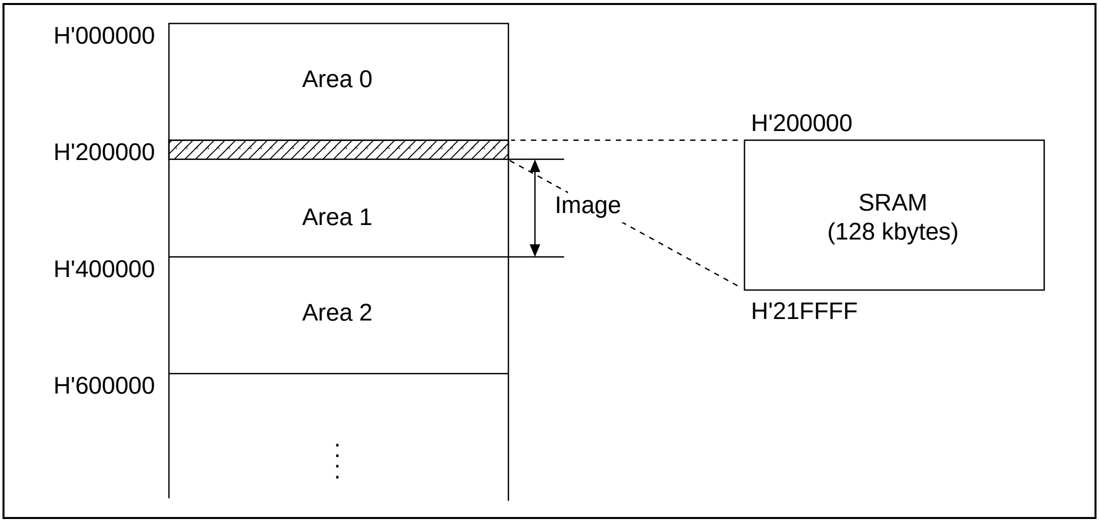


Figure 3.2.3 (b) Memory Map

3. Table 3.2.3 (a) shows the bus controller settings.

Table 3.2.3 (a) Bus Controller Settings

Name	Abbrev.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Setting
Bus width control register	ABWCR	ABW7 *	ABW6 *	ABW5 *	ABW4 *	ABW3 *	ABW2 *	ABW1 1	ABW0 *	Area 1: 8-bit access space
Access state control register	ASTCR	AST7 *	AST6 *	AST5 *	AST4 *	AST3 *	AST2 *	AST1 1	AST0 *	Area 1: 3-state access space
Wait control register H	WCRH	W71 *	W70 *	W61 *	W60 *	W51 *	W50 *	W41 *	W40 *	—
Wait control register L	WCRL	W31 *	W30 *	W21 *	W20 *	W11 0	W10 0	W01 *	W00 *	Area 1: No program wait inserted
Bus control register H	BCRH	ICIS1 *	ICIS0 *	BRSTRM 0	BRSTS1 *	BRSTS0 *	RMTS2 *	RMTS1 *	RMTS0 *	—
Bus control register L	BCRL	BRLE *	BREQOE *	EAE *	LCASS *	DDS *	ASS 1	WDBE *	WAITE *	Area partition unit: 2 Mbytes (16 Mbytes)
Memory control register	MCR	TPC *	BE *	RCDM *	CW2 *	MXC1 *	MXC0 *	RLW1 *	RLW0 *	—
DRAM control register	DRAMCR	RFSHE *	RCW *	RMODE *	CMF *	CMIE *	CKS2 *	CKS1 *	CKS0 *	—
Refresh time constant register	RTCOR	*	*	*	*	*	*	*	*	—

*: Don't care

Operation

The calculations used to check whether the AC characteristics are satisfied in SRAM access are shown below. The t_{cyc} value, unspecified min value, and unspecified max value are as follows.

- t_{cyc}: 50 ns (20 MHz oscillator (= ϕ))
- Unspecified min value: 0 ns
- Unspecified max value: min value

In the times obtained based on ϕ, the reference timing is shown in [ ].

For the timing values, see 2. AC Characteristics below.

1. Read/Write Access
   Figure 3.2.3 (c) shows the SRAM read/write timing chart.
   Confirm that the following AC characteristics are satisfied.

Item		Symbol
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}
SRAM (HM628128B-8)	Input data setting time	t_{DW}
	Input data hold time	t_{DH}
	Address setup time	t_{AS}
	Address hold time	t_{WR}
	Write pulse width	t_{WP}
	Chip select time	t_{CW}

a. Read cycle
   Confirm H8S/2655 t_{RDS} and t_{RDH}.

   i. When address is critical
      - Setup time calculation [$T_{1\text{-}1}$ cycle rise]
        $3\ t_{cyc} – (t_{AD\ (max)} + t_{AA\ (max)}) = 45\ ns \geq 15\ ns\ (t_{RDS})$
      - Hold time calculation [$T_{1\text{-}2}$ cycle rise]
        $t_{AD\ (min)} + t_{OH\ (min)} = 10\ ns \geq 0\ ns\ (t_{RDH})$

   ii. When CS is critical
      - Setup time calculation [$T_{1\text{-}1}$ cycle rise]
        $3\ t_{cyc}\ \ (t_{CSD1\ (max)} + t_{CO1\ (max)}) = 45\ ns \geq 15\ ns\ (t_{RDS})$
      - Hold time calculation [$T_{1\text{-}2}$ cycle rise]
        $t_{CSD1\ (min)} + t_{OH\ (min)} = 10\ ns \geq 0\ ns\ (t_{RDH})$

iii. When RD is critical

- Setup time calculation [T_{1-1} cycle fall]

  $2.5\ t_{cyc} - (t_{RSD1\ (max)} + t_{OE\ (max)}) = 60\ ns \geq 15\ ns\ (t_{RDS})$
- Hold time calculation [T_{1-2} cycle rise]

  $t_{RSD2\ (min)} + t_{OH\ (min)} = 10\ ns \geq 0\ ns\ (t_{RDH})$

b. Write cycle

Confirm SRAM t_{DW}, t_{DH}, t_{WP}, t_{CW}, t_{AS}, and t_{WR}.

i. SRAM t_{DW} and t_{DH}

- Input data setting time calculation [T_{1-1} cycle fall]

  $2\ t_{cyc} + t_{WRD2\ (min)} - t_{WDD\ (max)} = 70\ ns \geq 35\ ns\ (t_{DW})$
- Input data hold time calculation

  $t_{WDH\ (min)} = 0.5\ t_{cyc} - 10 = 15\ ns \geq 0\ ns\ (t_{DH})$

ii. SRAM t_{WP} and t_{CW}

- Write pulse width calculation [T_2 cycle rise]

  $1.5\ t_{cyc} + t_{WRD2\ (min)} - t_{WRD1\ (max)} = 55\ ns \geq 55\ ns\ (t_{WP})$
- Chip select time calculation [T_{1-1} cycle rise]

  $3\ t_{cyc} + t_{CSD1\ (min)} - t_{CSD1\ (max)} = 130\ ns \geq 75\ ns\ (t_{CW})$

iii. SRAM t_{AS} and t_{WR}

- Address setup time calculation [T_{1-1} cycle rise]

  $t_{cyc} + t_{WRD1\ (min)} - t_{AD\ (max)} = 30\ ns \geq 0\ ns\ (t_{AS})$
- Address hold time calculation [T_3 cycle fall]

  $0.5\ t_{cyc} + t_{AD\ (min)} - t_{WRD2\ (max)} = 5\ ns \geq 0\ ns\ (t_{WR})$

2. AC Characteristics

a. H8S/2655

Item	Symbol	Min	Max	Unit
Address delay time	t_{AD}	—	20	ns
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	ns
$\overline{RD}$ delay time 1	t_{RSD1}	—	20	ns
$\overline{RD}$ delay time 2	t_{RSD2}	—	20	ns
Read data setup time	t_{RDS}	15	—	ns
Read data hold time	t_{RDH}	0	—	ns
$\overline{WR}$ delay time 1	t_{WRD1}	—	20	ns
$\overline{WR}$ delay time 2	t_{WRD2}	—	20	ns
Write data delay time	t_{WDD}	—	30	ns
Write data hold time	t_{WDH}	$0.5 – Xt_{cyc} – 10$	—	ns

b. HM628128B-8

Item	Symbol	Min	Max	Unit
Address access time	t_{AA}	—	85	ns
Chip select access time	t_{CO1}	—	85	ns
Output enable access time	t_{OE}	—	45	ns
Output hold time	t_{OH}	10	—	ns
Chip select time	t_{CW}	60	—	ns
Address setup time	t_{AS}	0	—	ns
Write pulse width	t_{WP}	50	—	ns
Address hold time	t_{WR}	0	—	ns
Input data setting time	t_{DW}	30	—	ns
Input data hold time	t_{DH}	0	—	ns

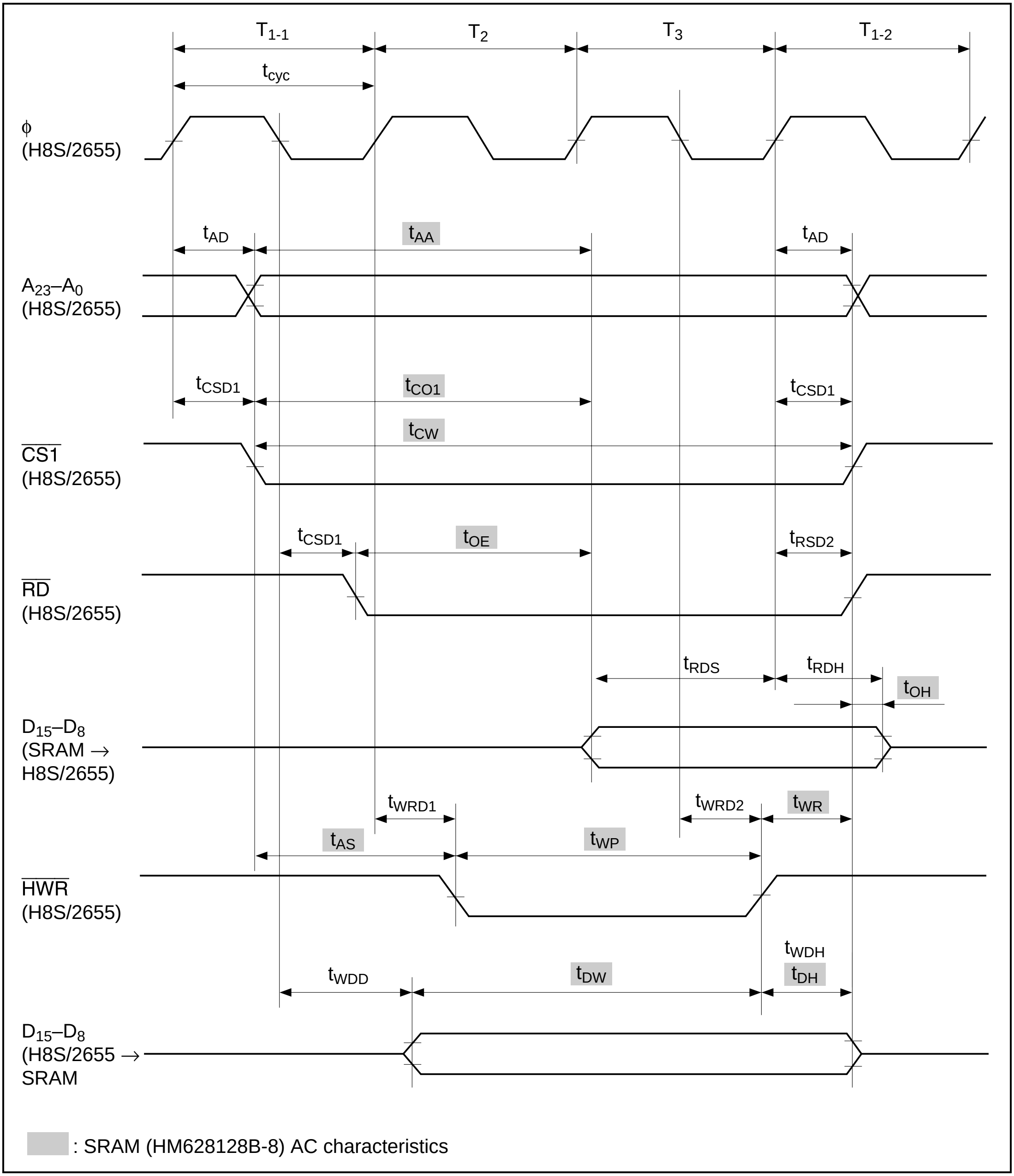


Figure 3.2.3 (c) Read/Write Timing Chart

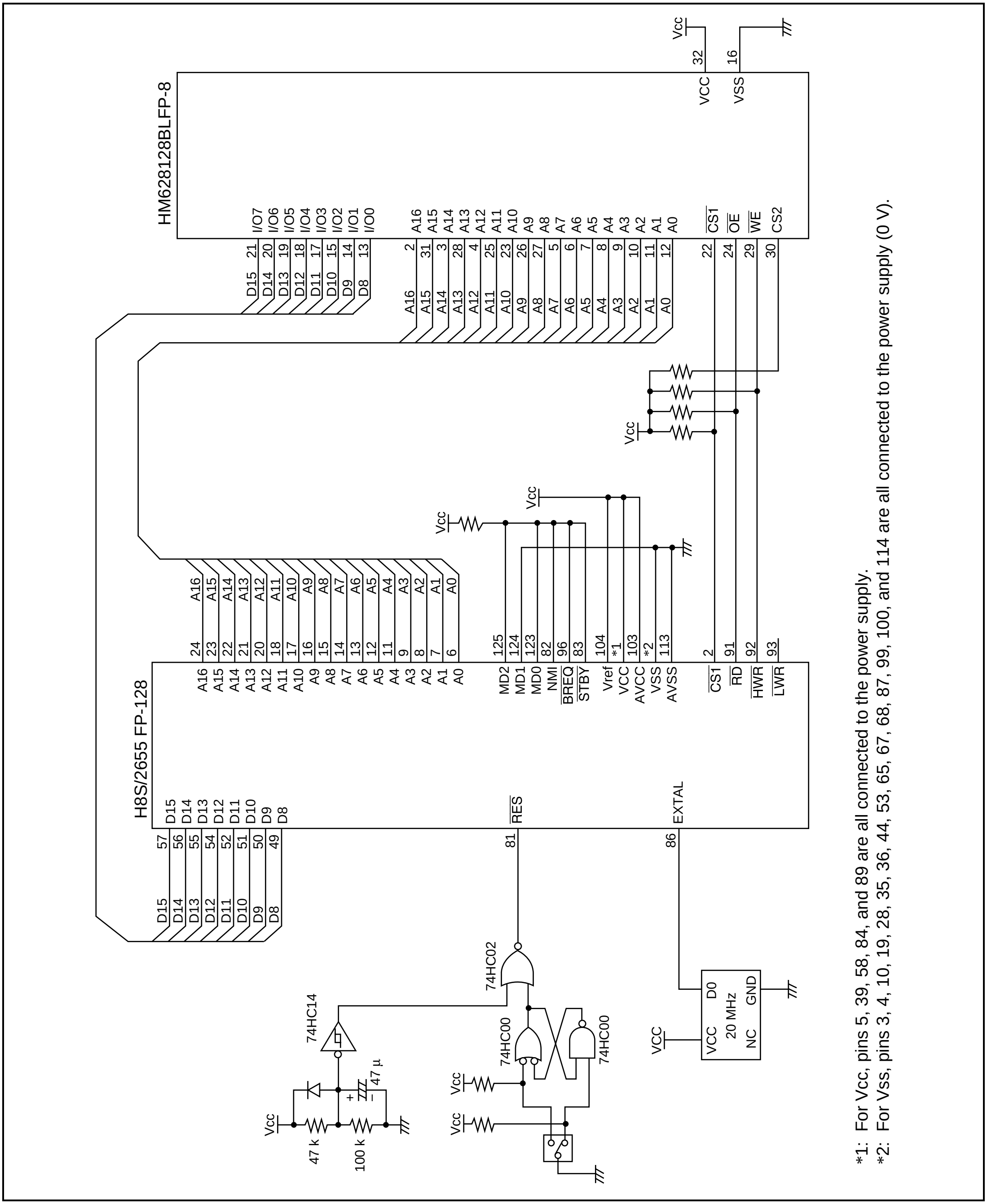


Figure 3.2.3 (d) HM628128BLFP-8 Interface

3.6 SRAM (HM628128B-8) Interface Using 16-Bit Bus Mode

SRAM (HM628128B-8) Interface	MCU: H8S/2655	Functions Used: Mode 4 (16-Bit Bus Mode)

Specifications

1. Figure 3.2.4 (a) shows an example of the connection between an H8S/2655 and ×8-bit configuration SRAMs (HM628128B-8s). The H8S/2655 is set to mode 4 16-bit bus mode, and the SRAMs are allocated to area 1.

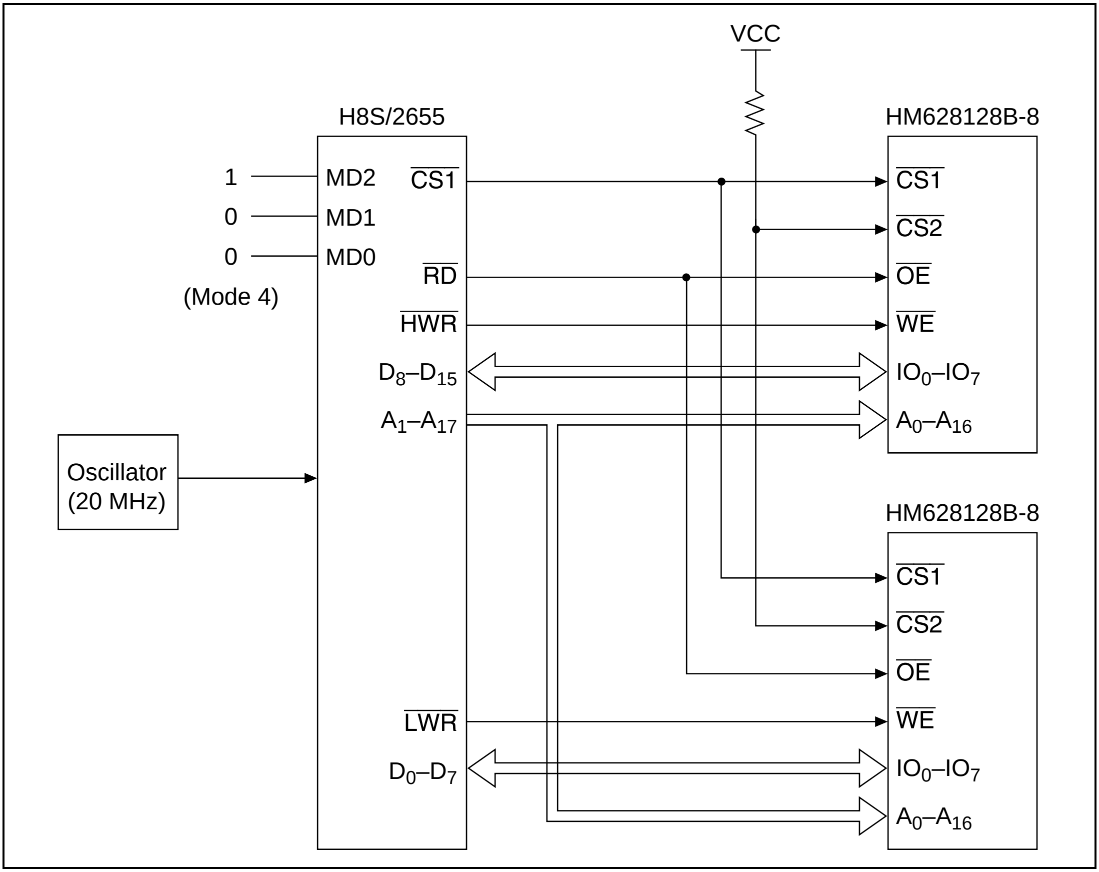


Figure 3.2.4 (a) Example of Connection between H8S/2655 and SRAMs

2. Figure 3.2.4 (b) shows the memory map. When the 16-Mbyte address space is divided into areas in 2-Mbyte units, the SRAM area is H'20 0000–H'23 FFFF.

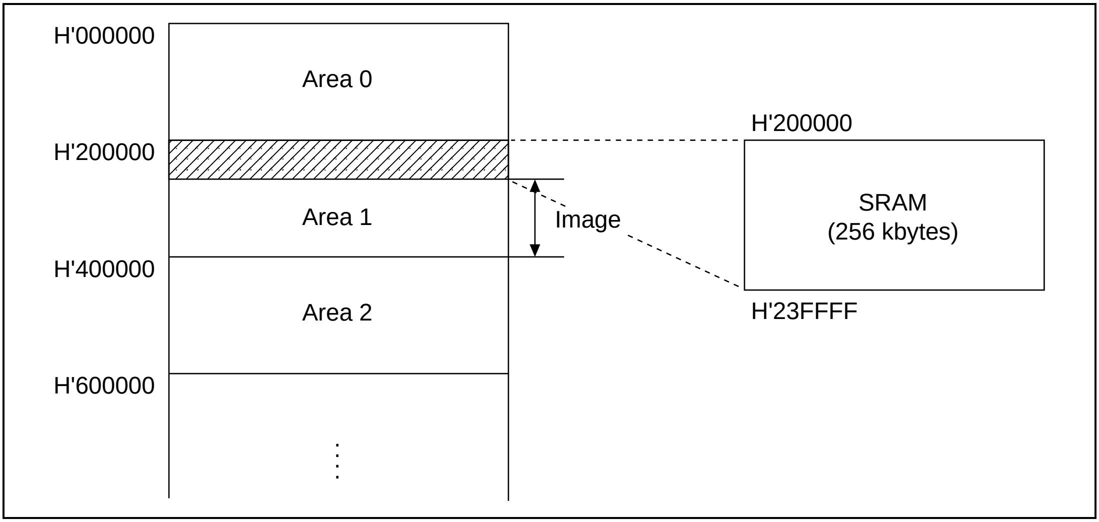


Figure 3.2.4 (b) Memory Map

3. Table 3.2.4 (a) shows the bus controller settings.

Table 3.2.4 (a) Bus Controller Settings

Name	Abbrev.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Setting
Bus width control register	ABWCR	ABW7 *	ABW6 *	ABW5 *	ABW4 *	ABW3 *	ABW2 *	ABW1 0	ABW0 *	Area 1: 16-bit access space
Access state control register	ASTCR	AST7 *	AST6 *	AST5 *	AST4 *	AST3 *	AST2 *	AST1 1	AST0 *	Area 1: 3-state access space
Wait control register H	WCRH	W71 *	W70 *	W61 *	W60 *	W51 *	W50 *	W41 *	W40 *	—
Wait control register L	WCRL	W31 *	W30 *	W21 *	W20 *	W11 0	W10 0	W01 *	W00 *	Area 1: No program wait inserted
Bus control register H	BCRH	ICIS1 *	ICIS0 *	BRSTRM *	BRSTS1 *	BRSTS0 *	RMTS2 *	RMTS1 *	RMTS0 *	—
Bus control register L	BCRL	BRLE *	BREQOE *	EAE *	LCASS *	DDS *	ASS 1	WDBE *	WAITE *	Area partition unit: 2 Mbytes (16 Mbytes)
Memory control register	MCR	TPC *	BE *	RCDM *	CW2 *	MXC1 *	MXC0 *	RLW1 *	RLW0 *	—
DRAM control register	DRAMCR	RFSHE *	RCW *	RMODE *	CMF *	CMIE *	CKS2 *	CKS1 *	CKS0 *	—
Refresh time constant register	RTCOR	*	*	*	*	*	*	*	*	—

*: Don't care

Operation

The calculations used to check whether the AC characteristics are satisfied in SRAM access are shown below. The t_{cyc} value, unspecified min value, and unspecified max value are as follows.

- t_{cyc}: 50 ns (20 MHz oscillator (= ϕ))
- Unspecified min value: 0 ns
- Unspecified max value: min value

In the times obtained based on ϕ, the reference timing is shown in [ ].

For the timing values, see 2. AC Characteristics below.

1. Read/Write Access

   Figure 3.2.4 (c) shows the SRAM read/write timing chart.

   Confirm that the following AC characteristics are satisfied.

Item		Symbol
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}
SRAM (HM628128B-8)	Input data setting time	t_{DW}
	Input data hold time	t_{DH}
	Address setup time	t_{AS}
	Address hold time	t_{WR}
	Write pulse width	t_{WP}
	Chip select time	t_{CW}

a. Read cycle

   Confirm H8S/2655 t_{RDS} and t_{RDH}.

   i. When address is critical

   - Setup time calculation [$T_{1\text{-}1}$ cycle rise]

     $3\ t_{cyc} - (t_{AD\ (max)} + t_{AA\ (max)}) = 45\ ns \geq 15\ ns\ (t_{RDS})$

   - Hold time calculation [$T_{1\text{-}2}$ cycle rise]

     $t_{AD\ (min)} + t_{OH\ (min)} = 10\ ns \geq 0\ ns\ (t_{RDH})$

   ii. When CS is critical

   - Setup time calculation [$T_{1\text{-}1}$ cycle rise]

     $3\ t_{cyc}\ \ (t_{CSD1\ (max)} + t_{CO1\ (max)}) = 45\ ns \geq 15\ ns\ (t_{RDS})$

   - Hold time calculation [$T_{1\text{-}2}$ cycle rise]

     $t_{CSD1\ (min)} + t_{OH\ (min)} = 10\ ns \geq 0\ ns\ (t_{RDH})$

iii. When RD is critical

- Setup time calculation [T_{1-1} cycle fall]

  $2.5\ t_{cyc} - (t_{RSD1\ (max)} + t_{OE\ (max)}) = 60\ ns \geq 15\ ns\ (t_{RDS})$

- Hold time calculation [T_{1-2} cycle rise]

  $t_{RSD2\ (min)} + t_{OH\ (min)} = 10\ ns \geq 0\ ns\ (t_{RDH})$

b. Write cycle

Confirm SRAM t_{DW}, t_{DH}, t_{WP}, t_{CW}, t_{AS}, and t_{WR}.

i. SRAM t_{DW} and t_{DH}

- Input data setting time calculation [T_{1-1} cycle fall]

  $2\ t_{cyc} + t_{WRD2\ (min)} - t_{WDD\ (max)} = 70\ ns \geq 35\ ns\ (t_{DW})$

- Input data hold time calculation

  $t_{WDH\ (min)} = 0.5\ t_{cyc} - 10 = 15\ ns \geq 0\ ns\ (t_{DH})$

ii. SRAM t_{WP} and t_{CW}

- Write pulse width calculation [T_2 cycle rise]

  $1.5\ t_{cyc} + t_{WRD2\ (min)} - t_{WRD1\ (max)} = 55\ ns \geq 55\ ns\ (t_{WP})$

- Chip select time calculation [T_{1-1} cycle rise]

  $3\ t_{cyc} + t_{CSD1\ (min)} - t_{CSD1\ (max)} = 130\ ns \geq 75\ ns\ (t_{CW})$

iii. SRAM t_{AS} and t_{WR}

- Address setup time calculation [T_{1-1} cycle rise]

  $t_{cyc} + t_{WRD1\ (min)} - t_{AD\ (max)} = 30\ ns \geq 0\ ns\ (t_{AS})$

- Address hold time calculation [T_3 cycle fall]

  $0.5\ t_{cyc} + t_{AD\ (min)} - t_{WRD2\ (max)} = 5\ ns \geq 0\ ns\ (t_{WR})$

2. AC Characteristics

a. H8S/2655

Item	Symbol	Min	Max	Unit
Address delay time	t_{AD}	—	20	ns
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	ns
$\overline{RD}$ delay time 1	t_{RSD1}	—	20	ns
$\overline{RD}$ delay time 2	t_{RSD2}	—	20	ns
Read data setup time	t_{RDS}	15	—	ns
Read data hold time	t_{RDH}	0	—	ns
$\overline{WR}$ delay time 1	t_{WRD1}	—	20	ns
$\overline{WR}$ delay time 2	t_{WRD2}	—	20	ns
Write data delay time	t_{WDD}	—	30	ns
Write data hold time	t_{WDH}	$0.5 – Xt_{cyc} – 10$	—	ns

b. HM628128B-8

Item	Symbol	Min	Max	Unit
Address access time	t_{AA}	—	85	ns
Chip select access time	t_{CO1}	—	85	ns
Output enable access time	t_{OE}	—	45	ns
Output hold time	t_{OH}	10	—	ns
Chip select time	t_{CW}	60	—	ns
Address setup time	t_{AS}	0	—	ns
Write pulse width	t_{WP}	50	—	ns
Address hold time	t_{WR}	0	—	ns
Input data setting time	t_{DW}	30	—	ns
Input data hold time	t_{DH}	0	—	ns

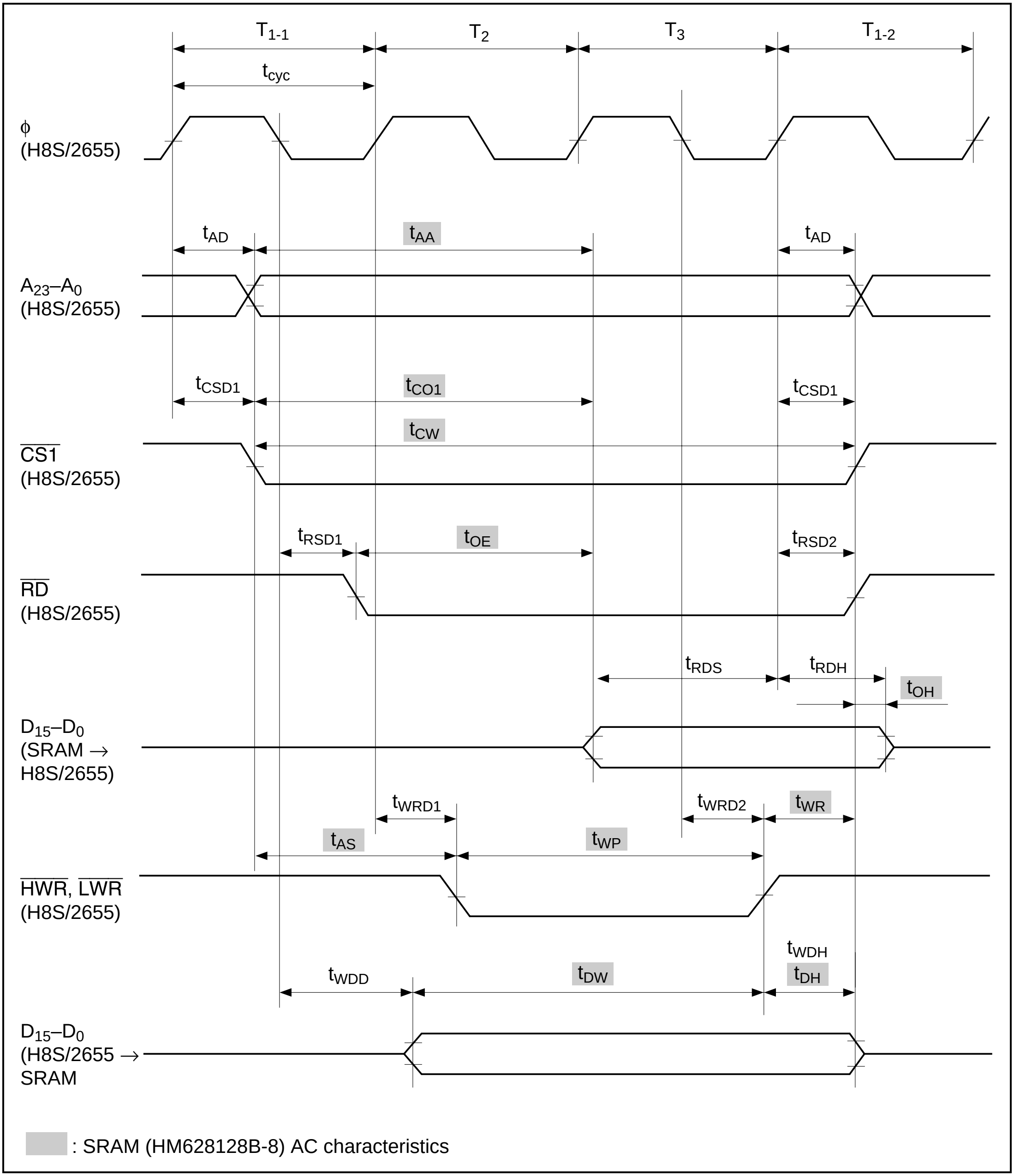


Figure 3.2.4 (c) Read/Write Timing Chart

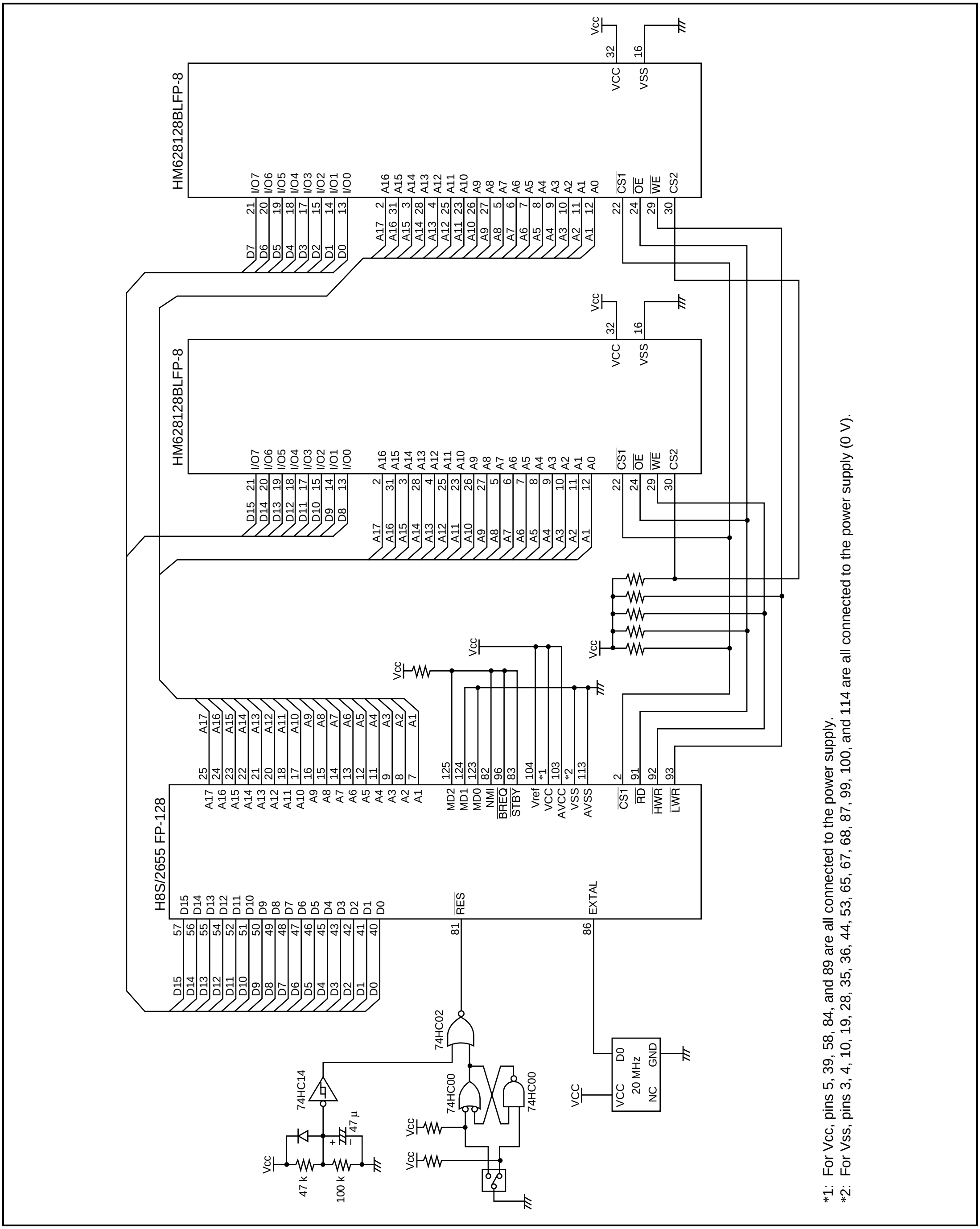


Figure 3.2.4 (d) HM628128BLFP-8 Interface

3.7 DRAM (HM514260C-7) Interface Using 2-CAS Control

DRAM (HM514260C-7) Interface	MCU: H8S/2655	Functions Used: Mode 4 (16-Bit Bus Mode)

Specifications

1. Figure 3.3.1 (a) shows an example of the connection between an H8S/2655 and ×16-bit configuration DRAM (HM514260C-7). The H8S/2655 is set to mode 4 16-bit bus mode, and the DRAM is allocated to area 2. The 2- $\overline{\text{CAS}}$ method is used for byte control.

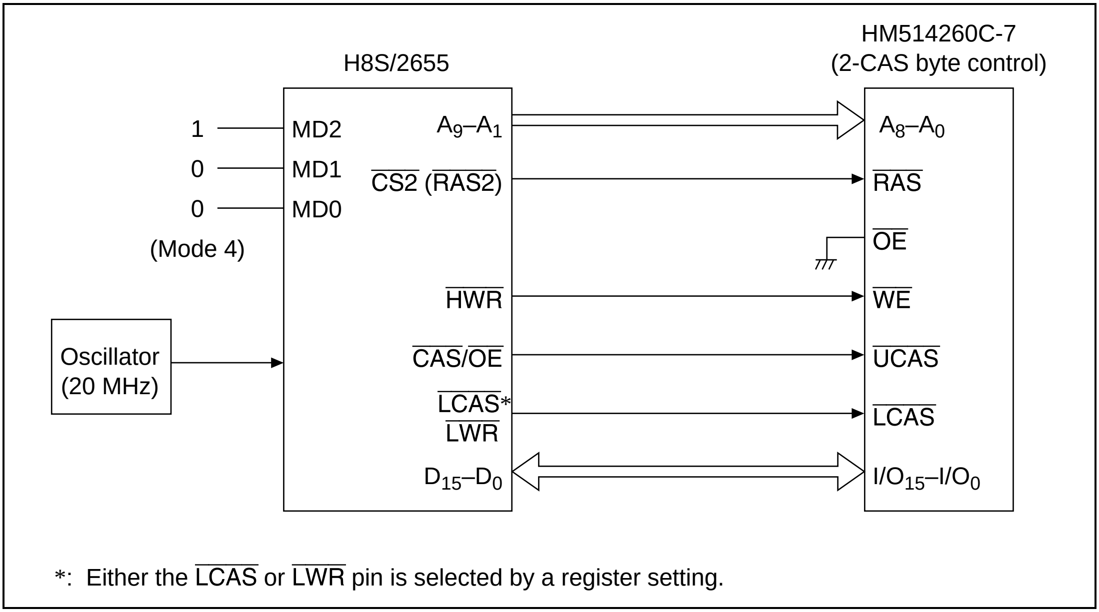


Figure 3.3.1 (a) Example of Connection between H8S/2655 and DRAM

2. Figure 3.3.1 (b) shows the memory map. When the 16-Mbyte address space is divided into areas in 2-Mbyte units, the DRAM area is H'40 0000–H'47 FFFF.

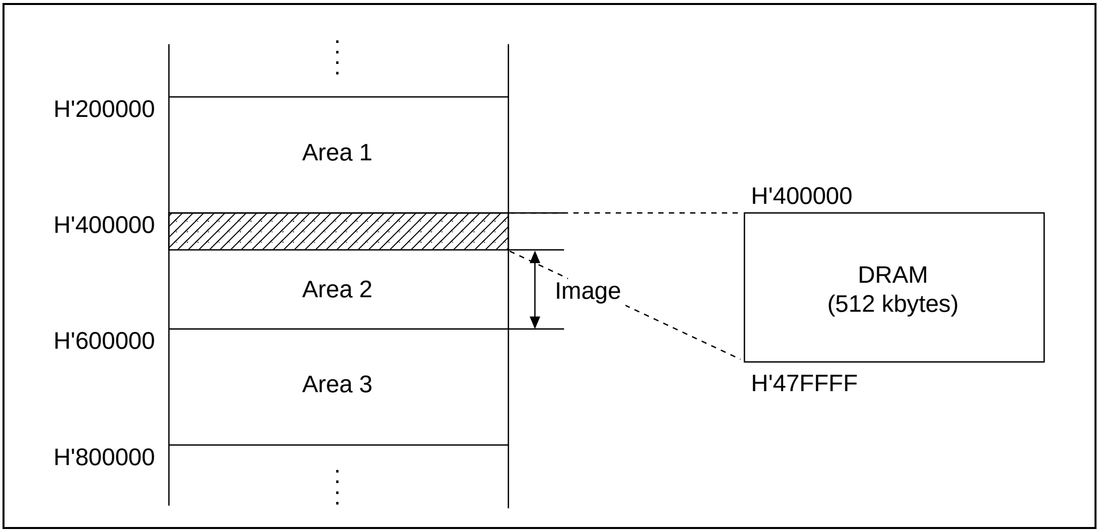


Figure 3.3.1 (b) Memory Map

3. Table 3.3.1 (a) shows the bus controller settings.

Table 3.3.1 (a) Bus Controller Settings

Name	Abbrev.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Setting
Bus width control register	ABWCR	ABW7 *	ABW6 *	ABW5 *	ABW4 *	ABW3 *	ABW2 0	ABW1 *	ABW0 *	Area 2: 16-bit access space
Access state control register	ASTCR	AST7 *	AST6 *	AST5 *	AST4 *	AST3 *	AST2 *	AST1 *	AST0 *	—
Wait control register H	WCRH	W71 *	W70 *	W61 *	W60 *	W51 *	W50 *	W41 *	W40 *	—
Wait control register L	WCRL	W31 *	W30 *	W21 0	W20 1	W11 *	W10 *	W01 *	W00 *	1 program wait state inserted
Bus control register H	BCRH	ICIS1 *	ICIS0 *	BRSTRM *	BRSTS1 *	BRSTS0 *	RMTS2 0	RMTS1 0	RMTS0 1	DRAM space: Area 2
Bus control register L	BCRL	BRLE *	BREQOE *	EAE *	LCASS 0: $\overline{\text{LCAS}}$ pin or 1: $\overline{\text{LWR}}$ pin	DDS *	ASS 1	WDBE *	WAITE *	$\overline{\text{LCAS}}$ signal selected from $\overline{\text{LCAS}}$ and $\overline{\text{LWR}}$ pins Area partition unit: 2 Mbytes (16 Mbytes)
Memory control register	MCR	TPC 0	BE 1	RCDM 0	CW2 0	MXC1 0	MXC0 1	RLW1 0	RLW0 0	1 precharge state Fast page mode $\overline{\text{RAS}}$ up mode 2-$\overline{\text{CAS}}$ control 9-bit shift $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refreshing, no wait
DRAM control register	DRAMCR	RFSHE 1	RCW 0	RMODE 0	CMF *	CMIE 0	CKS2 0	CKS1 0	CKS0 1	Refresh control performed $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refreshing wait state insertion disabled $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refreshing Compare-match interrupts disabled Refresh counter clock: $\phi/2$
Refresh time constant register	RTCOR	0	1	0	0	1	1	1	1	H'4F*1

*: Don't care

*1: The HM514260C-7 uses 512-cycle/8 ms refreshing. To allow for cases where refreshing cannot be performed at the specified time, calculations are based on twice this figure: 1024 cycles/8 ms. With a refresh counter clock of $\phi/2$ (100 ns), the RTCOR value is (8 ms/1024 cycles) / 100 ns $\cong$ 79 (= H'4F).

Operation

The calculations used to check whether the AC characteristics are satisfied in DRAM access are shown below. The t_{cyc} value, unspecified min value, and unspecified max value are as follows.

- t_{cyc}: 50 ns (20 MHz oscillator (= ϕ))
- Unspecified min value: 0 ns
- Unspecified max value: min value

In the times obtained based on ϕ, the reference timing is shown in [ ].

For the timing values, see 5. AC Characteristics below.

1. Read Access

   Figure 3.3.1 (c) shows the DRAM read timing chart. Confirm that the following AC characteristics are satisfied.

Item		Symbol
DRAM (HM514260C-7)	Row address setup time	t_{ASR}
	Row address hold time	t_{RAH}
	Column address setup time	t_{ASC}
	Column address hold time	t_{CAH}
	$\overline{\text{RAS}}$-$\overline{\text{CAS}}$ delay time	t_{RCD}
	$\overline{\text{RAS}}$-column address delay time	t_{RAD}
	$\overline{\text{RAS}}$ precharge time	t_{RP}
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}

a. DRAM

i. Row address setup time calculation [T_{r-1} cycle rise]

$0.5\ t_{cyc} + t_{CSD2\ (min)} - t_{AD\ (max)} = 5\text{ns} \geq 0\text{ ns}\ (t_{ASR})$

ii. Row address hold time calculation

$t_{AH\ (min)} = 0.5\ t_{cyc} - 10 = 15\text{ ns} \geq 10\text{ ns}\ (t_{RAH})$

iii. Column address setup time calculation [T_{c1-1} cycle rise]

$t_{cyc} + t_{CASD\ (min)} - t_{AD\ (max)} = 30\text{ ns} \geq 0\text{ ns}\ (t_{ASC})$

iv. Column address hold time calculation [T_{w-1} cycle rise]

$2\ t_{cyc} + t_{AD\ (min)} - t_{CASD\ (max)} = 80\text{ ns} \geq 15\text{ ns}\ (t_{CAH})$

v. $\overline{RAS}$-$\overline{CAS}$ delay time calculation [T_{r-1} cycle fall]

$1.5\ t_{cyc} + t_{CASD\ (min)} - t_{CSD2\ (max)} = 55\ ns \geq 20\ ns\ (t_{RCD})$

vi. $\overline{RAS}$-column address delay time calculation

$t_{AH\ (min)} = 0.5\ t_{cyc} - 10 = 15\ ns \geq 15\ ns\ (t_{RAD})$

vii. $\overline{RAS}$ precharge time calculation [T_{p-3} cycle rise]

$1.5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD1\ (max)} = 55\ ns \geq 50\ ns\ (t_{RP})$

b. H8S/2655

i. Read data setup time calculation [T_{w-1} cycle rise]

$2\ t_{cyc} - t_{CASD\ (max)} + t_{CAC\ (max)} = 60\ ns \geq 15\ ns\ (t_{RDS})$

Note: Access times are specified as follows according to t_{RCD} and t_{RAD}.

Conditions	Applicable Time
t_{RCD} (calculated value) $\geq t_{RCD}$ (max) and t_{RAD} (calculated value) $\leq t_{RAD}$ (max)	Access time from $\overline{CAS}$ (t_{CAC})
t_{RCD} (calculated value) $\leq t_{RCD}$ (max) and t_{RAD} (calculated value) $\geq t_{RAD}$ (max)	Access time from address (t_{AA})
t_{RCD} (calculated value) $\leq t_{RCD}$ (max) and t_{RAD} (calculated value) $\leq t_{RAD}$ (max)	Access time from $\overline{RAS}$ (t_{RAC})

ii. Read data hold time calculation [T_{c1-2} cycle rise]

$t_{CASD\ (min)} + t_{OFF1\ (min)} = 0\ ns \geq 0\ ns\ (t_{RDH})$

2. Write Access

Figure 3.3.1 (d) shows the DRAM write timing chart. Confirm that the following AC characteristics are satisfied.

Item		Symbol
DRAM (HM514260C-7)	Write command setup time	t_{WCS}
	Write command hold time	t_{WCH}
	Write input setup time	t_{DS}
	Write input hold time	t_{DH}

a. Write command setup time calculation

$t_{WCS\ (min)} = 0.5\ t_{cyc} - 10 = 15\ ns \geq 0\ ns\ (t_{WCS})$

b. Write command hold time calculation [T_{w-1} cycle rise]

$1.5\ t_{cyc} - t_{CASD\ (max)} = 55\ ns \geq 15\ ns\ (t_{WCH})$

c. Write input setup time calculation

$t_{WDS\,(min)} = 0.5\ t_{cyc} - 20 = 5\text{ ns} \geq 0\text{ ns } (t_{DS})$

d. Write input hold time calculation [$T_{w\text{-}1}$ cycle rise]

$1.5\ t_{cyc} + t_{WRD1\,(min)} + t_{WDH\,(min)} - t_{CASD\,(max)} = 55\text{ ns} \geq 15\text{ ns } (t_{DH})$

3. Burst Mode

a. Fast page mode

In fast page mode, confirm that the following AC characteristics are satisfied.

Item		Symbol
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}
DRAM (HM514260C-7)	Fast page mode $\overline{CAS}$ precharge time	t_{CP}
	Fast page mode cycle time	t_{PC}
	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}

i. H8S/2655

i-1 Read data setup time calculation [$T_{c1\text{-}2}$ cycle rise]

$3\ t_{cyc} - t_{CASD\,(max)} - t_{ACP\,(max)} = 90\text{ ns} \geq 15\text{ ns } (t_{RDS})$

i-2 Read data hold time calculation [$T_{p\text{-}3}$ cycle rise]

$t_{CSD1\,(min)} + t_{OFF1\,(min)} = 0\text{ ns} \geq 0\text{ ns } (t_{RDH})$

ii. DRAM

ii-1 Fast page mode $\overline{CAS}$ precharge time calculation [$T_{c1\text{-}2}$ cycle rise]

$t_{cyc} + t_{CASD\,(min)} - t_{CASD\,(max)} = 30\text{ ns} \geq 10\text{ ns } (t_{CP})$

ii-2 Fast page mode cycle time calculation [$T_{w\text{-}1}$ cycle rise]

$3\ t_{cyc} + t_{CASD\,(min)} - t_{CASD\,(max)} = 130\text{ ns} \geq 45\text{ ns } (t_{PC})$

ii-3 $\overline{RAS}$ hold time from $\overline{CAS}$ precharge calculation [$T_{c1\text{-}2}$ cycle rise]

$3\ t_{cyc} + t_{CSD1\,(min)} - t_{CASD\,(max)} = 130\text{ ns} \geq 40\text{ ns } (t_{RHCP})$

b. $\overline{RAS}$ down mode

$\overline{RAS}$ down mode can be selected by setting the RCDM bit to 1 in the memory control register (MCR). This mode cannot be selected when the $\overline{LWR}$ pin is used for the $\overline{LCAS}$ signal.

4. Refresh Cycle ($\overline{CAS}$-Before-$\overline{RAS}$ Refreshing)

Figures 3.3.1 (e) and 3.3.1 (f) show the $\overline{CAS}$-before-$\overline{RAS}$ refresh timing charts. Confirm that the following AC characteristics are satisfied.

Item		Symbol
DRAM (HM514260C-7)	$\overline{RAS}$ precharge time	t_{RP}
	$\overline{CAS}$ setup time	t_{CSR}
	$\overline{RAS}$ pulse width	t_{RAS}
	$\overline{CAS}$ hold time	t_{CHR}
	Normal mode $\overline{CAS}$ precharge time	t_{CPN}
	Random read/write cycle time	t_{RC}

a. $\overline{RAS}$ precharge time

i. Transition from normal cycle to refresh cycle [T_{Rp} cycle rise]

$1.5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD1\ (max)} = 55\ ns \geq 50\ ns\ (t_{RP})$

ii. Transition from refresh cycle to normal cycle

ii-1 When using $\overline{LCAS}$ pin for $\overline{LCAS}$ signal [T_p cycle rise]

$1.5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD1\ (max)} = 55\ ns \geq 50\ ns\ (t_{RP})$

ii-2 When using $\overline{LWR}$ pin for $\overline{LCAS}$ signal [T_{RI} cycle rise]

$2.5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD1\ (max)} = 105\ ns \geq 50\ ns\ (t_{RP})$

b. $\overline{CAS}$ setup time

$t_{CSR\ (min)} = 15\ ns \geq 10\ ns\ (t_{CSR})$

c. $\overline{RAS}$ pulse width [T_{Rr} cycle fall]

$2.5\ t_{cyc} + t_{CSD1\ (min)} - t_{CSD2\ (max)} = 105\ ns \geq 70\ ns\ (t_{RAS})$

d. $\overline{CAS}$ hold time [T_{Rr} cycle fall]

$2.5\ t_{cyc} + t_{CASD\ (min)} - t_{CSD2\ (max)} = 105\ ns \geq 10\ ns\ (t_{CHR})$

e. Normal mode $\overline{CAS}$ precharge time

i. Transition from normal cycle to refresh cycle [T_{Rp} cycle rise]

$t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 70\ ns \geq 10\ ns\ (t_{CPN})$

ii. Transition from refresh cycle to normal cycle

ii-1 When using $\overline{LCAS}$ pin for $\overline{LCAS}$ signal [T_p cycle rise]

$3\ t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 130\ ns \geq 10\ ns\ (t_{CPN})$

ii-2 When using $\overline{LWR}$ pin for $\overline{LCAS}$ signal [T_{RI} cycle rise]

$4\ t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 180\ ns \geq 10\ ns\ (t_{CPN})$

f. Random read/write cycle time [T_{Rr} cycle fall]

i. When using $\overline{LCAS}$ pin for $\overline{LCAS}$ signal

$4\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD2\ (max)} = 180$ ns ≥ 130 ns (t_{RC})

ii. When using $\overline{LWR}$ pin for $\overline{LCAS}$ signal

$5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD2\ (max)} = 230$ ns ≥ 130 ns (t_{RC})

5. AC Characteristics

Table 3.3.1 (b) shows the AC characteristics of the H8S/2655, and table 3.3.1. (c) the AC characteristics of the HM514260C-7.

Table 3.3.1 (b) AC Characteristics of H8S/2655

Item	Symbol	Min	Max	Unit
Address delay time	t_{AD}	—	20	ns
Address hold time	t_{AH}	$0.5 \times t_{cyc} - 10$	—	ns
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	ns
$\overline{CS}$ delay time 2	t_{CSD2}	—	20	ns
$\overline{CAS}$ delay time	t_{CASD}	—	20	ns
Read data setup time	t_{RDS}	15	—	ns
Read data hold time	t_{RDH}	0	—	ns
$\overline{WR}$ delay time 1	t_{WRD1}	—	20	ns
Write data setup time	t_{WDS}	$0.5 \times t_{cyc} - 20$	—	ns
Write data hold time	t_{WDH}	$0.5 \times t_{cyc} - 10$	—	ns
$\overline{WR}$ setup time	t_{WCS}	$0.5 \times t_{cyc} - 10$	—	ns

Table 3.3.1 (c) AC Characteristics of HM514260C-7

Item	Symbol	Min	Max	Unit
Random read/write cycle time	t_{RC}	130	—	ns
$\overline{RAS}$ precharge time	t_{RP}	50	—	ns
$\overline{RAS}$ pulse width	t_{RAS}	70	10000	ns
Row address setup time	t_{ASR}	0	—	ns
Row address hold time	t_{RAH}	10	—	ns
Column address setup time	t_{ASC}	0	—	ns
Column address hold time	t_{CAH}	15	—	ns
$\overline{RAS}$-$\overline{CAS}$ delay time	t_{RCD}	20	50	ns
$\overline{RAS}$-column address delay time	t_{RAD}	15	35	ns
Access time from $\overline{RAS}$	t_{RAC}	—	70	ns
Access time from $\overline{CAS}$	t_{CAC}	—	20	ns
Access time from address	t_{AA}	—	35	ns
Output buffer turn-off time	t_{OFF1}	0	15	ns
Write command setup time	t_{WCS}	0	—	ns
Write command hold time	t_{WCH}	15	—	ns
Data input setup time	t_{DS}	0	—	ns
Data input hold time	t_{DH}	15	—	ns
$\overline{CAS}$ setup time	t_{CSR}	10	—	ns
$\overline{CAS}$ hold time	t_{CHR}	10	—	ns
Normal mode $\overline{CAS}$ precharge time	t_{CPN}	10	—	ns
Fast page mode cycle time	t_{PC}	45	—	ns
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	ns
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	ns
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40	—	ns

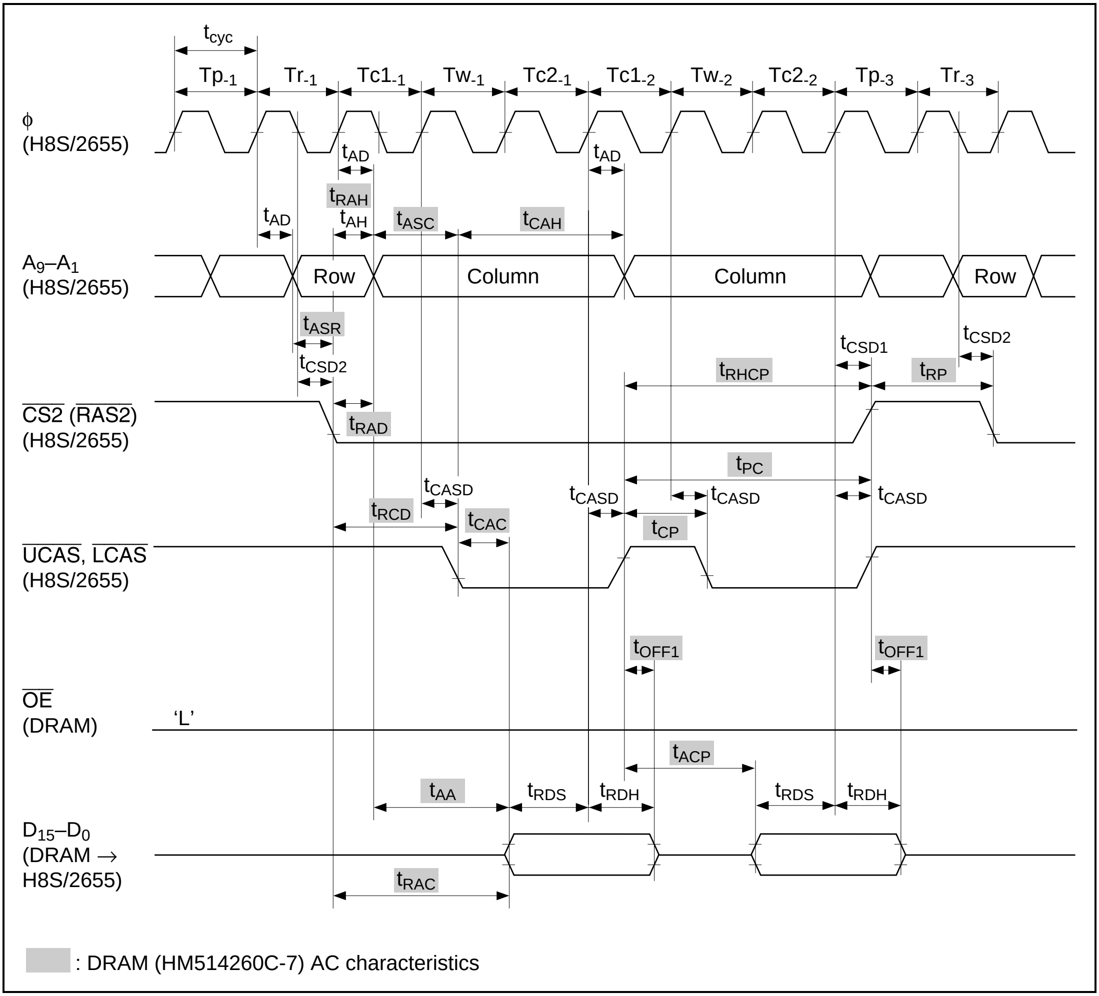


Figure 3.3.1 (c) DRAM Read Timing Chart

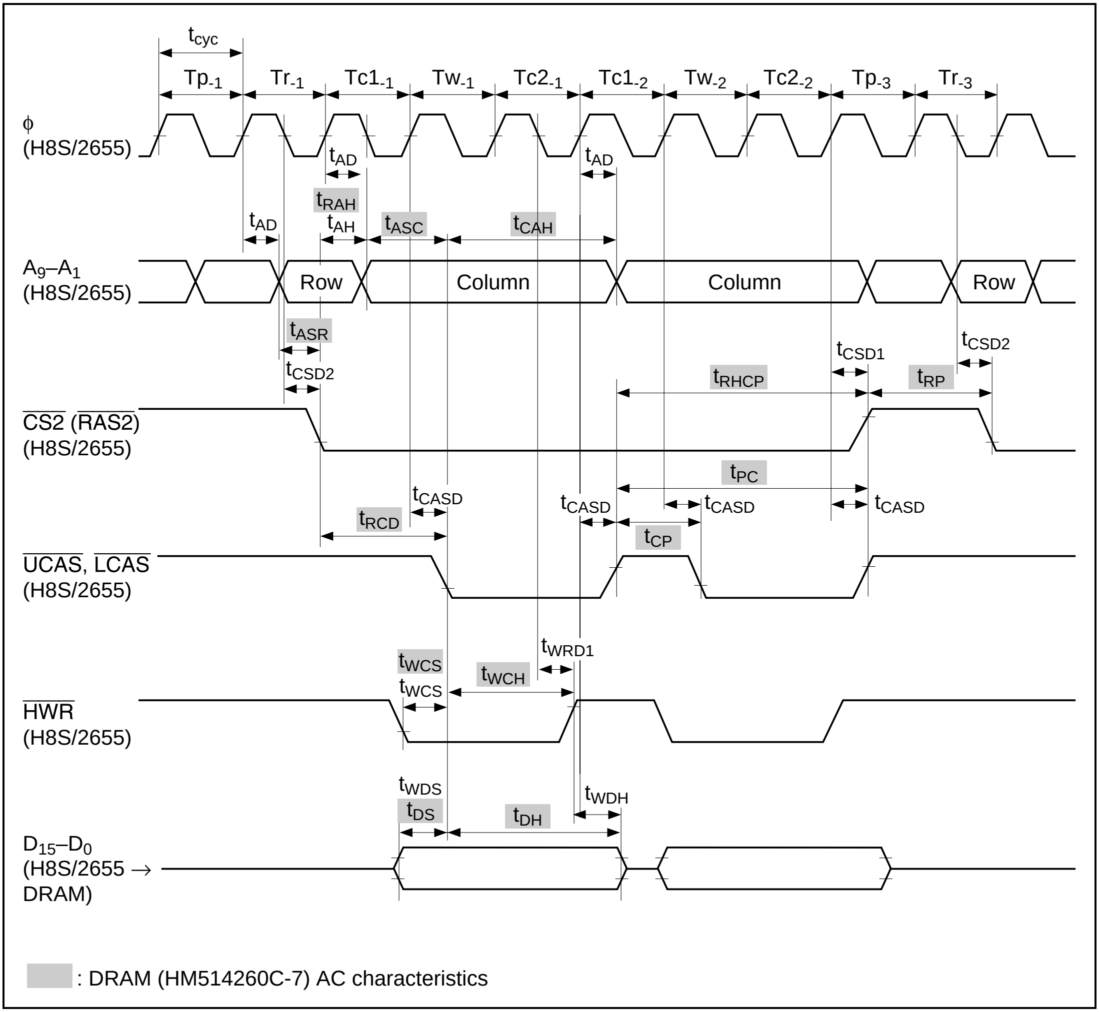


Figure 3.3.1 (d) DRAM Write Timing Chart

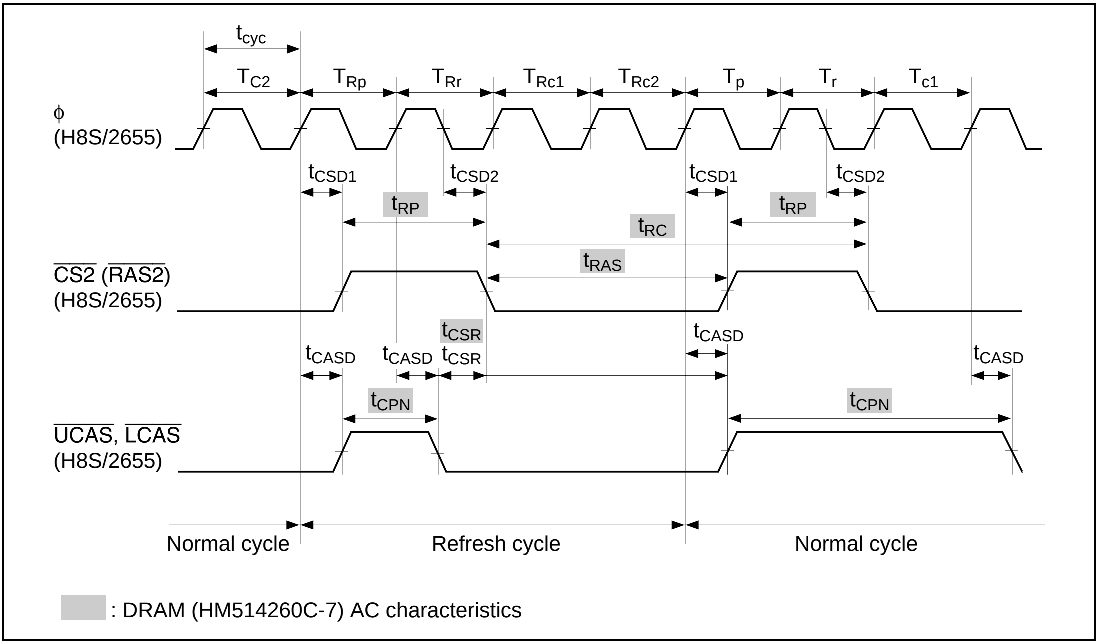


Figure 3.3.1 (e) $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Timing Chart ($\overline{\text{LCAS}}$ Pin Used for $\overline{\text{LCAS}}$ Signal)

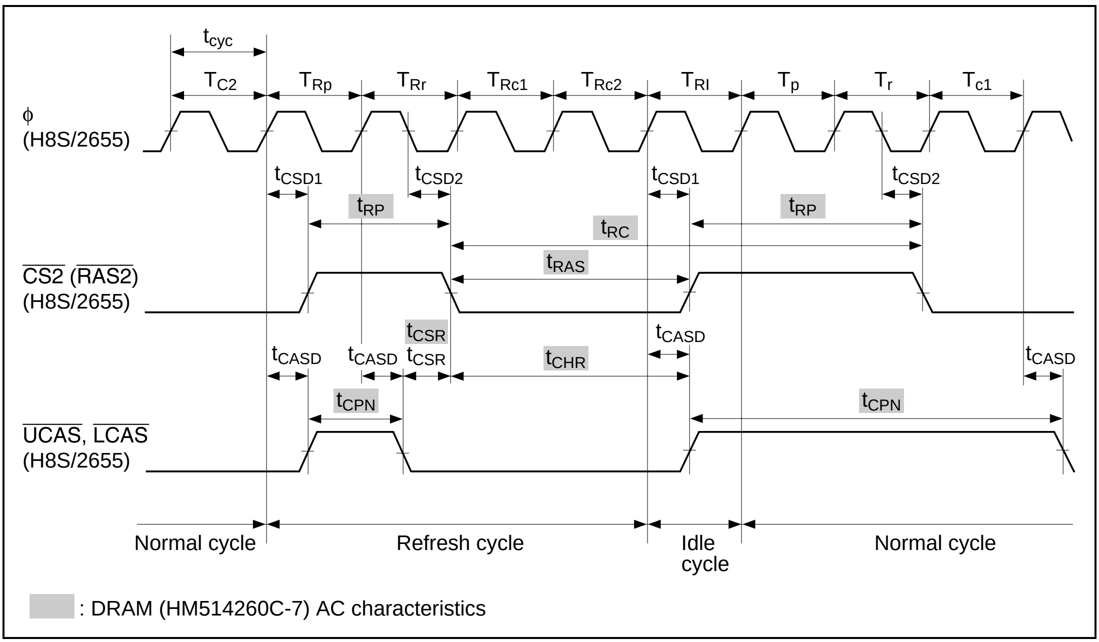


Figure 3.3.1 (f) $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Timing Chart ($\overline{\text{LWR}}$ Pin Used for $\overline{\text{LCAS}}$ Signal)

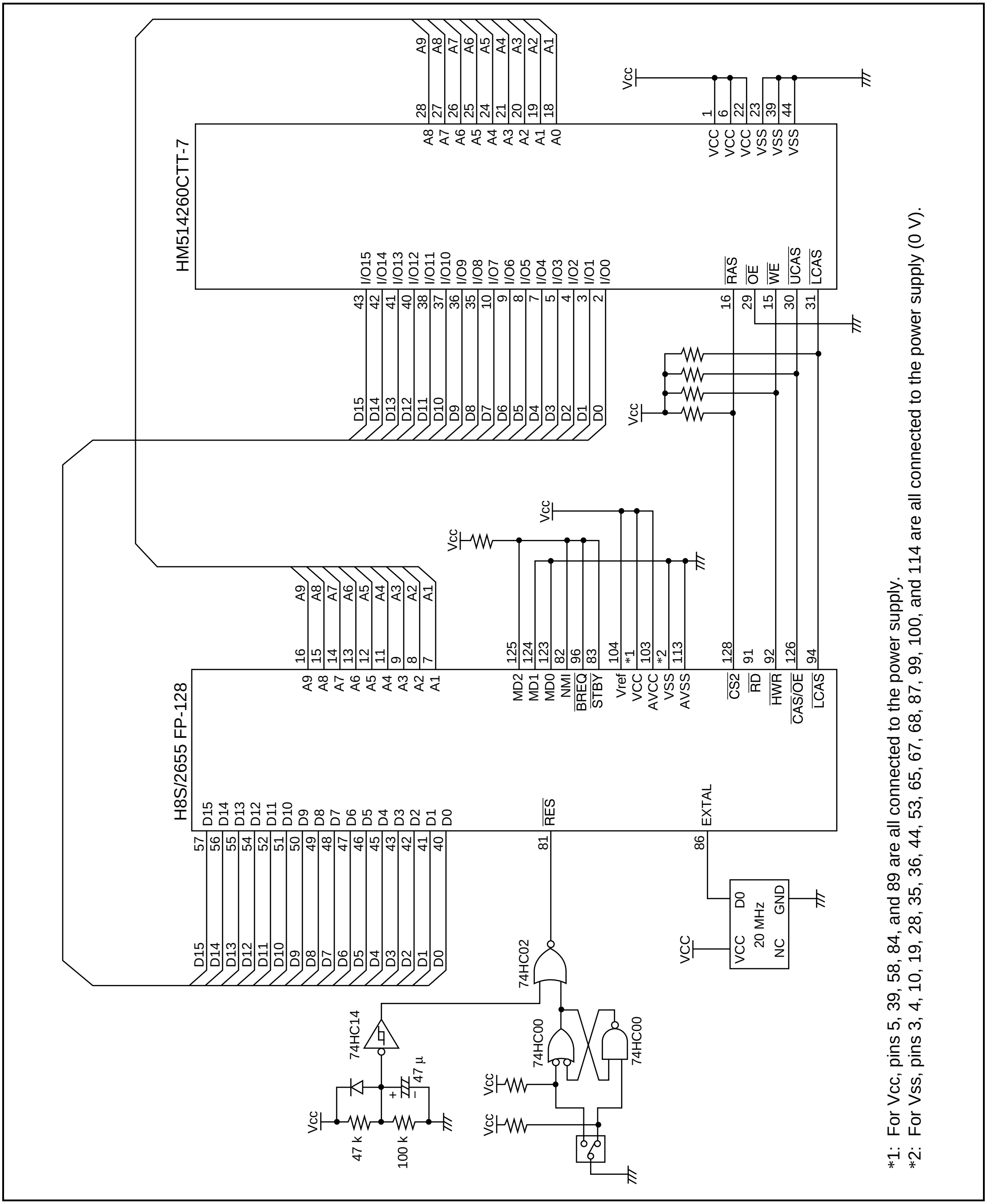


Figure 3.3.1 (g) HM514260CTT-7 Interface ($\overline{\text{LCAS}}$ Pin Used for $\overline{\text{LCAS}}$ Signal)

3.8 DRAM (HM514270C-7) Interface Using 2-WE Control

DRAM (HM514270C-7) Interface	MCU: H8S/2655	Functions Used: Mode 4 (16-Bit Bus Mode)

Specifications

1. Figure 3.3.2 (a) shows an example of the connection between an H8S/2655 and ×16-bit configuration DRAM (HM514270C-7). The H8S/2655 is set to mode 4 16-bit bus mode, and the DRAM is allocated to area 2. The 2- $\overline{\text{WE}}$ method is used for byte control.

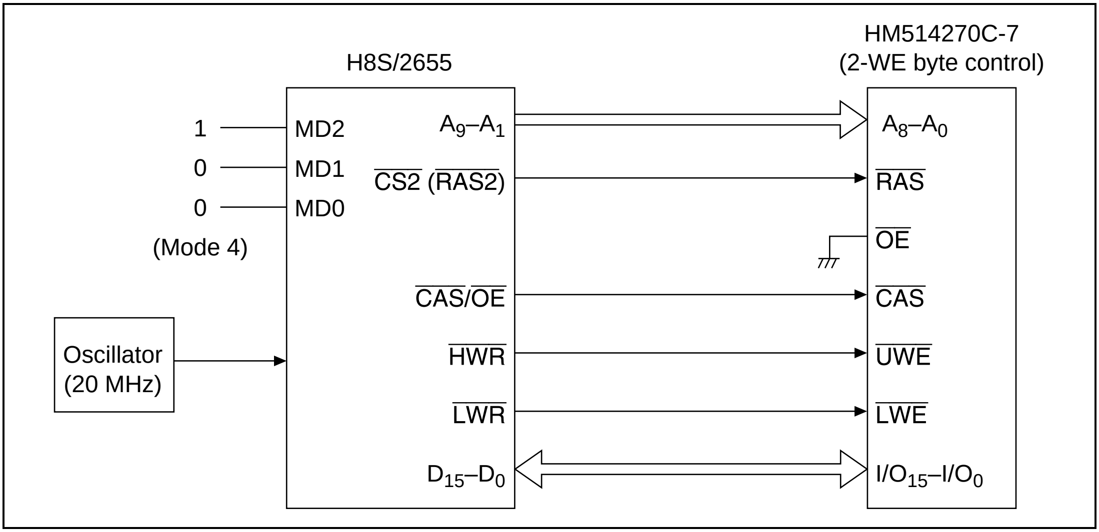


Figure 3.3.2 (a) Example of Connection between H8S/2655 and DRAM

2. Figure 3.3.2 (b) shows the memory map. When the 16-Mbyte address space is divided into areas in 2-Mbyte units, the DRAM area is H'40 0000–H'47 FFFF.

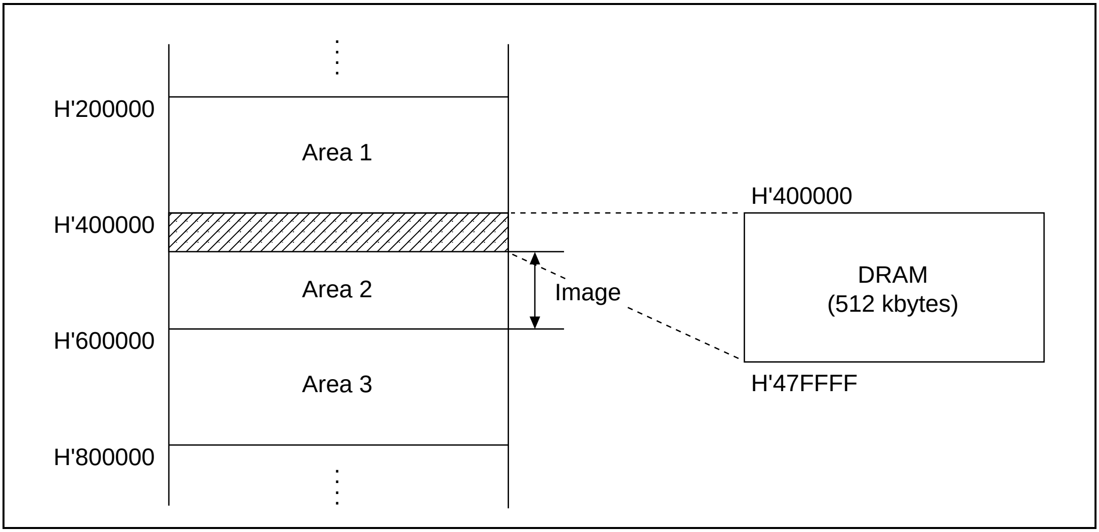


Figure 3.3.2 (b)   Memory Map

3. Table 3.3.2 (a) shows the bus controller settings.

Table 3.3.2 (a) Bus Controller Settings

Name	Abbrev.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Setting
Bus width control register	ABWCR	ABW7	ABW6	ABW5	ABW4	ABW3	ABW2	ABW1	ABW0	
		*	*	*	*	*	0	*	*	Area 2: 16-bit access space
Access state control register	ASTCR	AST7	AST6	AST5	AST4	AST3	AST2	AST1	AST0	
		*	*	*	*	*	*	*	*	—
Wait control register H	WCRH	W71	W70	W61	W60	W51	W50	W41	W40	
		*	*	*	*	*	*	*	*	—
Wait control register L	WCRL	W31	W30	W21	W20	W11	W10	W01	W00	
		*	*	0	1	*	*	*	*	1 program wait state inserted
Bus control register H	BCRH	ICIS1	ICIS0	BRSTRM	BRSTS1	BRSTS0	RMTS2	RMTS1	RMTS0	
		*	*	*	*	*	0	0	1	DRAM space: Area 2
Bus control register L	BCRL	BRLE	BREQOE	EAE	LCASS	DDS	ASS	WDBE	WAITE	
		*	*	*	*	*	1	*	*	Area partition unit: 2 Mbytes (16 Mbytes)
Memory control register	MCR	TPC	BE	RCDM	CW2	MXC1	MXC0	RLW1	RLW0	
		0	1	0	1	0	1	0	0	1 precharge state Fast page mode $\overline{\text{RAS}}$ up mode 2-$\overline{\text{WE}}$ control 9-bit shift $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refreshing, no wait
DRAM control register	DRAMCR	RFSHE	RCW	RMODE	CMF	CMIE	CKS2	CKS1	CKS0	
		1	0	0	*	0	0	0	1	Refresh control performed $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refreshing wait state insertion disabled $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refreshing Compare-match interrupts disabled Refresh counter clock: $\phi/2$
Refresh time constant register	RTCOR	0	1	0	0	1	1	1	1	H'4F*1

*: Don't care

*1: The HM514270C-7 uses 512-cycle/8 ms refreshing. To allow for cases where refreshing cannot be performed at the specified time, calculations are based on twice this figure: 1024 cycles/8 ms. With a refresh counter clock of $\phi/2$ (100 ns), the RTCOR value is (8 ms/1024 cycles) / 100 ns $\cong$ 79 (= H'4F).

Operation

The calculations used to check whether the AC characteristics are satisfied in DRAM access are shown below. The t_{cyc} value, unspecified min value, and unspecified max value are as follows.

- t_{cyc}: 50 ns (20 MHz oscillator (= ϕ))
- Unspecified min value: 0 ns
- Unspecified max value: min value

In the times obtained based on ϕ, the reference timing is shown in [ ].

For the timing values, see 5. AC Characteristics below.

1. Read Access

   Figure 3.3.2 (c) shows the DRAM read timing chart. Confirm that the following AC characteristics are satisfied.

Item		Symbol
DRAM (HM514270C-7)	Row address setup time	t_{ASR}
	Row address hold time	t_{RAH}
	Column address setup time	t_{ASC}
	Column address hold time	t_{CAH}
	$\overline{RAS}$-$\overline{CAS}$ delay time	t_{RCD}
	$\overline{RAS}$-column address delay time	t_{RAD}
	$\overline{RAS}$ precharge time	t_{RP}
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}

   a. DRAM

      i. Row address setup time calculation [T_{r-1} cycle rise]

      $0.5\ t_{cyc} + t_{CSD2\ (min)} - t_{AD\ (max)} = 5ns \geq 0\ ns\ (t_{ASR})$

      ii. Row address hold time calculation

      $t_{AH\ (min)} = 0.5\ t_{cyc} - 10 = 15\ ns \geq 10\ ns\ (t_{RAH})$

      iii. Column address setup time calculation [T_{c1} cycle rise]

      $t_{cyc} + t_{CASD\ (min)} - t_{AD\ (max)} = 30\ ns \geq 0\ ns\ (t_{ASC})$

      iv. Column address hold time calculation [T_{w-1} cycle rise]

      $2\ t_{cyc} + t_{AD\ (min)} - t_{CASD\ (max)} = 80\ ns \geq 15\ ns\ (t_{CAH})$

v. $\overline{RAS}$-$\overline{CAS}$ delay time calculation [T_{r-1} cycle fall]

$1.5\ t_{cyc} + t_{CASD\ (min)} - t_{CSD2\ (max)} = 55\ ns \geq 20\ ns\ (t_{RCD})$

vi. $\overline{RAS}$-column address delay time calculation

$t_{AH\ (min)} = 0.5\ t_{cyc} - 10 = 15\ ns \geq 15\ ns\ (t_{RAD})$

vii. $\overline{RAS}$ precharge time calculation [T_{p-3} cycle rise]

$1.5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD1\ (max)} = 55\ ns \geq 50\ ns\ (t_{RP})$

b. H8S/2655

i. Read data setup time calculation [T_{w-1} cycle rise]

$2\ t_{cyc} - t_{CASD\ (max)} + t_{CAC\ (max)} = 60\ ns \geq 15\ ns\ (t_{RDS})$

Note: Access times are specified as follows according to t_{RCD} and t_{RAD}.

Conditions	**Applicable Time**
t_{RCD} (calculated value) ≥ t_{RCD} (max) and t_{RAD} (calculated value) ≤ t_{RAD} (max)	Access time from $\overline{CAS}$ (t_{CAC})
t_{RCD} (calculated value) ≤ t_{RCD} (max) and t_{RAD} (calculated value) ≥ t_{RAD} (max)	Access time from address (t_{AA})
t_{RCD} (calculated value) ≤ t_{RCD} (max) and t_{RAD} (calculated value) ≤ t_{RAD} (max)	Access time from $\overline{RAS}$ (t_{RAC})

ii. Read data hold time calculation [T_{c1-2} cycle rise]

$t_{CASD\ (min)} + t_{OFF1\ (min)} = 0\ ns \geq 0\ ns\ (t_{RDH})$

2. Write Access

Figure 3.3.2 (d) shows the DRAM write timing chart. Confirm that the following AC characteristics are satisfied.

Item		**Symbol**
DRAM (HM514270C-7)	Write command setup time	t_{WCS}
	Write command hold time	t_{WCH}
	Write input setup time	t_{DS}
	Write input hold time	t_{DH}

a. Write command setup time calculation

$t_{WCS\ (min)} = 0.5\ t_{cyc} - 10 = 15\ ns \geq 0\ ns\ (t_{WCS})$

b. Write command hold time calculation [T_{w-1} cycle rise]

$1.5\ t_{cyc} - t_{CASD\ (max)} = 55\ ns \geq 15\ ns\ (t_{WCH})$

c. Write input setup time calculation

$t_{WDS\ (min)} = 0.5\ t_{cyc} - 20 = 5\ ns \geq 0\ ns\ (t_{DS})$

d. Write input hold time calculation [T_{w-1} cycle rise]

$1.5\ t_{cyc} + t_{WRD1\ (min)} + t_{WDH\ (min)} - t_{CASD\ (max)} = 55\ ns \geq 15\ ns\ (t_{DH})$

3. Burst Mode

a. Fast page mode

In fast page mode, confirm that the following AC characteristics are satisfied.

Item		Symbol
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}
DRAM (HM514270C-7)	Fast page mode $\overline{CAS}$ precharge time	t_{CP}
	Fast page mode cycle time	t_{PC}
	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}

i. H8S/2655

i-1 Read data setup time calculation [T_{c1-2} cycle rise]

$3\ t_{cyc} - t_{CASD\ (max)} - t_{ACP\ (max)} = 90\ ns \geq 15\ ns\ (t_{RDS})$

i-2 Read data hold time calculation [T_{p-3} cycle rise]

$t_{CSD1\ (min)} + t_{OFF1\ (min)} = 0\ ns \geq 0\ ns\ (t_{RDH})$

ii. DRAM

ii-1 Fast page mode $\overline{CAS}$ precharge time calculation [T_{c1-2} cycle rise]

$t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 30\ ns \geq 10\ ns\ (t_{CP})$

ii-2 Fast page mode cycle time calculation [T_{w-1} cycle rise]

$3\ t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 130\ ns \geq 45\ ns\ (t_{PC})$

ii-3 $\overline{RAS}$ hold time from $\overline{CAS}$ precharge calculation [T_{c1-2} cycle rise]

$3\ t_{cyc} + t_{CSD1\ (min)} - t_{CASD\ (max)} = 130\ ns \geq 40\ ns\ (t_{RHCP})$

b. $\overline{RAS}$ down mode

$\overline{RAS}$ down mode can be selected by setting the RCDM bit to 1 in the memory control register (MCR).

4. Refresh Cycle ($\overline{CAS}$-Before-$\overline{RAS}$ Refreshing)

Figure 3.3.2 (e) shows the $\overline{CAS}$-before-$\overline{RAS}$ refresh timing chart. Confirm that the following AC characteristics are satisfied.

Item		Symbol
DRAM (HM514270C-7)	$\overline{RAS}$ precharge time	t_{RP}
	$\overline{CAS}$ setup time	t_{CSR}
	$\overline{RAS}$ pulse width	t_{RAS}
	$\overline{CAS}$ hold time	t_{CHR}
	Normal mode $\overline{CAS}$ precharge time	t_{CPN}
	Random read/write cycle time	t_{RC}

a. $\overline{RAS}$ precharge time

i. Transition from normal cycle to refresh cycle [T_{Rp} cycle rise]

$1.5\ t_{cyc} + t_{CSD2\ (min)} – t_{CSD1\ (max)} = 55\ ns \geq 50\ ns\ (t_{RP})$

ii. Transition from refresh cycle to normal cycle [T_p cycle rise]

$1.5\ t_{cyc} + t_{CSD2\ (min)} – t_{CSD1\ (max)} = 55\ ns \geq 50\ ns\ (t_{RP})$

b. $\overline{CAS}$ setup time

$t_{CSR\ (min)} = 15\ ns \geq 10\ ns\ (t_{CSR})$

c. $\overline{RAS}$ pulse width [T_{Rr} cycle fall]

$2.5\ t_{cyc} + t_{CSD1\ (min)} – t_{CSD2\ (max)} = 105\ ns \geq 70\ ns\ (t_{RAS})$

d. $\overline{CAS}$ hold time [T_{Rr} cycle fall]

$2.5\ t_{cyc} + t_{CASD\ (min)} – t_{CSD2\ (max)} = 105\ ns \geq 10\ ns\ (t_{CHR})$

e. Normal mode $\overline{CAS}$ precharge time

i. Transition from normal cycle to refresh cycle [T_{Rp} cycle rise]

$t_{cyc} + t_{CASD\ (min)} – t_{CASD\ (max)} = 70\ ns \geq 10\ ns\ (t_{CPN})$

ii. Transition from refresh cycle to normal cycle [T_{Rp} cycle rise]

$3\ t_{cyc} + t_{CASD\ (min)} – t_{CASD\ (max)} = 130\ ns \geq 10\ ns\ (t_{CPN})$

f. Random read/write cycle time [T_{Rr} cycle fall]

$4\ t_{cyc} + t_{CSD2\ (min)} – t_{CSD2\ (max)} = 180\ ns \geq 130\ ns\ (t_{RC})$

5. AC Characteristics

Table 3.3.2 (b) shows the AC characteristics of the H8S/2655, and table 3.3.2. (c) the AC characteristics of the HM514270C-7.

Table 3.3.2 (b) AC Characteristics of H8S/2655

Item	Symbol	Min	Max	Unit
Address delay time	t_{AD}	—	20	ns
Address hold time	t_{AH}	$0.5 \times t_{cyc} - 10$	—	ns
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	ns
$\overline{CS}$ delay time 2	t_{CSD2}	—	20	ns
$\overline{CAS}$ delay time	t_{CASD}	—	20	ns
Read data setup time	t_{RDS}	15	—	ns
Read data hold time	t_{RDH}	0	—	ns
$\overline{WR}$ delay time 1	t_{WRD1}	—	20	ns
Write data setup time	t_{WDS}	$0.5 \times t_{cyc} - 20$	—	ns
Write data hold time	t_{WDH}	$0.5 \times t_{cyc} - 10$	—	ns
$\overline{WR}$ setup time	t_{WCS}	$0.5 \times t_{cyc} - 10$	—	ns

Table 3.3.2 (c) AC Characteristics of HM514270C-7

Item	Symbol	Min	Max	Unit
Random read/write cycle time	t_{RC}	130	—	ns
$\overline{RAS}$ precharge time	t_{RP}	50	—	ns
$\overline{RAS}$ pulse width	t_{RAS}	70	10000	ns
Row address setup time	t_{ASR}	0	—	ns
Row address hold time	t_{RAH}	10	—	ns
Column address setup time	t_{ASC}	0	—	ns
Column address hold time	t_{CAH}	15	—	ns
$\overline{RAS}$-$\overline{CAS}$ delay time	t_{RCD}	20	50	ns
$\overline{RAS}$-column address delay time	t_{RAD}	15	35	ns
Access time from $\overline{RAS}$	t_{RAC}	—	70	ns
Access time from $\overline{CAS}$	t_{CAC}	—	20	ns
Access time from address	t_{AA}	—	35	ns
Output buffer turn-off time	t_{OFF1}	0	15	ns
Write command setup time	t_{WCS}	0	—	ns
Write command hold time	t_{WCH}	15	—	ns
Data input setup time	t_{DS}	0	—	ns
Data input hold time	t_{DH}	15	—	ns
$\overline{CAS}$ setup time	t_{CSR}	10	—	ns
$\overline{CAS}$ hold time	t_{CHR}	10	—	ns
Normal mode $\overline{CAS}$ precharge time	t_{CPN}	10	—	ns
Fast page mode cycle time	t_{PC}	45	—	ns
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	ns
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	ns
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40	—	ns

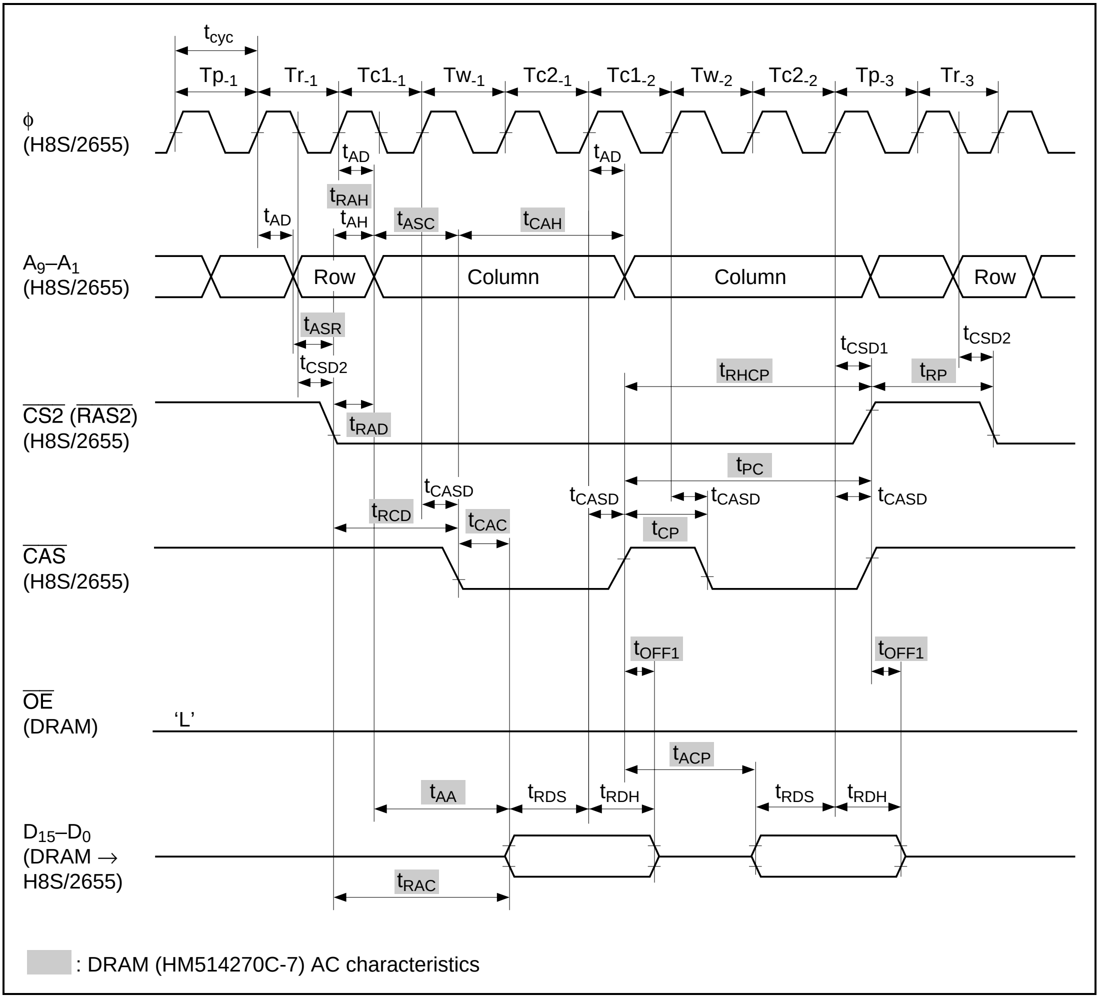


Figure 3.3.2 (c) DRAM Read Timing Chart

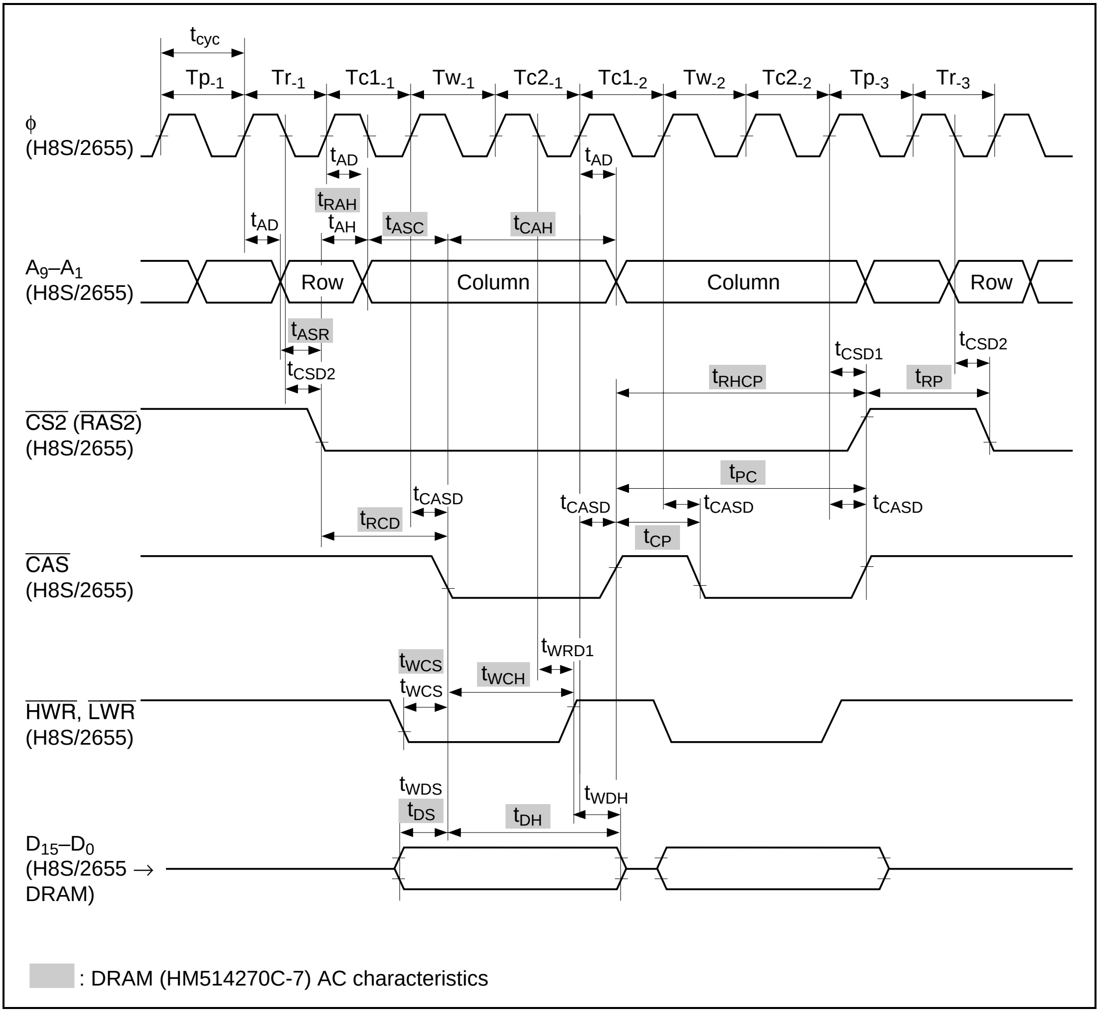


Figure 3.3.2 (d) DRAM Write Timing Chart

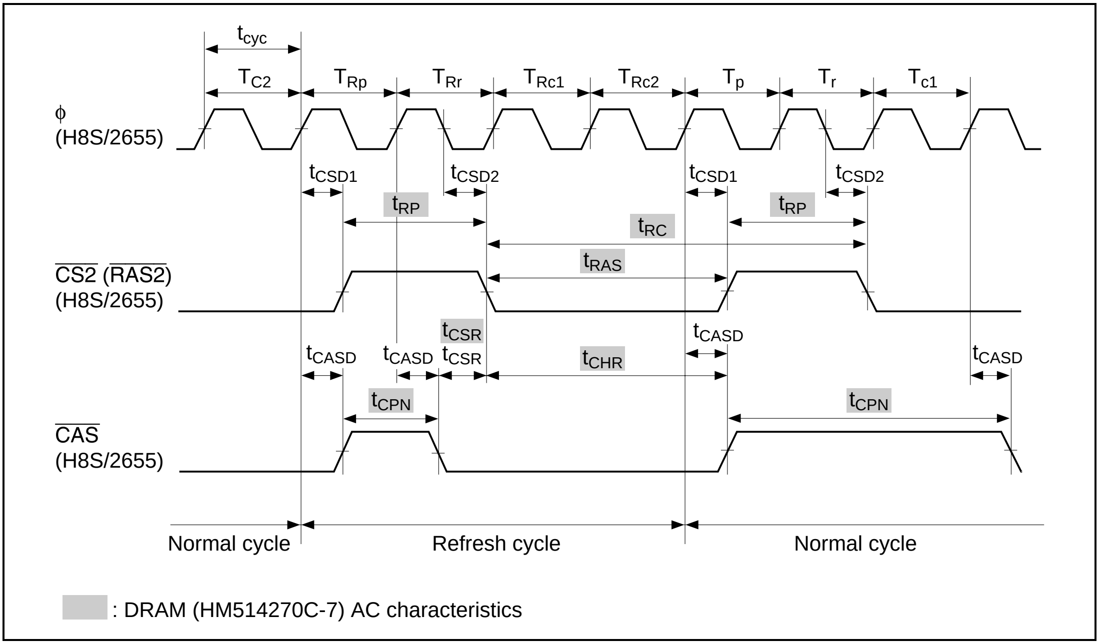


Figure 3.3.2 (e) $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Timing Chart

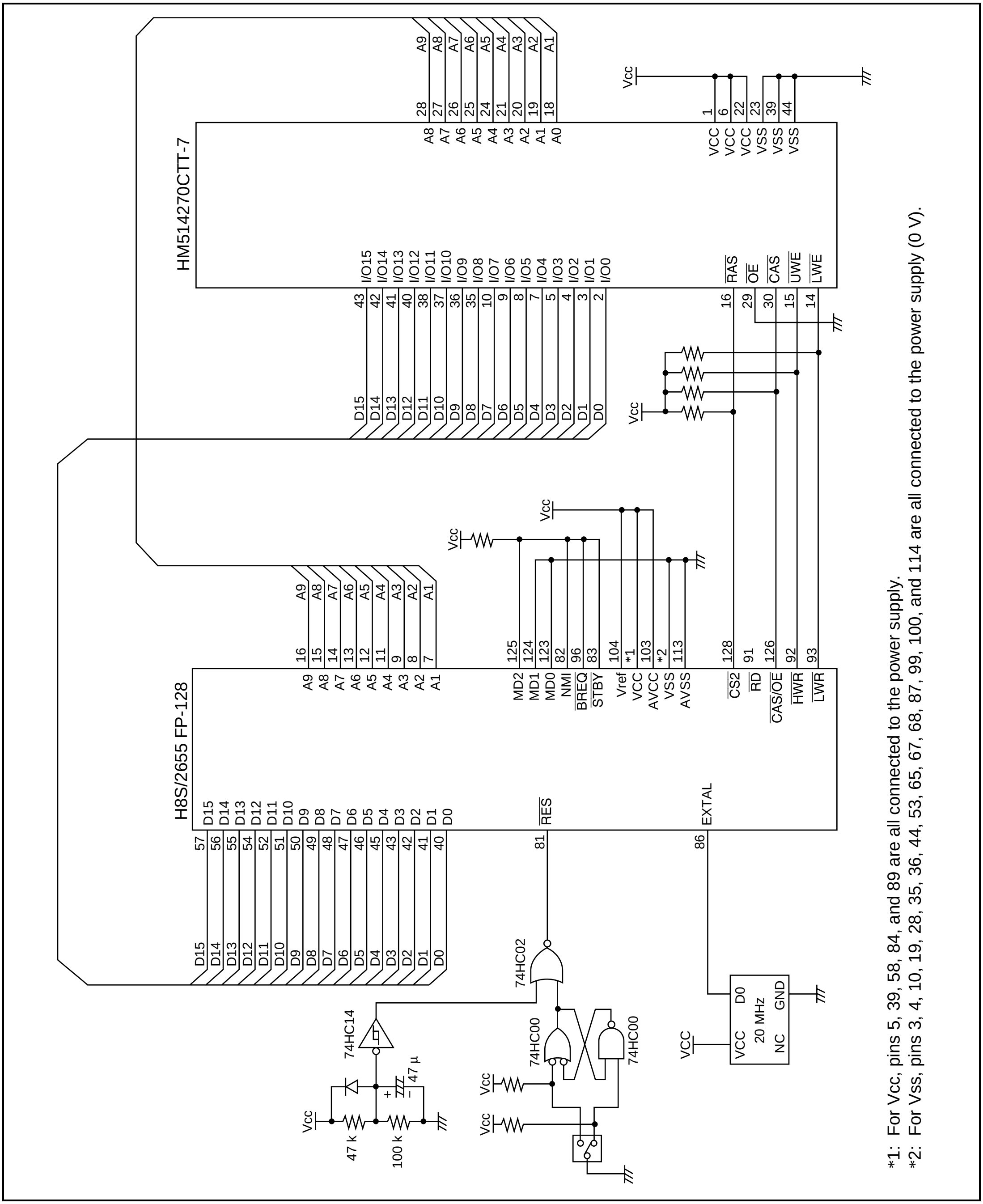


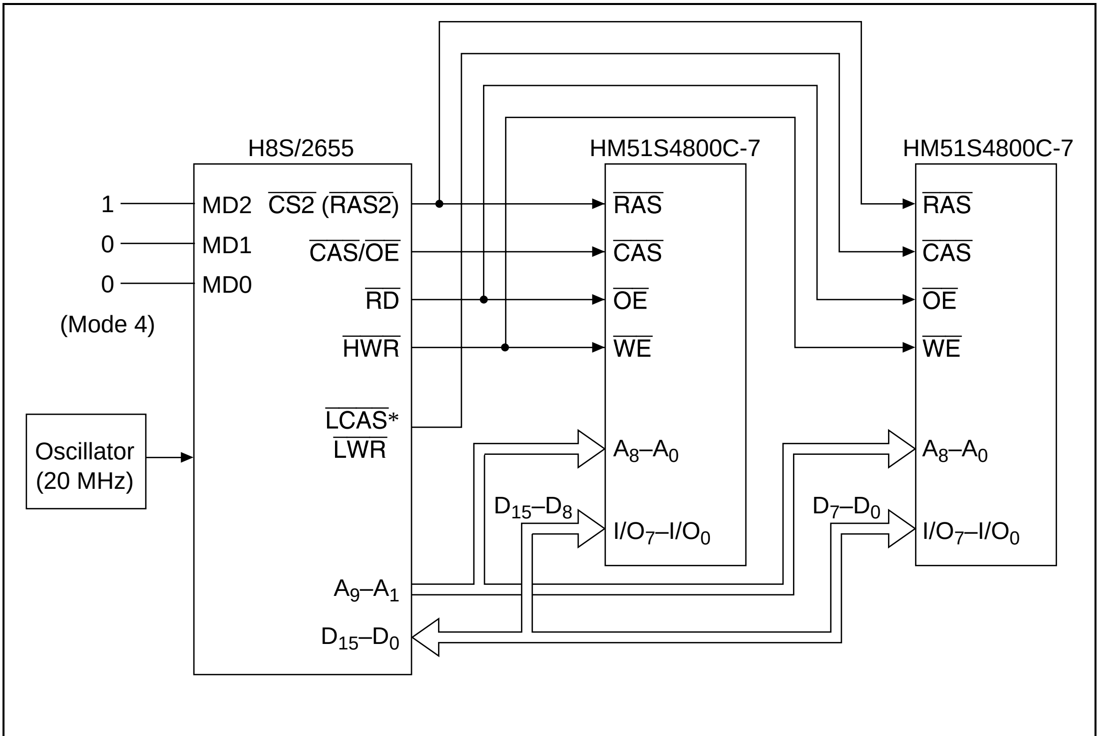
Figure 3.3.2 (f) HM514270CTT-7 Interface

3.9 DRAM (HM51S4800C-7) Interface Using 2-CAS Control

DRAM (HM51S4800C-7) Interface	MCU: H8S/2655	Functions Used: Mode 4 (16-Bit Bus Mode)

Specifications

1. Figure 3.3.3 (a) shows an example of the connection between an H8S/2655 and ×8-bit configuration DRAMs (HM51S4800C-7s). The H8S/2655 is set to mode 4 16-bit bus mode, and the DRAMs are allocated to area 2. The 2- $\overline{\text{CAS}}$ method is used for byte control.



*: Either the $\overline{\text{LCAS}}$ or $\overline{\text{LWR}}$ pin is selected by a register setting.

Figure 3.3.3 (a) Example of Connection between H8S/2655 and DRAMs (2-$\overline{\text{CAS}}$ Byte Control)

2. Figure 3.3.3 (b) shows the memory map. When the 16-Mbyte address space is divided into areas in 2-Mbyte units, the DRAM area is H'40 0000–H'4F FFFF.

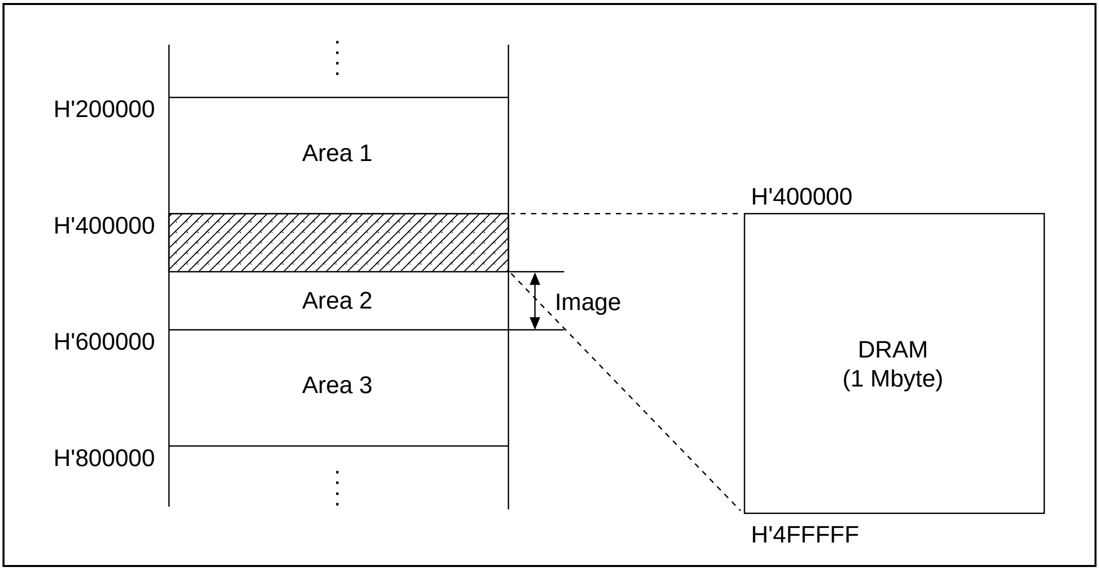


Figure 3.3.3 (b) Memory Map

3. Table 3.3.3 (a) shows the bus controller settings.

Table 3.3.3 (a) Bus Controller Settings

Name	Abbrev.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Setting
Bus width control register	ABWCR	ABW7 *	ABW6 *	ABW5 *	ABW4 *	ABW3 *	ABW2 0	ABW1 *	ABW0 *	Area 2: 16-bit access space
Access state control register	ASTCR	AST7 *	AST6 *	AST5 *	AST4 *	AST3 *	AST2 *	AST1 *	AST0 *	—
Wait control register H	WCRH	W71 *	W70 *	W61 *	W60 *	W51 *	W50 *	W41 *	W40 *	—
Wait control register L	WCRL	W31 *	W30 *	W21 0	W20 1	W11 *	W10 *	W01 *	W00 *	1 program wait state inserted
Bus control register H	BCRH	ICIS1 *	ICIS0 *	BRSTRM *	BRSTS1 *	BRSTS0 *	RMTS2 0	RMTS1 0	RMTS0 1	DRAM space: Area 2
Bus control register L	BCRL	BRLE *	BREQOE *	EAE *	LCASS 0: $\overline{LCAS}$ pin or 1: $\overline{LWR}$ pin	DDS *	ASS 1	WDBE *	WAITE *	$\overline{LCAS}$ signal selected from $\overline{LCAS}$ and $\overline{LWR}$ pins Area partition unit: 2 Mbytes (16 Mbytes)
Memory control register	MCR	TPC 0	BE 1	RCDM 0	CW2 0	MXC1 0	MXC0 1	RLW1 0	RLW0 0	1 precharge state Fast page mode $\overline{RAS}$ up mode 2-$\overline{CAS}$ control 9-bit shift $\overline{CAS}$-before-$\overline{RAS}$ refreshing, no wait
DRAM control register	DRAMCR	RFSHE 1	RCW 0	RMODE 0	CMF *	CMIE 0	CKS2 0	CKS1 0	CKS0 1	Refresh control performed $\overline{CAS}$-before-$\overline{RAS}$ refreshing wait state insertion disabled $\overline{CAS}$-before-$\overline{RAS}$ refreshing Compare-match interrupts disabled Refresh counter clock: $\phi/2$
Refresh time constant register	RTCOR	0	1	0	0	1	1	1	1	H'4F[*1]

*: Don't care

*1: The HM51S4800C-7 uses 1024-cycle/16 ms refreshing. To allow for cases where refreshing cannot be performed at the specified time, calculations are based on twice this figure: 2048 cycles/16 ms. With a refresh counter clock of $\phi/2$ (100 ns), the RTCOR value is (16 ms/2048 cycles) / 100 ns ≅ 79 (= H'4F).

Operation

The calculations used to check whether the AC characteristics are satisfied in DRAM access are shown below. The t_{cyc} value, unspecified min value, and unspecified max value are as follows.

- t_{cyc}: 50 ns (20 MHz oscillator (= ϕ))
- Unspecified min value: 0 ns
- Unspecified max value: min value

In the times obtained based on ϕ, the reference timing is shown in [ ].

For the timing values, see 5. AC Characteristics below.

1. Read Access

   Figure 3.3.3 (c) shows the DRAM read timing chart. Confirm that the following AC characteristics are satisfied.

Item		Symbol
DRAM (HM51S4800C-7)	Row address setup time	t_{ASR}
	Row address hold time	t_{RAH}
	Column address setup time	t_{ASC}
	Column address hold time	t_{CAH}
	$\overline{\text{RAS}}$-$\overline{\text{CAS}}$ delay time	t_{RCD}
	$\overline{\text{RAS}}$-column address delay time	t_{RAD}
	$\overline{\text{RAS}}$ precharge time	t_{RP}
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}

   a. DRAM

      i. Row address setup time calculation [T_{r-1} cycle rise]

      $0.5\ t_{cyc} + t_{CSD2\ (min)} – t_{AD\ (max)} = 5ns \geq 0\ ns\ (t_{ASR})$

      ii. Row address hold time calculation

      $t_{AH\ (min)} = 0.5\ t_{cyc} – 10 = 15\ ns \geq 10\ ns\ (t_{RAH})$

      iii. Column address setup time calculation [T_{c1-1} cycle rise]

      $t_{cyc} + t_{CASD\ (min)} – t_{AD\ (max)} = 30\ ns \geq 0\ ns\ (t_{ASC})$

      iv. Column address hold time calculation [T_{w-1} cycle rise]

      $2\ t_{cyc} + t_{AD\ (min)} – t_{CASD\ (max)} = 80\ ns \geq 15\ ns\ (t_{CAH})$

v. $\overline{RAS}$-$\overline{CAS}$ delay time calculation [T_{r-1} cycle fall]

$1.5\ t_{cyc} + t_{CASD\ (min)} - t_{CSD2\ (max)} = 55\ ns \geq 20\ ns\ (t_{RCD})$

vi. $\overline{RAS}$-column address delay time calculation

$t_{AH\ (min)} = 0.5\ t_{cyc} - 10 = 15\ ns \geq 15\ ns\ (t_{RAD})$

vii. $\overline{RAS}$ precharge time calculation [T_{p-3} cycle rise]

$1.5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD1\ (max)} = 55\ ns \geq 50\ ns\ (t_{RP})$

b. H8S/2655

i. Read data setup time calculation [T_{w-1} cycle rise]

$2\ t_{cyc} - t_{CASD\ (max)} + t_{CAC\ (max)} = 60\ ns \geq 15\ ns\ (t_{RDS})$

Note: Access times are specified as follows according to t_{RCD} and t_{RAD}.

Conditions	Applicable Time
t_{RCD} (calculated value) $\geq t_{RCD}$ (max) and t_{RAD} (calculated value) $\leq t_{RAD}$ (max)	Access time from $\overline{CAS}$ (t_{CAC})
t_{RCD} (calculated value) $\leq t_{RCD}$ (max) and t_{RAD} (calculated value) $\geq t_{RAD}$ (max)	Access time from address (t_{AA})
t_{RCD} (calculated value) $\leq t_{RCD}$ (max) and t_{RAD} (calculated value) $\leq t_{RAD}$ (max)	Access time from $\overline{RAS}$ (t_{RAC})

ii. Read data hold time calculation [T_{c1-2} cycle rise]

$t_{CASD\ (min)} + t_{OFF1\ (min)} = 0\ ns \geq 0\ ns\ (t_{RDH})$

2. Write Access

Figure 3.3.3 (d) shows the DRAM write timing chart. Confirm that the following AC characteristics are satisfied.

Item		Symbol
DRAM (HM51S4800C-7)	Write command setup time	t_{WCS}
	Write command hold time	t_{WCH}
	Write input setup time	t_{DS}
	Write input hold time	t_{DH}

a. Write command setup time calculation

$t_{WCS\ (min)} = 0.5\ t_{cyc} - 10 = 15\ ns \geq 0\ ns\ (t_{WCS})$

b. Write command hold time calculation [T_{w-1} cycle rise]

$1.5\ t_{cyc} - t_{CASD\ (max)} = 55\ ns \geq 15\ ns\ (t_{WCH})$

c. Write input setup time calculation

$t_{WDS\ (min)} = 0.5\ t_{cyc} - 20 = 5\ ns \geq 0\ ns\ (t_{DS})$

d. Write input hold time calculation [T_{w-1} cycle rise]

$1.5\ t_{cyc} + t_{WRD1\ (min)} + t_{WDH\ (min)} - t_{CASD\ (max)} = 55\ ns \geq 15\ ns\ (t_{DH})$

3. Burst Mode

a. Fast page mode

In fast page mode, confirm that the following AC characteristics are satisfied.

Item		Symbol
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}
DRAM (HM51S4800C-7)	Fast page mode $\overline{CAS}$ precharge time	t_{CP}
	Fast page mode cycle time	t_{PC}
	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}

i. H8S/2655

i-1 Read data setup time calculation [T_{c1-2} cycle rise]

$3\ t_{cyc} - t_{CASD\ (max)} - t_{ACP\ (max)} = 90\ ns \geq 15\ ns\ (t_{RDS})$

i-2 Read data hold time calculation [T_{p-3} cycle rise]

$t_{CSD1\ (min)} + t_{OFF1\ (min)} = 0\ ns \geq 0\ ns\ (t_{RDH})$

ii. DRAM

ii-1 Fast page mode$\overline{CAS}$ precharge time calculation [T_{c1-2} cycle rise]

$t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 30\ ns \geq 10\ ns\ (t_{CP})$

ii-2 Fast page mode cycle time calculation [T_{w-1} cycle rise]

$3\ t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 130\ ns \geq 45\ ns\ (t_{PC})$

ii-3 $\overline{RAS}$ hold time from $\overline{CAS}$ precharge calculation [T_{c1-2} cycle rise]

$3\ t_{cyc} + t_{CSD1\ (min)} - t_{CASD\ (max)} = 130\ ns \geq 40\ ns\ (t_{RHCP})$

b. $\overline{RAS}$ down mode

$\overline{RAS}$ down mode can be selected by setting the RCDM bit to 1 in the memory control register (MCR). This mode cannot be selected when the $\overline{LWR}$ pin is used for the $\overline{LCAS}$ signal.

4. Refresh Cycle

a. $\overline{CAS}$-before-$\overline{RAS}$ refreshing

Figures 3.3.3 (e) and 3.3.3 (f) show the $\overline{CAS}$-before-$\overline{RAS}$ refresh timing charts. Confirm that the following AC characteristics are satisfied.

Item		Symbol
DRAM (HM51S4800C-7)	$\overline{RAS}$ precharge time	t_{RP}
	$\overline{CAS}$ setup time	t_{CSR}
	$\overline{RAS}$ pulse width	t_{RAS}
	$\overline{CAS}$ hold time	t_{CHR}
	Normal mode $\overline{CAS}$ precharge time	t_{CPN}
	Random read/write cycle time	t_{RC}

i. $\overline{RAS}$ precharge time

i-1 Transition from normal cycle to refresh cycle [T_{Rp} cycle rise]

$1.5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD1\ (max)} = 55\ ns \geq 50\ ns\ (t_{RP})$

i-2 Transition from refresh cycle to normal cycle

- When using $\overline{LCAS}$ pin for $\overline{LCAS}$ signal [T_p cycle rise]

  $1.5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD1\ (max)} = 55\ ns \geq 50\ ns\ (t_{RP})$

- When using $\overline{LWR}$ pin for $\overline{LCAS}$ signal [T_{Rl} cycle rise]

  $2.5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD1\ (max)} = 105\ ns \geq 50\ ns\ (t_{RP})$

ii. $\overline{CAS}$ setup time

$t_{CSR\ (min)} = 15\ ns \geq 10\ ns\ (t_{CSR})$

iii. $\overline{RAS}$ pulse width [T_{Rr} cycle fall]

$2.5\ t_{cyc} + t_{CSD1\ (min)} - t_{CSD2\ (max)} = 105\ ns \geq 70\ ns\ (t_{RAS})$

iv. $\overline{CAS}$ hold time [T_{Rr} cycle fall]

$2.5\ t_{cyc} + t_{CASD\ (min)} - t_{CSD2\ (max)} = 105\ ns \geq 10\ ns\ (t_{CHR})$

v. Normal mode $\overline{CAS}$ precharge time

v-1 Transition from normal cycle to refresh cycle [T_{Rp} cycle rise]

$t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 70\ ns \geq 10\ ns\ (t_{CPN})$

v-2 Transition from refresh cycle to normal cycle

- When using $\overline{LCAS}$ pin for $\overline{LCAS}$ signal [T_p cycle rise]

  $3\ t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 130\ ns \geq 10\ ns\ (t_{CPN})$

- When using $\overline{LWR}$ pin for $\overline{LCAS}$ signal [T_{Rl} cycle rise]

  $4\ t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 180\ ns \geq 10\ ns\ (t_{CPN})$

vi. Random read/write cycle time [T_{Rr} cycle fall] vi-1 When using $\overline{LCAS}$ pin for $\overline{LCAS}$ signal

$4\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD2\ (max)} = 180\ ns \geq 130\ ns\ (t_{RC})$

vi-2 When using $\overline{LWR}$ pin for $\overline{LCAS}$ signal

$5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD2\ (max)} = 230\ ns \geq 130\ ns\ (t_{RC})$

b. Self-refresh mode

Figure 3.3.3 (g) shows the self-refresh timing chart.

A transition can be made to self-refresh mode by setting the RMODE bit to 1 in the DRAM control register (DRAMCR), then executing a SLEEP instruction to enter software standby mode.

In self-refresh mode, confirm that the following AC characteristics are satisfied.

Item		Symbol
DRAM (HM51S4800C-7)	$\overline{RAS}$ pulse width	t_{RASS}
	$\overline{CAS}$ hold time	t_{CHS}
	$\overline{RAS}$ precharge time	t_{RPS}

i. $\overline{RAS}$ pulse width calculation [T_{Rr} cycle fall]

$3.5\ t_{cyc}$ + (software standby time) + $t_{CSD1\ (max)} - t_{CSD2\ (min)}$

= 105 + (software standby time) ns ≥ 100 ns (t_{RASS})

ii. $\overline{CAS}$ hold time calculation [T_{Rc} cycle fall]

$0.5\ t_{cyc} + t_{CASD\ (min)} - t_{CSD1\ (max)} = 5\ ns \geq -50\ ns\ (t_{CHS})$

iii. $\overline{RAS}$ precharge time calculation [T_{Rc} cycle fall]

When the interrupt handling routine area is in DRAM:

t_{cyc} + (interrupt exception handling time) + $1.5\ t_{cyc} + t_{CSD2\ (max)} - t_{CSD1\ (min)}$
= 105 + (interrupt exception handling time) ns ≥ 130 ns (t_{RPS})

Note: Under the following conditions, the interrupt exception handling time is $21\ t_{cyc}$ = 1050 ns, so that the above $\overline{RAS}$ precharge time inequality is true.

- Interrupt mode: Mode 0
- Area 0 access states: 4
- Stack area access states: 3

5. AC Characteristics

Table 3.3.3 (b) shows the AC characteristics of the H8S/2655, and table 3.3.3. (c) the AC characteristics of the HM51S4800C-7.

Table 3.3.3 (b) AC Characteristics of H8S/2655

Item	Symbol	Min	Max	Unit
Address delay time	t_{AD}	—	20	ns
Address hold time	t_{AH}	$0.5 \times t_{cyc} – 10$	—	ns
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	ns
$\overline{CS}$ delay time 2	t_{CSD2}	—	20	ns
$\overline{RD}$ delay time 1	t_{RSD1}	—	20	ns
$\overline{CAS}$ delay time	t_{CASD}	—	20	ns
Read data setup time	t_{RDS}	15	—	ns
Read data hold time	t_{RDH}	0	—	ns
$\overline{WR}$ delay time 1	t_{WRD1}	—	20	ns
Write data setup time	t_{WDS}	$0.5 \times t_{cyc} – 20$	—	ns
Write data hold time	t_{WDH}	$0.5 \times t_{cyc} – 10$	—	ns
$\overline{WR}$ setup time	t_{WCS}	$0.5 \times t_{cyc} – 10$	—	ns

Table 3.3.3 (c) AC Characteristics of HM51S4800C-7

Item	Symbol	Min	Max	Unit
Random read/write cycle time	t_{RC}	130	—	ns
$\overline{\text{RAS}}$ precharge time	t_{RP}	50	—	ns
$\overline{\text{RAS}}$ pulse width	t_{RAS}	70	10000	ns
Row address setup time	t_{ASR}	0	—	ns
Row address hold time	t_{RAH}	10	—	ns
Column address setup time	t_{ASC}	0	—	ns
Column address hold time	t_{CAH}	15	—	ns
$\overline{\text{RAS}}$-$\overline{\text{CAS}}$ delay time	t_{RCD}	20	50	ns
$\overline{\text{RAS}}$-column address delay time	t_{RAD}	15	35	ns
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	70	ns
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	20	ns
Access time from address	t_{AA}	—	35	ns
Access time from $\overline{\text{OE}}$	t_{OAC}	—	20	ns
Output buffer turn-off time	t_{OFF1}	0	15	ns
Write command setup time	t_{WCS}	0	—	ns
Write command hold time	t_{WCH}	15	—	ns
Data input setup time	t_{DS}	0	—	ns
Data input hold time	t_{DH}	15	—	ns
$\overline{\text{CAS}}$ setup time	t_{CSR}	10	—	ns
$\overline{\text{CAS}}$ hold time	t_{CHR}	10	—	ns
Normal mode $\overline{\text{CAS}}$ precharge time	t_{CPN}	10	—	ns
Fast page mode cycle time	t_{PC}	45	—	ns
Fast page mode $\overline{\text{CAS}}$ precharge time	t_{CP}	10	—	ns
Access time from $\overline{\text{CAS}}$ precharge	t_{ACP}	—	40	ns
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t_{RHCP}	40	—	ns
Self-refresh $\overline{\text{RAS}}$ pulse width	t_{RASS}	100	—	ns
Self-refresh $\overline{\text{RAS}}$ precharge time	t_{RPS}	130	—	ns
Self-refresh $\overline{\text{CAS}}$ hold time	t_{CHS}	–50	—	ns

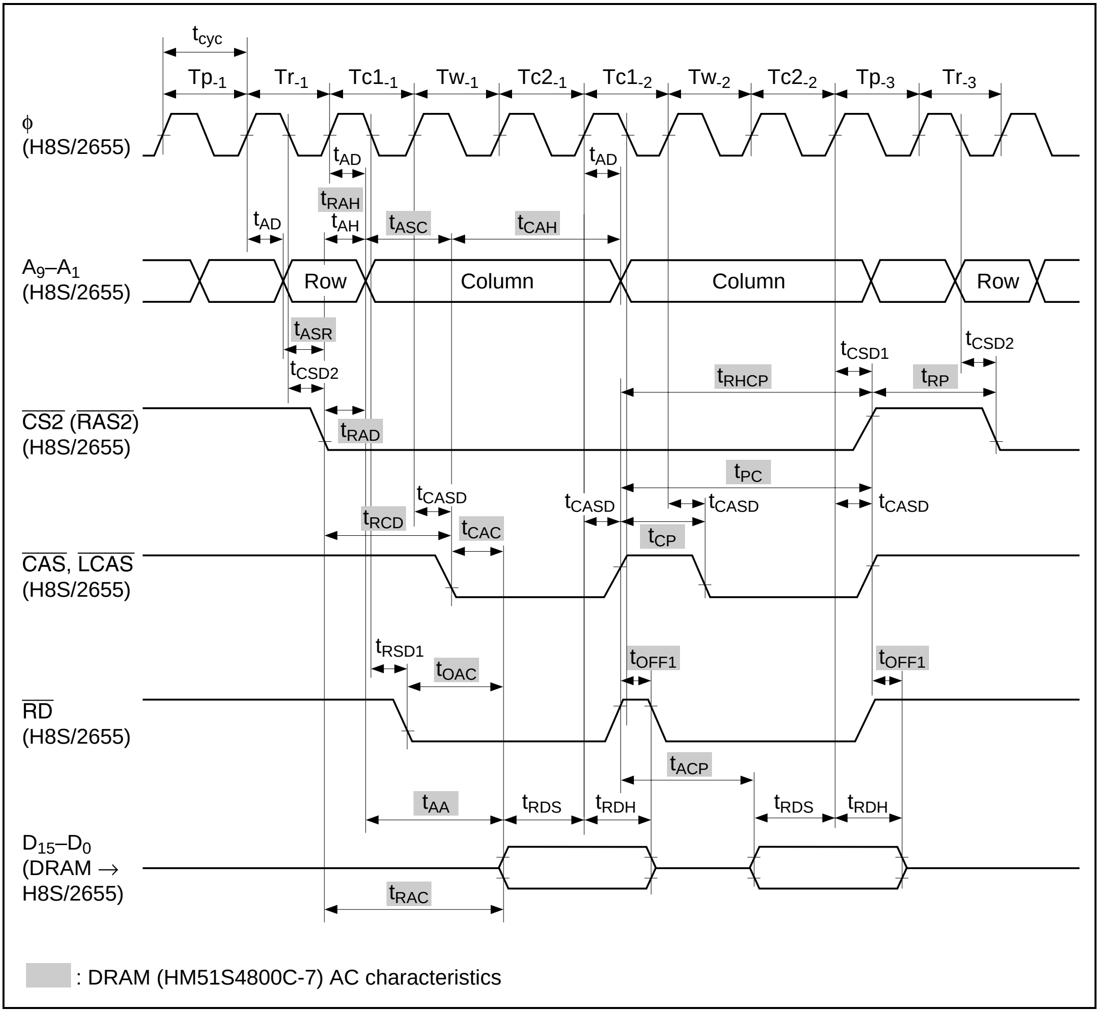


Figure 3.3.3 (c) DRAM Read Timing Chart

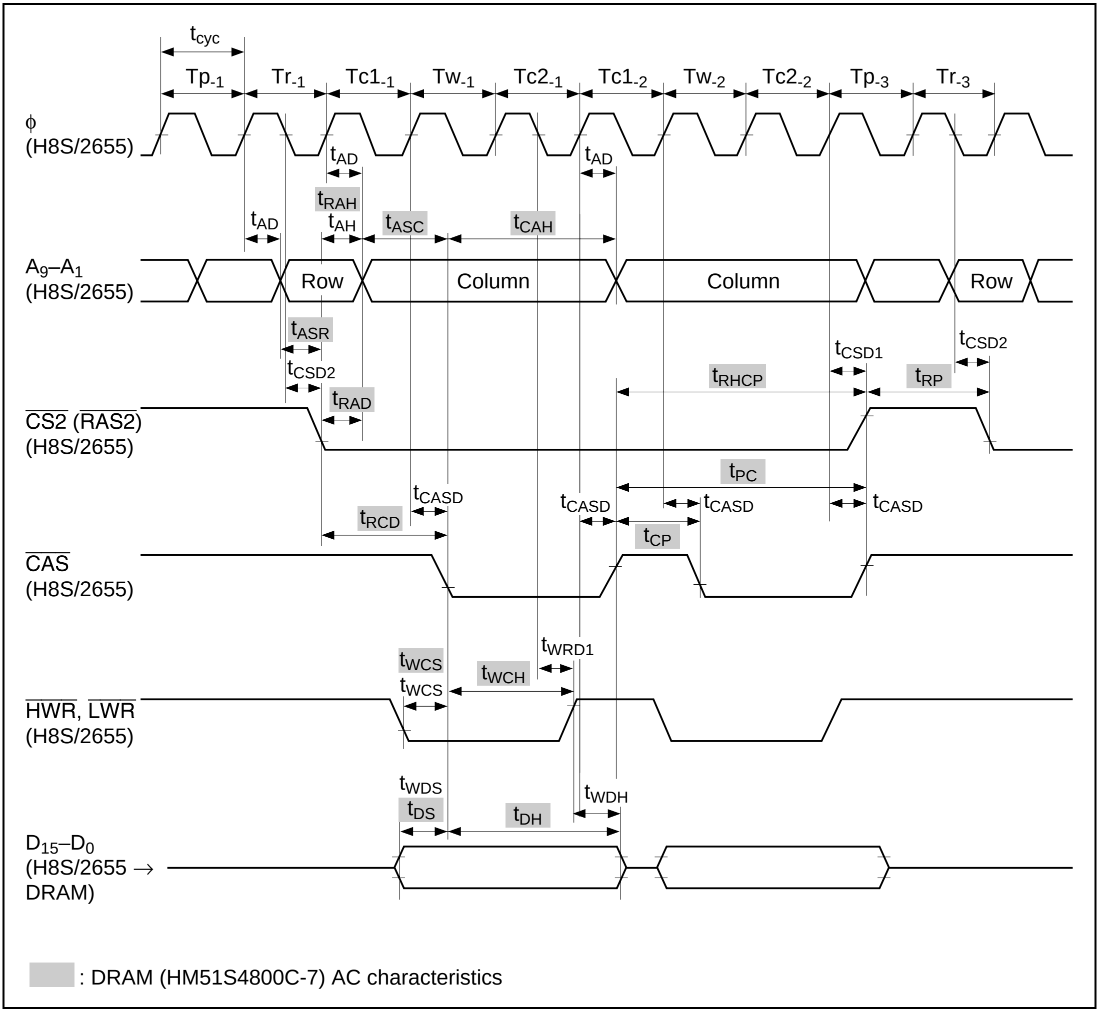


Figure 3.3.3 (d) DRAM Write Timing Chart

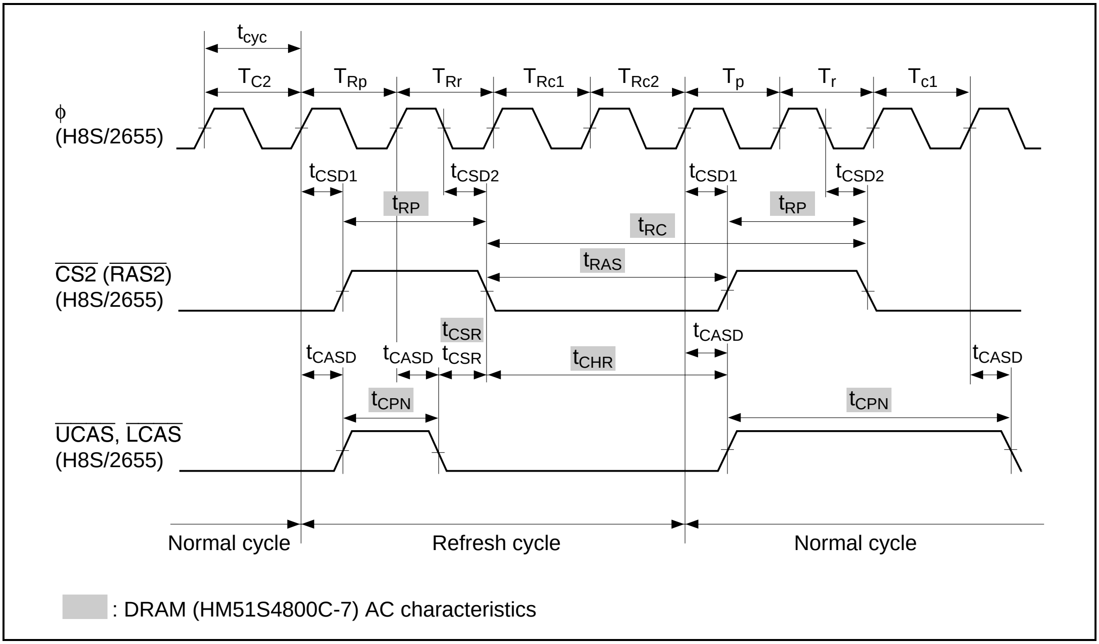


Figure 3.3.3 (e) $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Timing Chart ($\overline{\text{LCAS}}$ Pin Used for $\overline{\text{LCAS}}$ Signal)

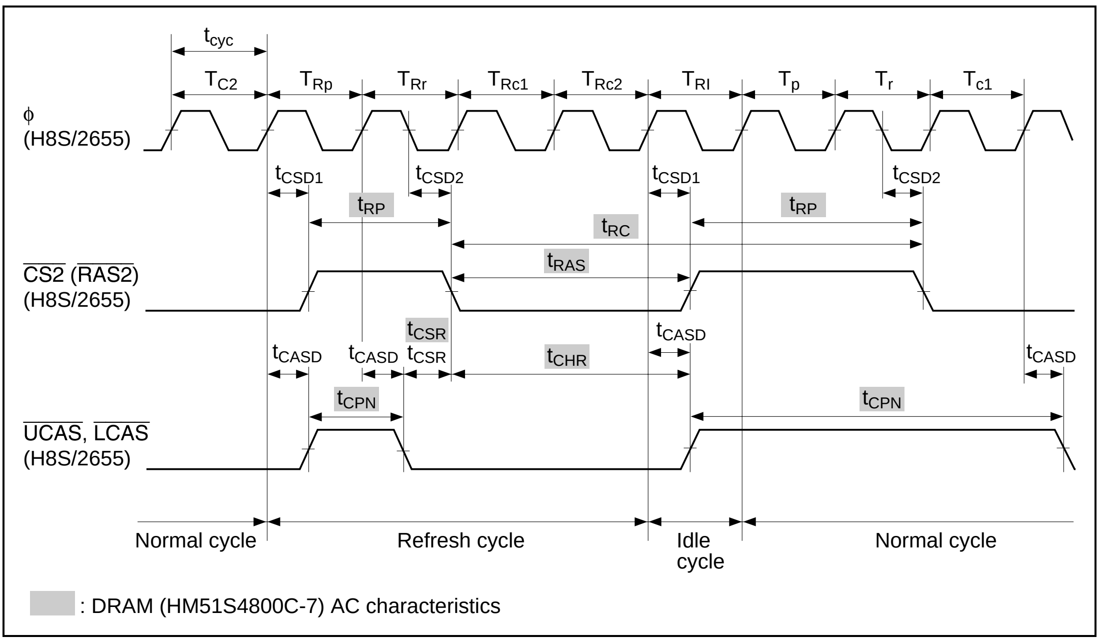


Figure 3.3.3 (f) $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Timing Chart ($\overline{\text{LWR}}$ Pin Used for $\overline{\text{LCAS}}$ Signal)

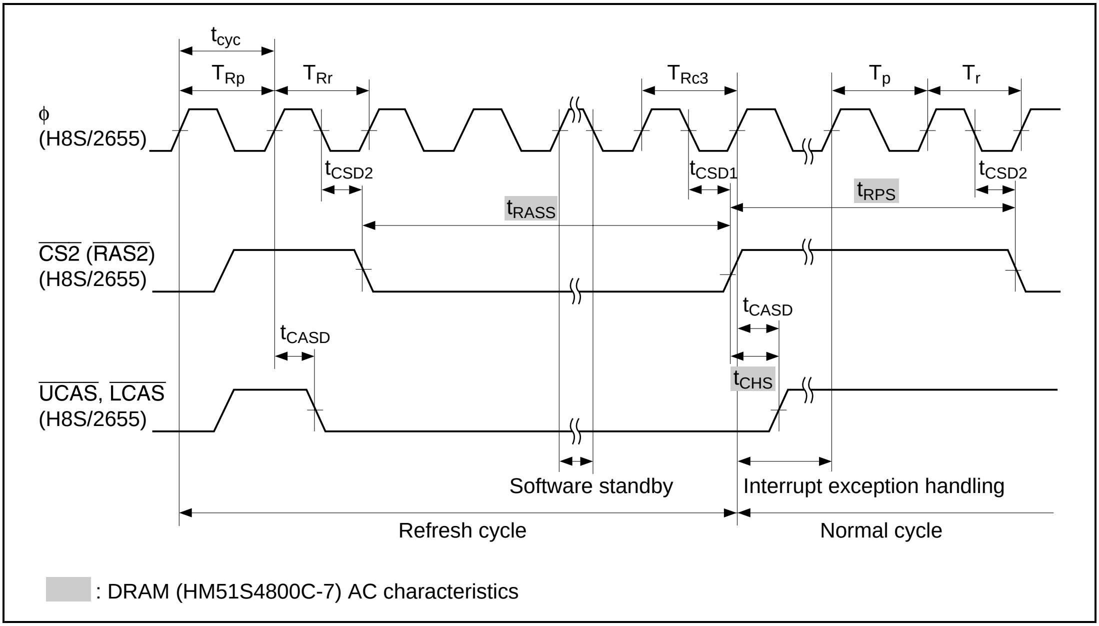


Figure 3.3.3 (g) Self-Refresh Timing Chart

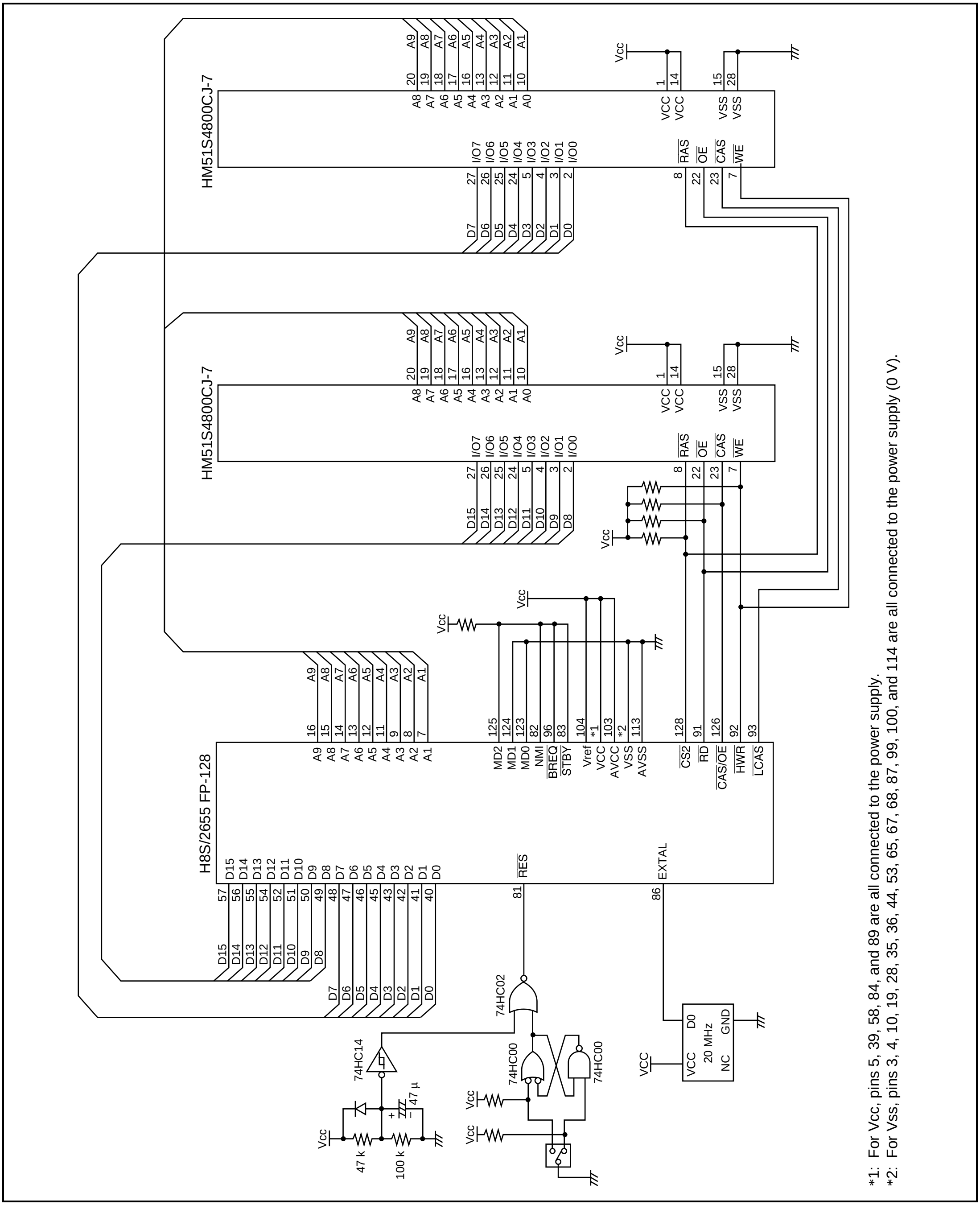


Figure 3.3.3 (h) HM51S4800CJ-7 Interface ($\overline{\text{LCAS}}$ Pin Used for $\overline{\text{LCAS}}$ Signal)

3.10 DRAM (HM51S4800C-7) Interface Using 2-WE Control

DRAM (HM51S4800C-7) Interface	MCU: H8S/2655	Functions Used: Mode 4 (16-Bit Bus Mode)

Specifications

1. Figure 3.3.4 (a) shows an example of the connection between an H8S/2655 and ×8-bit configuration DRAMs (HM51S4800C-7s). The H8S/2655 is set to mode 4 16-bit bus mode, and the DRAMs are allocated to area 2. The 2- $\overline{WE}$ method is used for byte control.

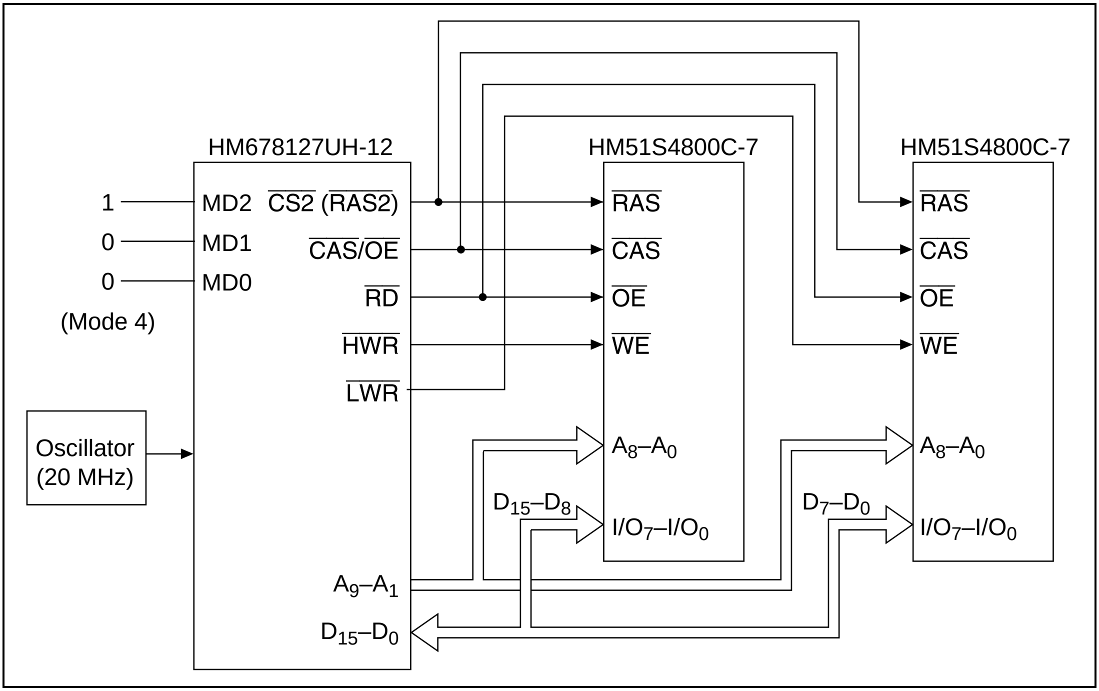


Figure 3.3.4 (a) Example of Connection between H8S/2655 and DRAMs (2-$\overline{WE}$ Byte Control)

2. Figure 3.3.4 (b) shows the memory map. When the 16-Mbyte address space is divided into areas in 2-Mbyte units, the DRAM area is H'40 0000–H'4F FFFF.

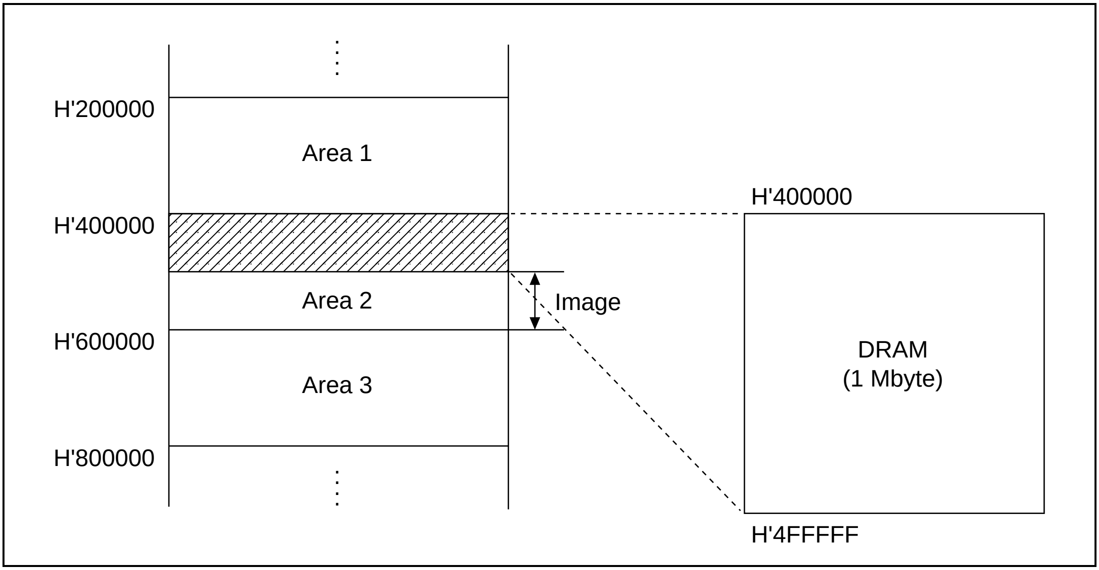


Figure 3.3.4 (b) Memory Map

3. Table 3.3.4 (a) shows the bus controller settings.

Table 3.3.4 (a) Bus Controller Settings

Name	Abbrev.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Setting
Bus width control register	ABWCR	ABW7 *	ABW6 *	ABW5 *	ABW4 *	ABW3 *	ABW2 0	ABW1 *	ABW0 *	Area 2: 16-bit access space
Access state control register	ASTCR	AST7 *	AST6 *	AST5 *	AST4 *	AST3 *	AST2 *	AST1 *	AST0 *	—
Wait control register H	WCRH	W71 *	W70 *	W61 *	W60 *	W51 *	W50 *	W41 *	W40 *	—
Wait control register L	WCRL	W31 *	W30 *	W21 0	W20 1	W11 *	W10 *	W01 *	W00 *	1 program wait state inserted
Bus control register H	BCRH	ICIS1 *	ICIS0 *	BRSTRM *	BRSTS1 *	BRSTS0 *	RMTS2 0	RMTS1 0	RMTS0 1	DRAM space: Area 2
Bus control register L	BCRL	BRLE *	BREQOE *	EAE *	LCASS *	DDS *	ASS 1	WDBE *	WAITE *	Area partition unit: 2 Mbytes (16 Mbytes)
Memory control register	MCR	TPC 0	BE 1	RCDM 0	CW2 1	MXC1 0	MXC0 1	RLW1 0	RLW0 0	1 precharge state Fast page mode $\overline{RAS}$ up mode 2-$\overline{WE}$ control 9-bit shift $\overline{CAS}$-before-$\overline{RAS}$ refreshing, no wait
DRAM control register	DRAMCR	RFSHE 1	RCW 0	RMODE 0	CMF *	CMIE 0	CKS2 0	CKS1 0	CKS0 1	Refresh control performed $\overline{CAS}$-before-$\overline{RAS}$ refreshing wait state insertion disabled $\overline{CAS}$-before-$\overline{RAS}$ refreshing Compare-match interrupts disabled Refresh counter clock: ϕ/2
Refresh time constant register	RTCOR	0	1	0	0	1	1	1	1	H'4F[*1]

*: Don't care

*1: The HM51S4800C-7 uses 1024-cycle/16 ms refreshing. To allow for cases where refreshing cannot be performed at the specified time, calculations are based on twice this figure: 2048 cycles/16 ms. With a refresh counter clock of ϕ/2 (100 ns), the RTCOR value is (16 ms/2048 cycles) / 100 ns $\cong$ 79 (= H'4F).

Operation

The calculations used to check whether the AC characteristics are satisfied in DRAM access are shown below. The t_{cyc} value, unspecified min value, and unspecified max value are as follows.

- t_{cyc}: 50 ns (20 MHz oscillator (= ϕ))
- Unspecified min value: 0 ns
- Unspecified max value: min value

In the times obtained based on ϕ, the reference timing is shown in [ ].

For the timing values, see 5. AC Characteristics below.

1. Read Access

   Figure 3.3.4 (c) shows the DRAM read timing chart. Confirm that the following AC characteristics are satisfied.

Item		Symbol
DRAM (HM51S4800C-7)	Row address setup time	t_{ASR}
	Row address hold time	t_{RAH}
	Column address setup time	t_{ASC}
	Column address hold time	t_{CAH}
	$\overline{\text{RAS}}$-$\overline{\text{CAS}}$ delay time	t_{RCD}
	$\overline{\text{RAS}}$-column address delay time	t_{RAD}
	$\overline{\text{RAS}}$ precharge time	t_{RP}
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}

   a. DRAM

      i. Row address setup time calculation [T_{r-1} cycle rise]

         $0.5\ t_{cyc} + t_{CSD2\ (min)} - t_{AD\ (max)} = 5\text{ns} \geq 0\text{ ns}\ (t_{ASR})$

      ii. Row address hold time calculation

         $t_{AH\ (min)} = 0.5\ t_{cyc} - 10 = 15\text{ ns} \geq 10\text{ ns}\ (t_{RAH})$

      iii. Column address setup time calculation [T_{c1-1} cycle rise]

         $t_{cyc} + t_{CASD\ (min)} - t_{AD\ (max)} = 30\text{ ns} \geq 0\text{ ns}\ (t_{ASC})$

      iv. Column address hold time calculation [T_{w-1} cycle rise]

         $2\ t_{cyc} + t_{AD\ (min)} - t_{CASD\ (max)} = 80\text{ ns} \geq 15\text{ ns}\ (t_{CAH})$

v. $\overline{\text{RAS}}$-$\overline{\text{CAS}}$ delay time calculation [T_{r-1} cycle fall]

$1.5\ t_{cyc} + t_{CASD\ (min)} - t_{CSD2\ (max)} = 55\ ns \geq 20\ ns\ (t_{RCD})$

vi. $\overline{\text{RAS}}$-column address delay time calculation

$t_{AH\ (min)} = 0.5\ t_{cyc} - 10 = 15\ ns \geq 15\ ns\ (t_{RAD})$

vii. $\overline{\text{RAS}}$ precharge time calculation [T_{p-3} cycle rise]

$1.5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD1\ (max)} = 55\ ns \geq 50\ ns\ (t_{RP})$

b. H8S/2655

i. Read data setup time calculation [T_{w-1} cycle rise]

$2\ t_{cyc} - t_{CASD\ (max)} + t_{CAC\ (max)} = 60\ ns \geq 15\ ns\ (t_{RDS})$

Note: Access times are specified as follows according to t_{RCD} and t_{RAD}.

Conditions	Applicable Time
t_{RCD} (calculated value) ≥ t_{RCD} (max) and t_{RAD} (calculated value) ≤ t_{RAD} (max)	Access time from $\overline{\text{CAS}}$ (t_{CAC})
t_{RCD} (calculated value) ≤ t_{RCD} (max) and t_{RAD} (calculated value) ≥ t_{RAD} (max)	Access time from address (t_{AA})
t_{RCD} (calculated value) ≤ t_{RCD} (max) and t_{RAD} (calculated value) ≤ t_{RAD} (max)	Access time from $\overline{\text{RAS}}$ (t_{RAC})

ii. Read data hold time calculation [T_{c1-2} cycle rise]

$t_{CASD\ (min)} + t_{OFF1\ (min)} = 0\ ns \geq 0\ ns\ (t_{RDH})$

2. Write Access

Figure 3.3.4 (d) shows the DRAM write timing chart. Confirm that the following AC characteristics are satisfied.

Item		Symbol
DRAM (HM51S4800C-7)	Write command setup time	t_{WCS}
	Write command hold time	t_{WCH}
	Write input setup time	t_{DS}
	Write input hold time	t_{DH}

a. Write command setup time calculation

$t_{WCS\ (min)} = 0.5\ t_{cyc} - 10 = 15\ ns \geq 0\ ns\ (t_{WCS})$

b. Write command hold time calculation [T_{w-1} cycle rise]

$1.5\ t_{cyc} - t_{CASD\ (max)} = 55\ ns \geq 15\ ns\ (t_{WCH})$

c. Write input setup time calculation

$t_{WDS\ (min)} = 0.5\ t_{cyc} - 20 = 5\ ns \geq 0\ ns\ (t_{DS})$

d. Write input hold time calculation [T_{w-1} cycle rise]

$1.5\ t_{cyc} + t_{WRD1\ (min)} + t_{WDH\ (min)} - t_{CASD\ (max)} = 55\ ns \geq 15\ ns\ (t_{DH})$

3. Burst Mode

a. Fast page mode

In fast page mode, confirm that the following AC characteristics are satisfied.

Item		Symbol
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}
DRAM (HM51S4800C-7)	Fast page mode $\overline{CAS}$ precharge time	t_{CP}
	Fast page mode cycle time	t_{PC}
	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}

i. H8S/2655

i-1 Read data setup time calculation [T_{c1-2} cycle rise]

$3\ t_{cyc} - t_{CASD\ (max)} - t_{ACP\ (max)} = 90\ ns \geq 15\ ns\ (t_{RDS})$

i-2 Read data hold time calculation [T_{p-3} cycle rise]

$t_{CSD1\ (min)} + t_{OFF1\ (min)} = 0\ ns \geq 0\ ns\ (t_{RDH})$

ii. DRAM

ii-1 Fast page mode $\overline{CAS}$ precharge time calculation [T_{c1-2} cycle rise]

$t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 30\ ns \geq 10\ ns\ (t_{CP})$

ii-2 Fast page mode cycle time calculation [T_{w-1} cycle rise]

$3\ t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 130\ ns \geq 45\ ns\ (t_{PC})$

ii-3 $\overline{RAS}$ hold time from $\overline{CAS}$ precharge calculation [T_{c1-2} cycle rise]

$3\ t_{cyc} + t_{CSD1\ (min)} - t_{CASD\ (max)} = 130\ ns \geq 40\ ns\ (t_{RHCP})$

b. $\overline{RAS}$ down mode

$\overline{RAS}$ down mode can be selected by setting the RCDM bit to 1 in the memory control register (MCR).

4. Refresh Cycle

a. $\overline{CAS}$-before-$\overline{RAS}$ refreshing

Figure 3.3.4 (e) shows the $\overline{CAS}$-before-$\overline{RAS}$ refresh timing chart. Confirm that the following AC characteristics are satisfied.

Item		**Symbol**
DRAM (HM51S4800C-7)	$\overline{RAS}$ precharge time	t_{RP}
	$\overline{CAS}$ setup time	t_{CSR}
	$\overline{RAS}$ pulse width	t_{RAS}
	$\overline{CAS}$ hold time	t_{CHR}
	Normal mode $\overline{CAS}$ precharge time	t_{CPN}
	Random read/write cycle time	t_{RC}

i. $\overline{RAS}$ precharge time

i-1 Transition from normal cycle to refresh cycle [T_{Rp} cycle rise]

$1.5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD1\ (max)} = 55\ ns \geq 50\ ns\ (t_{RP})$

i-2 Transition from refresh cycle to normal cycle [T_p cycle rise]

$1.5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD1\ (max)} = 55\ ns \geq 50\ ns\ (t_{RP})$

ii. $\overline{CAS}$ setup time

$t_{CSR\ (min)} = 15\ ns \geq 10\ ns\ (t_{CSR})$

iii. $\overline{RAS}$ pulse width [T_{Rr} cycle fall]

$2.5\ t_{cyc} + t_{CSD1\ (min)} - t_{CSD2\ (max)} = 105\ ns \geq 70\ ns\ (t_{RAS})$

iv. $\overline{CAS}$ hold time [T_{Rr} cycle fall]

$2.5\ t_{cyc} + t_{CASD\ (min)} - t_{CSD2\ (max)} = 105\ ns \geq 10\ ns\ (t_{CHR})$

v. Normal mode $\overline{CAS}$ precharge time

v-1 Transition from normal cycle to refresh cycle [T_{Rp} cycle rise]

$t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 70\ ns \geq 10\ ns\ (t_{CPN})$

v-2 Transition from refresh cycle to normal cycle [T_p cycle rise]

$3\ t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 130\ ns \geq 10\ ns\ (t_{CPN})$

vi. Random read/write cycle time [T_{Rr} cycle fall]

$4\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD2\ (max)} = 180\ ns \geq 130\ ns\ (t_{RC})$

b. Self-refresh mode

Figure 3.3.4 (f) shows the self-refresh timing chart.

A transition can be made to self-refresh mode by setting the RMODE bit to 1 in the DRAM control register (DRAMCR), then executing a SLEEP instruction to enter software standby mode.

In self-refresh mode, confirm that the following AC characteristics are satisfied.

Item		Symbol
DRAM (HM51S4800C-7)	$\overline{\text{RAS}}$ pulse width	t_{RASS}
	$\overline{\text{CAS}}$ hold time	t_{CHS}
	$\overline{\text{RAS}}$ precharge time	t_{RPS}

i. $\overline{\text{RAS}}$ pulse width calculation [T_{Rr} cycle fall]

$3.5\ t_{cyc}$ + (software standby time) + $t_{CSD1\ (max)} - t_{CSD2\ (min)}$

= 105 + (software standby time) ns ≥ 100 ns (t_{RASS})

ii. $\overline{\text{CAS}}$ hold time calculation [T_{Rc} cycle fall]

$0.5\ t_{cyc} + t_{CASD\ (min)} - t_{CSD1\ (max)} = 5\text{ ns} \geq -50\text{ ns}$ (t_{CHS})

iii. $\overline{\text{RAS}}$ precharge time calculation [T_{Rc} cycle fall]

When the interrupt handling routine area is in DRAM:

t_{cyc} + (interrupt exception handling time) + $1.5\ t_{cyc} + t_{CSD2\ (max)} - t_{CSD1\ (min)}$
= 105 + (interrupt exception handling time) ns ≥ 130 ns (t_{RPS})

Note: Under the following conditions, the interrupt exception handling time is 21 t_{cyc} = 1050 ns, so that the above $\overline{\text{RAS}}$ precharge time inequality is true.

- Interrupt mode: Mode 0
- Area 0 access states: 4
- Stack area access states: 3

5. AC Characteristics

Table 3.3.4 (b) shows the AC characteristics of the H8S/2655, and table 3.3.4. (c) the AC characteristics of the HM51S4800C-7.

Table 3.3.4 (b) AC Characteristics of H8S/2655

Item	Symbol	Min	Max	Unit
Address delay time	t_{AD}	—	20	ns
Address hold time	t_{AH}	$0.5 \times t_{cyc} - 10$	—	ns
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	ns
$\overline{CS}$ delay time 2	t_{CSD2}	—	20	ns
$\overline{RD}$ delay time 1	t_{RSD1}	—	20	ns
$\overline{CAS}$ delay time	t_{CASD}	—	20	ns
Read data setup time	t_{RDS}	15	—	ns
Read data hold time	t_{RDH}	0	—	ns
$\overline{WR}$ delay time 1	t_{WRD1}	—	20	ns
Write data setup time	t_{WDS}	$0.5 \times t_{cyc} - 20$	—	ns
Write data hold time	t_{WDH}	$0.5 \times t_{cyc} - 10$	—	ns
$\overline{WR}$ setup time	t_{WCS}	$0.5 \times t_{cyc} - 10$	—	ns

Table 3.3.4 (c) AC Characteristics of HM51S4800C-7

Item	Symbol	Min	Max	Unit
Random read/write cycle time	t_{RC}	130	—	ns
$\overline{\text{RAS}}$ precharge time	t_{RP}	50	—	ns
$\overline{\text{RAS}}$ pulse width	t_{RAS}	70	10000	ns
Row address setup time	t_{ASR}	0	—	ns
Row address hold time	t_{RAH}	10	—	ns
Column address setup time	t_{ASC}	0	—	ns
Column address hold time	t_{CAH}	15	—	ns
$\overline{\text{RAS}}$-$\overline{\text{CAS}}$ delay time	t_{RCD}	20	50	ns
$\overline{\text{RAS}}$-column address delay time	t_{RAD}	15	35	ns
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	70	ns
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	20	ns
Access time from address	t_{AA}	—	35	ns
Access time from $\overline{\text{OE}}$	t_{OAC}	—	20	ns
Output buffer turn-off time	t_{OFF1}	0	15	ns
Write command setup time	t_{WCS}	0	—	ns
Write command hold time	t_{WCH}	15	—	ns
Data input setup time	t_{DS}	0	—	ns
Data input hold time	t_{DH}	15	—	ns
$\overline{\text{CAS}}$ setup time	t_{CSR}	10	—	ns
$\overline{\text{CAS}}$ hold time	t_{CHR}	10	—	ns
Normal mode $\overline{\text{CAS}}$ precharge time	t_{CPN}	10	—	ns
Fast page mode cycle time	t_{PC}	45	—	ns
Fast page mode $\overline{\text{CAS}}$ precharge time	t_{CP}	10	—	ns
Access time from $\overline{\text{CAS}}$ precharge	t_{ACP}	—	40	ns
$\overline{\text{RAS}}$ hold time from $\overline{\text{CAS}}$ precharge	t_{RHCP}	40	—	ns
Self-refresh $\overline{\text{RAS}}$ pulse width	t_{RASS}	100	—	ns
Self-refresh $\overline{\text{RAS}}$ precharge time	t_{RPS}	130	—	ns
Self-refresh $\overline{\text{CAS}}$ hold time	t_{CHS}	–50	—	ns

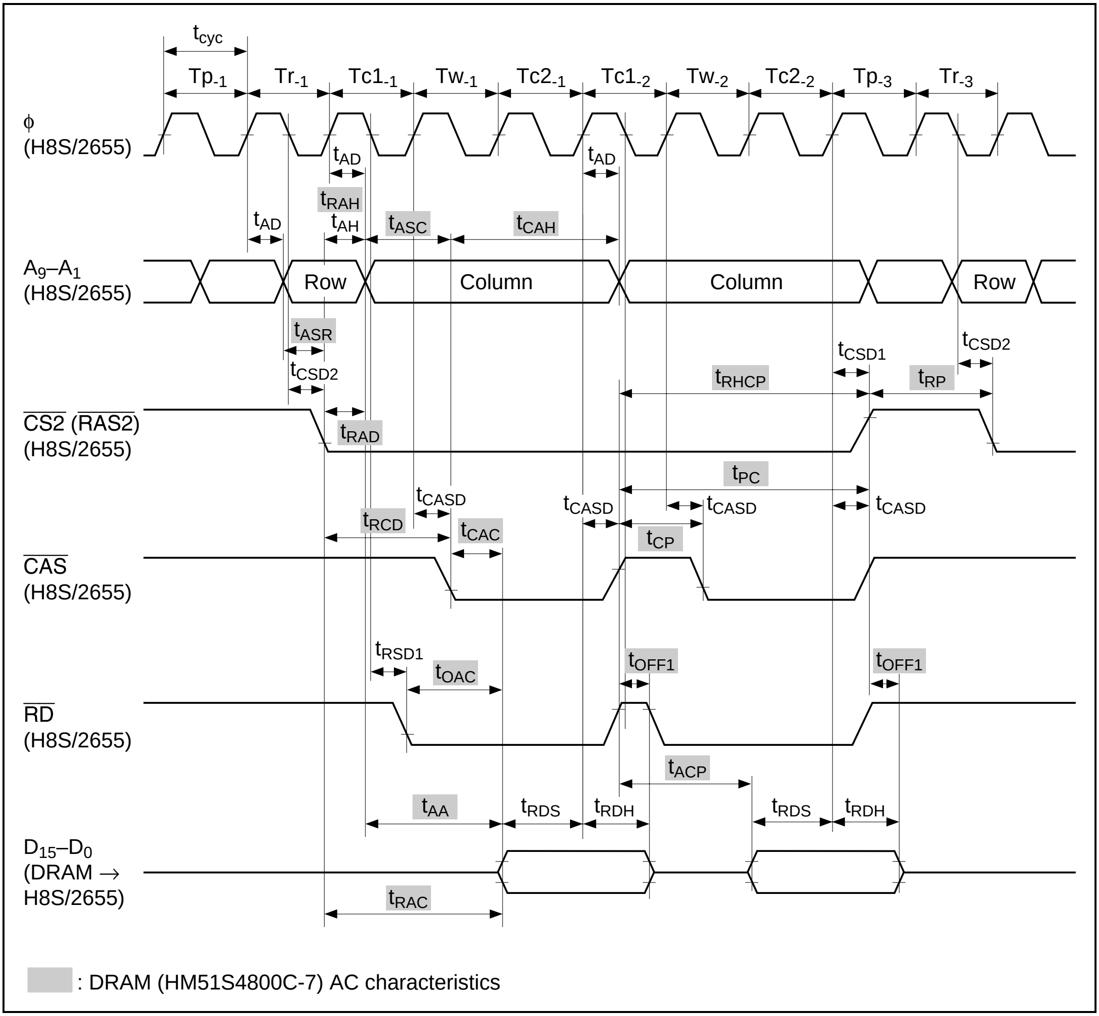


Figure 3.3.4 (c) DRAM Read Timing Chart

RENESAS

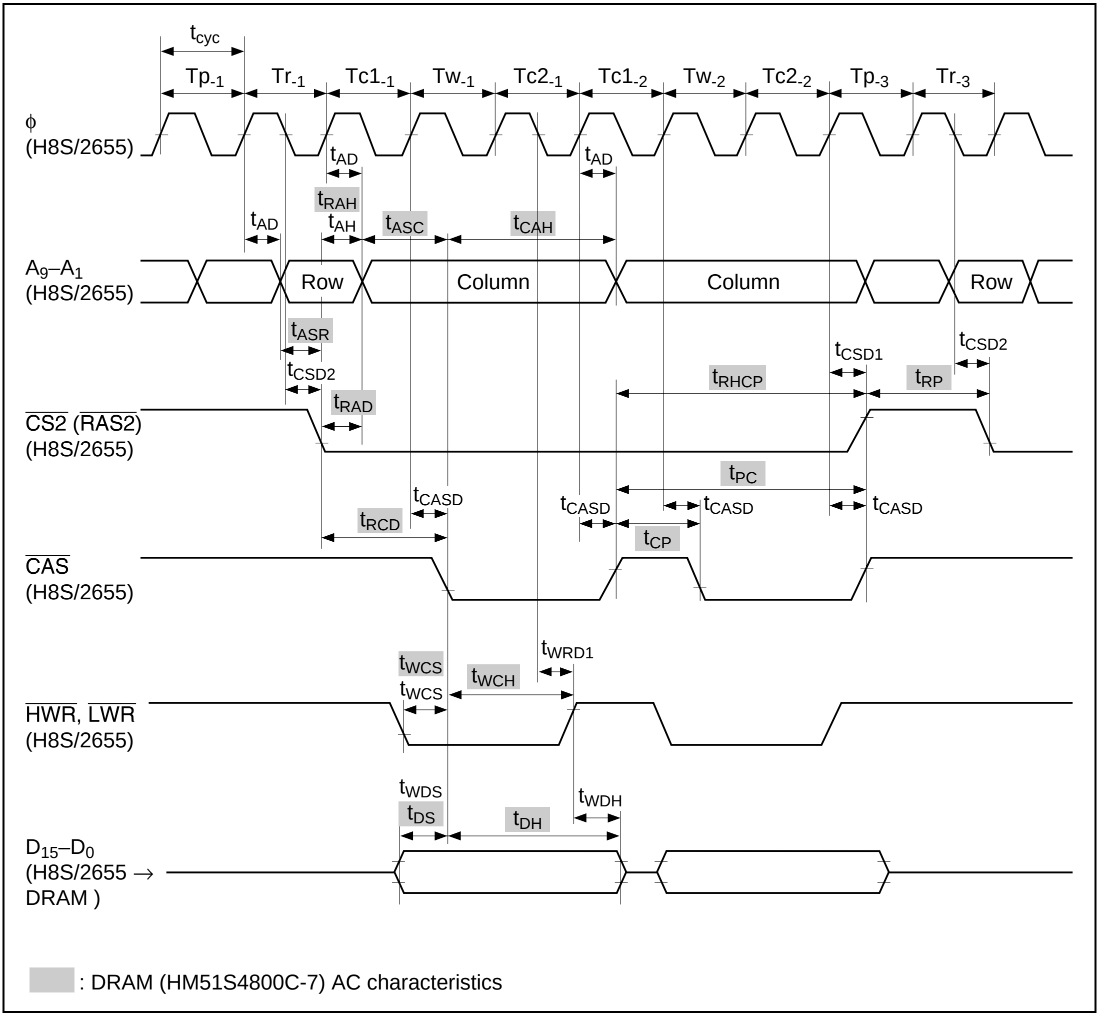


Figure 3.3.4 (d) DRAM Write Timing Chart

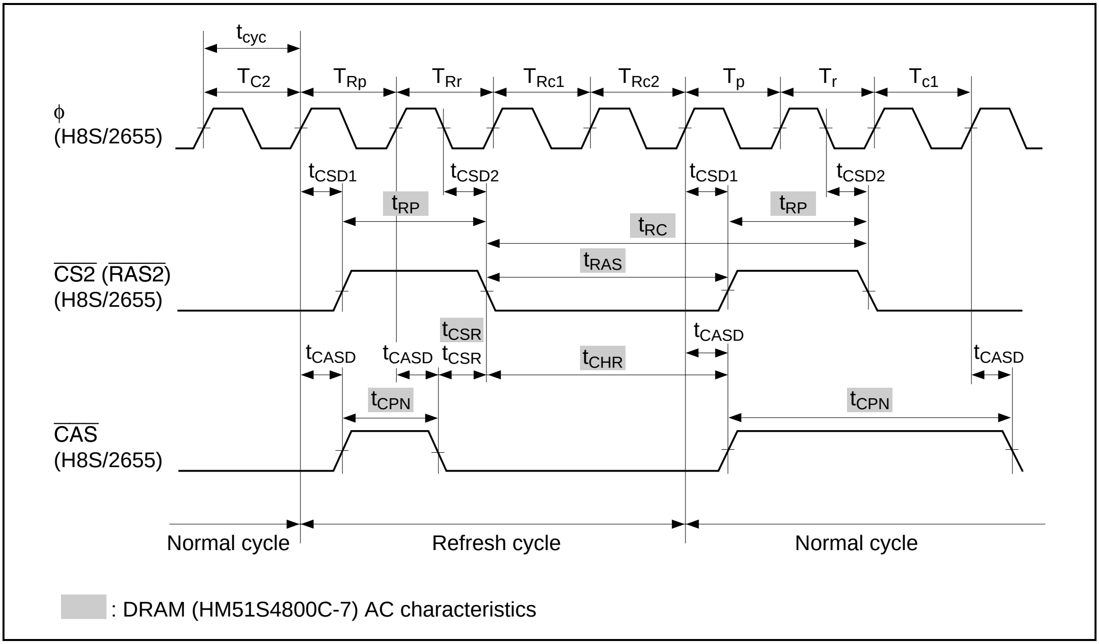


Figure 3.3.4 (e) $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Timing Chart

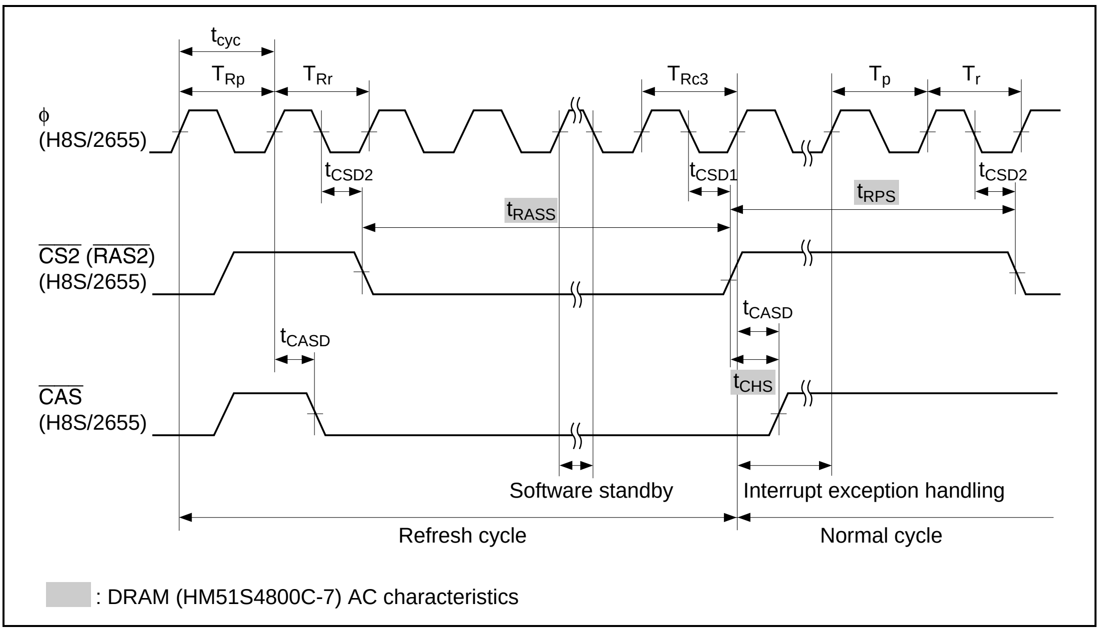


Figure 3.3.4 (f) Self-Refresh Timing Chart

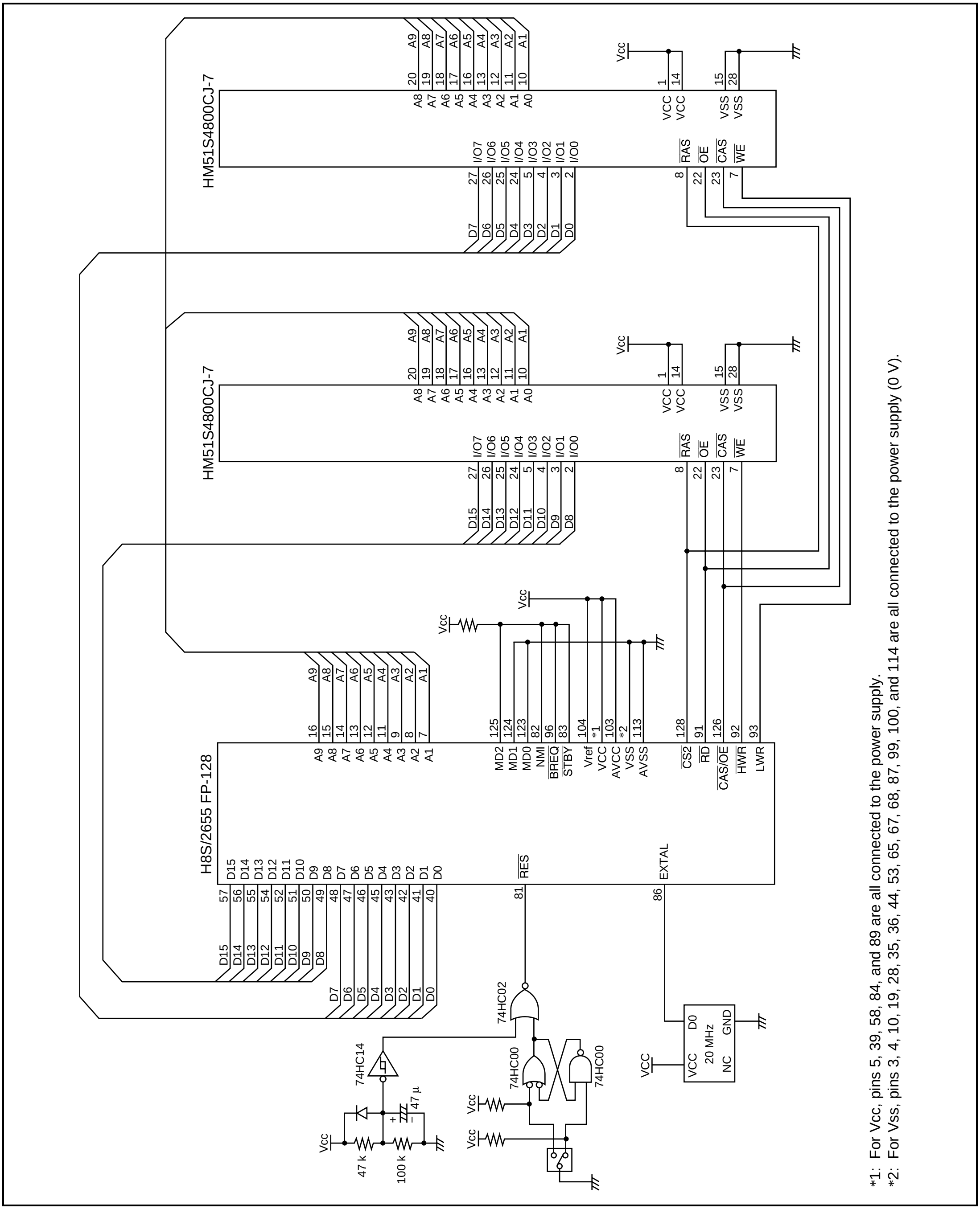


Figure 3.3.4 (g) HM51S4800CJ-7 Interface

3.11 DRAM (HM51S4800C-7) Interface Using 8-Bit Bus Mode

DRAM (HM51S4800C-7) Interface	MCU: H8S/2655	Functions Used: Mode 4 (8-Bit Bus Mode)

Specifications

1. Figure 3.3.5 (a) shows an example of the connection between an H8S/2655 and ×8-bit configuration DRAM (HM51S4800C-7). The H8S/2655 is set to mode 4 8-bit bus mode, and the DRAM is allocated to area 3.

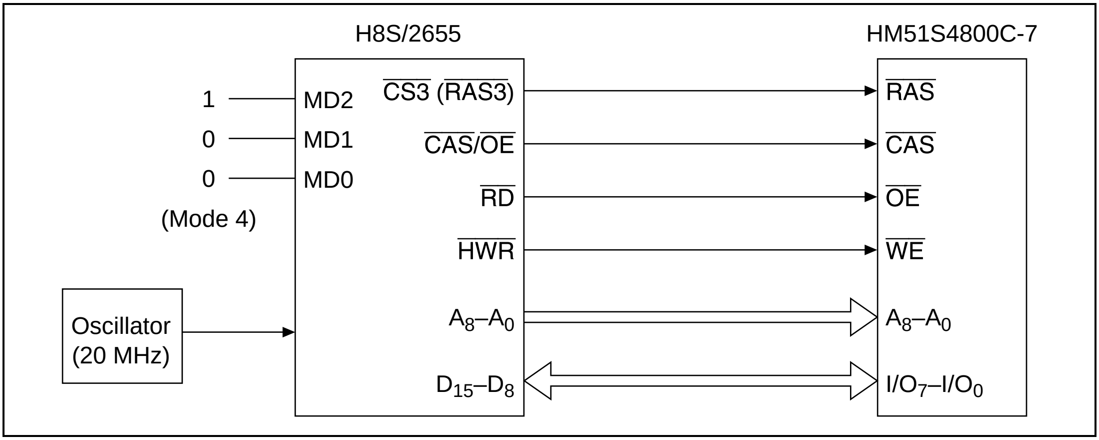


Figure 3.3.5 (a) Example of Connection between H8S/2655 and DRAM

2. Figure 3.3.5 (b) shows the memory map. When the 16-Mbyte address space is divided into areas in 2-Mbyte units, the DRAM area is H'60 0000–H'67 FFFF.

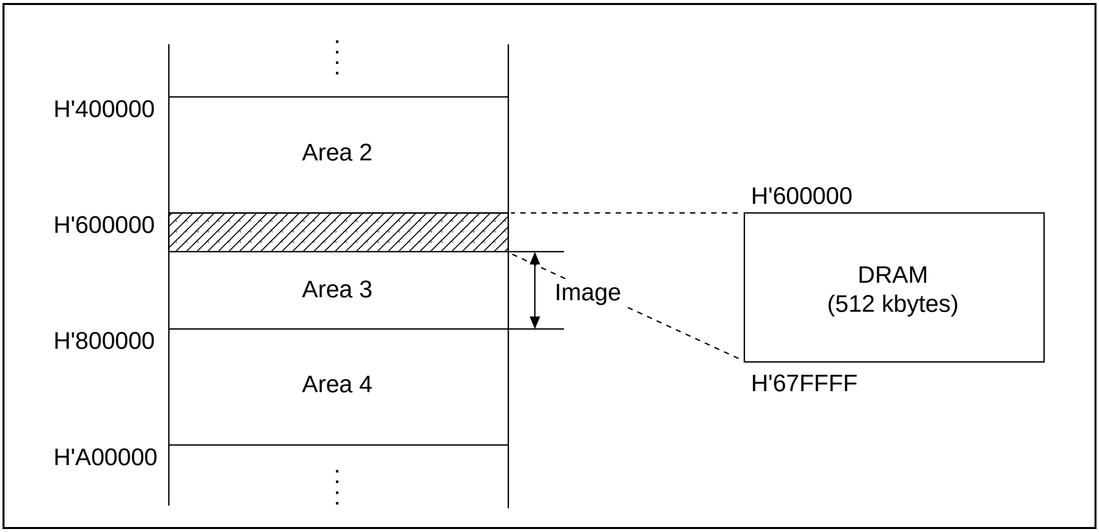


Figure 3.3.5 (b) Memory Map

3. Table 3.3.5 (a) shows the bus controller settings.

Table 3.3.5 (a) Bus Controller Settings

Name	Abbrev.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Setting
Bus width control register	ABWCR	ABW7 *	ABW6 *	ABW5 *	ABW4 *	ABW3 1	ABW2 *	ABW1 *	ABW0 *	Area 3: 8-bit access space
Access state control register	ASTCR	AST7 *	AST6 *	AST5 *	AST4 *	AST3 *	AST2 *	AST1 *	AST0 *	—
Wait control register H	WCRH	W71 *	W70 *	W61 *	W60 *	W51 *	W50 *	W41 *	W40 *	—
Wait control register L	WCRL	W31 0	W30 1	W21 *	W20 *	W11 *	W10 *	W01 *	W00 *	1 program wait state inserted
Bus control register H	BCRH	ICIS1 *	ICIS0 *	BRSTRM *	BRSTS1 *	BRSTS0 *	RMTS2 0	RMTS1 1	RMTS0 1	DRAM space: Areas 2 and 3
Bus control register L	BCRL	BRLE *	BREQOE *	EAE *	LCASS *	DDS *	ASS 1	WDBE *	WAITE *	Area partition unit: 2 Mbytes (16 Mbytes)
Memory control register	MCR	TPC 0	BE 1	RCDM 0	CW2 *	MXC1 0	MXC0 1	RLW1 0	RLW0 0	1 precharge state Fast page mode $\overline{\text{RAS}}$ up mode 2-$\overline{\text{WE}}$ control 9-bit shift $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refreshing, no wait
DRAM control register	DRAMCR	RFSHE 1	RCW 0	RMODE 0	CMF *	CMIE 0	CKS2 0	CKS1 0	CKS0 1	Refresh control performed $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refreshing wait state insertion disabled $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refreshing Compare-match interrupts disabled Refresh counter clock: ϕ/2
Refresh time constant register	RTCOR	0	1	0	0	1	1	1	1	H'4F[*1]

*: Don't care

*1: The HM51S4800C-7 uses 1024-cycle/16 ms refreshing. To allow for cases where refreshing cannot be performed at the specified time, calculations are based on twice this figure: 2048 cycles/16 ms. With a refresh counter clock of ϕ/2 (100 ns), the RTCOR value is (16 ms/2048 cycles) / 100 ns $\cong$ 79 (= H'4F).

Operation

The calculations used to check whether the AC characteristics are satisfied in DRAM access are shown below. The t_{cyc} value, unspecified min value, and unspecified max value are as follows.

- t_{cyc}: 50 ns (20 MHz oscillator (= ϕ))
- Unspecified min value: 0 ns
- Unspecified max value: min value

In the times obtained based on ϕ, the reference timing is shown in [ ].

For the timing values, see 5. AC Characteristics below.

1. Read Access

   Figure 3.3.5 (c) shows the DRAM read timing chart. Confirm that the following AC characteristics are satisfied.

Item		Symbol
DRAM (HM51S4800C-7)	Row address setup time	t_{ASR}
	Row address hold time	t_{RAH}
	Column address setup time	t_{ASC}
	Column address hold time	t_{CAH}
	$\overline{\text{RAS}}$-$\overline{\text{CAS}}$ delay time	t_{RCD}
	$\overline{\text{RAS}}$-column address delay time	t_{RAD}
	$\overline{\text{RAS}}$ precharge time	t_{RP}
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}

a. DRAM

i. Row address setup time calculation [T_{r-1} cycle rise]

$0.5\ t_{cyc} + t_{CSD2\ (min)} - t_{AD\ (max)} = 5\text{ns} \geq 0\text{ ns}\ (t_{ASR})$

ii. Row address hold time calculation

$t_{AH\ (min)} = 0.5\ t_{cyc} - 10 = 15\text{ ns} \geq 10\text{ ns}\ (t_{RAH})$

iii. Column address setup time calculation [T_{c1-1} cycle rise]

$t_{cyc} + t_{CASD\ (min)} - t_{AD\ (max)} = 30\text{ ns} \geq 0\text{ ns}\ (t_{ASC})$

iv. Column address hold time calculation [T_{w-1} cycle rise]

$2\ t_{cyc} + t_{AD\ (min)} - t_{CASD\ (max)} = 80\text{ ns} \geq 15\text{ ns}\ (t_{CAH})$

v. $\overline{RAS}$-$\overline{CAS}$ delay time calculation [T_{r-1} cycle fall]

$1.5\ t_{cyc} + t_{CASD\ (min)} - t_{CSD2\ (max)} = 55\ ns \geq 20\ ns\ (t_{RCD})$

vi. $\overline{RAS}$-column address delay time calculation

$t_{AH\ (min)} = 0.5\ t_{cyc} - 10 = 15\ ns \geq 15\ ns\ (t_{RAD})$

vii. $\overline{RAS}$ precharge time calculation [T_{p-3} cycle rise]

$1.5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD1\ (max)} = 55\ ns \geq 50\ ns\ (t_{RP})$

b. H8S/2655

i. Read data setup time calculation [T_{w-1} cycle rise]

$2\ t_{cyc} - t_{CASD\ (max)} + t_{CAC\ (max)} = 60\ ns \geq 15\ ns\ (t_{RDS})$

Note: Access times are specified as follows according to t_{RCD} and t_{RAD}.

Conditions	Applicable Time
t_{RCD} (calculated value) ≥ t_{RCD} (max) and t_{RAD} (calculated value) ≤ t_{RAD} (max)	Access time from $\overline{CAS}$ (t_{CAC})
t_{RCD} (calculated value) ≤ t_{RCD} (max) and t_{RAD} (calculated value) ≥ t_{RAD} (max)	Access time from address (t_{AA})
t_{RCD} (calculated value) ≤ t_{RCD} (max) and t_{RAD} (calculated value) ≤ t_{RAD} (max)	Access time from $\overline{RAS}$ (t_{RAC})

ii. Read data hold time calculation [T_{c1-2} cycle rise]

$t_{CASD\ (min)} + t_{OFF1\ (min)} = 0\ ns \geq 0\ ns\ (t_{RDH})$

2. Write Access

Figure 3.3.5 (d) shows the DRAM write timing chart. Confirm that the following AC characteristics are satisfied.

Item		Symbol
DRAM (HM51S4800C-7)	Write command setup time	t_{WCS}
	Write command hold time	t_{WCH}
	Write input setup time	t_{DS}
	Write input hold time	t_{DH}

a. Write command setup time calculation

$t_{WCS\ (min)} = 0.5\ t_{cyc} - 10 = 15\ ns \geq 0\ ns\ (t_{WCS})$

b. Write command hold time calculation [T_{w-1} cycle rise]

$1.5\ t_{cyc} - t_{CASD\ (max)} = 55\ ns \geq 15\ ns\ (t_{WCH})$

c. Write input setup time calculation

$t_{WDS\ (min)} = 0.5\ t_{cyc} - 20 = 5\ ns \geq 0\ ns\ (t_{DS})$

d. Write input hold time calculation [T_{w-1} cycle rise]

$1.5\ t_{cyc} + t_{WRD1\ (min)} + t_{WDH\ (min)} - t_{CASD\ (max)} = 55\ ns \geq 15\ ns\ (t_{DH})$

3. Burst Mode

a. Fast page mode

In fast page mode, confirm that the following AC characteristics are satisfied.

Item		Symbol
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}
DRAM (HM51S4800C-7)	Fast page mode $\overline{CAS}$ precharge time	t_{CP}
	Fast page mode cycle time	t_{PC}
	$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}

i. H8S/2655

i-1 Read data setup time calculation [T_{c1-2} cycle rise]

$3\ t_{cyc} - t_{CASD\ (max)} - t_{ACP\ (max)} = 90\ ns \geq 15\ ns\ (t_{RDS})$

i-2 Read data hold time calculation [T_{p-3} cycle rise]

$t_{CSD1\ (min)} + t_{OFF1\ (min)} = 0\ ns \geq 0\ ns\ (t_{RDH})$

ii. DRAM

ii-1 Fast page mode $\overline{CAS}$ precharge time calculation [T_{c1-2} cycle rise]

$t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 30\ ns \geq 10\ ns\ (t_{CP})$

ii-2 Fast page mode cycle time calculation [T_{w-1} cycle rise]

$3\ t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 130\ ns \geq 45\ ns\ (t_{PC})$

ii-3 $\overline{RAS}$ hold time from $\overline{CAS}$ precharge calculation [T_{c1-2} cycle rise]

$3\ t_{cyc} + t_{CSD1\ (min)} - t_{CASD\ (max)} = 130\ ns \geq 40\ ns\ (t_{RHCP})$

b. $\overline{RAS}$ down mode

$\overline{RAS}$ down mode can be selected by setting the RCDM bit to 1 in the memory control register (MCR).

4. Refresh Cycle

a. $\overline{CAS}$-before-$\overline{RAS}$ refreshing

Figures 3.3.5 (e) and 3.3.5 (f) show the $\overline{CAS}$-before-$\overline{RAS}$ refresh timing charts. Confirm that the following AC characteristics are satisfied. (The LCASS bit in bus control register L is written as BCRL.LCASS, and the CW2 bit in the memory control register as MCR.CW2.)

Item		**Symbol**
DRAM (HM51S4800C-7)	$\overline{RAS}$ precharge time	t_{RP}
	$\overline{CAS}$ setup time	t_{CSR}
	$\overline{RAS}$ pulse width	t_{RAS}
	$\overline{CAS}$ hold time	t_{CHR}
	Normal mode $\overline{CAS}$ precharge time	t_{CPN}
	Random read/write cycle time	t_{RC}

i. $\overline{RAS}$ precharge time

i-1 Transition from normal cycle to refresh cycle [T_{Rp} cycle rise]

$1.5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD1\ (max)} = 55\ ns \geq 50\ ns\ (t_{RP})$

i-2 Transition from refresh cycle to normal cycle

i-2.1 When BCRL.LCASS = 0 and MCR.CW2 = 0 or MCR.CW2 = 1 [T_p cycle rise]

$1.5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD1\ (max)} = 55\ ns \geq 50\ ns\ (t_{RP})$

i-2.2 When BCRL.LCASS = 1 and MCR.CW2 = 0 [T_{RI} cycle rise]

$2.5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD1\ (max)} = 105\ ns \geq 50\ ns\ (t_{RP})$

ii. $\overline{CAS}$ setup time

$t_{CSR\ (min)} = 15\ ns \geq 10\ ns\ (t_{CSR})$

iii. $\overline{RAS}$ pulse width [T_{Rr} cycle fall]

$2.5\ t_{cyc} + t_{CSD1\ (min)} - t_{CSD2\ (max)} = 105\ ns \geq 70\ ns\ (t_{RAS})$

iv. $\overline{CAS}$ hold time [T_{Rr} cycle fall]

$2.5\ t_{cyc} + t_{CASD\ (min)} - t_{CSD2\ (max)} = 105\ ns \geq 10\ ns\ (t_{CHR})$

v. Normal mode $\overline{CAS}$ precharge time

v-1 Transition from normal cycle to refresh cycle [T_{Rp} cycle rise]

$t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 70$ ns ≥ 10 ns (t_{CPN})

v-2 Transition from refresh cycle to normal cycle [T_p cycle rise]

v-2.1 When BCRL.LCASS = 0 and MCR.CW2 = 0 or MCR.CW2 = 1 [T_p cycle rise]

$3\ t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 130$ ns ≥ 10 ns (t_{CPN})

v-2.2 When BCRL.LCASS = 1 and MCR.CW2 = 0 [T_{RI} cycle rise]

$4\ t_{cyc} + t_{CASD\ (min)} - t_{CASD\ (max)} = 180$ ns ≥ 10 ns (t_{CPN})

vi. Random read/write cycle time [T_{Rr} cycle fall]

vi-1 When BCRL.LCASS = 0 and MCR.CW2 = 0 or MCR.CW2 = 1

$4\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD2\ (max)} = 180$ ns ≥ 130 ns (t_{RC})

vi-2 When BCRL.LCASS = 1 and MCR.CW2 = 0

$5\ t_{cyc} + t_{CSD2\ (min)} - t_{CSD2\ (max)} = 230$ ns ≥ 130 ns (t_{RC})

b. Self-refresh mode

Figure 3.3.5 (g) shows the self-refresh timing chart.

A transition can be made to self-refresh mode by setting the RMODE bit to 1 in the DRAM control register (DRAMCR), then executing a SLEEP instruction to enter software standby mode.

In self-refresh mode, confirm that the following AC characteristics are satisfied.

Item		**Symbol**
DRAM (HM51S4800C-7)	$\overline{RAS}$ pulse width	t_{RASS}
	$\overline{CAS}$ hold time	t_{CHS}
	$\overline{RAS}$ precharge time	t_{RPS}

i. $\overline{RAS}$ pulse width calculation [T_{Rr} cycle fall]

$3.5\ t_{cyc}$ + (software standby time) + $t_{CSD1\ (max)} - t_{CSD2\ (min)}$

= 105 + (software standby time) ns $\geq$ 100 ns (t_{RASS})

ii. $\overline{CAS}$ hold time calculation [T_{Rc} cycle fall]

$0.5\ t_{cyc} + t_{CASD\ (min)} - t_{CSD1\ (max)} = 5$ ns ≥ -50 ns (t_{CHS})

iii. $\overline{RAS}$ precharge time calculation [T_{Rc} cycle fall]

When the interrupt handling routine area is in DRAM:

t_{cyc} + (interrupt exception handling time) + $1.5\ t_{cyc} + t_{CSD2\ (max)} - t_{CSD1\ (min)}$
= 105 + (interrupt exception handling time) ns $\geq$ 130 ns (t_{RPS})

Note: Under the following conditions, the interrupt exception handling time is 21 t_{cyc} = 1050 ns, so that the above $\overline{\text{RAS}}$ precharge time inequality is true.

- Interrupt mode: Mode 0
- Area 0 access states: 4
- Stack area access states: 3

5. AC Characteristics

Table 3.3.5 (b) shows the AC characteristics of the H8S/2655, and table 3.3.5. (c) the AC characteristics of the HM51S4800C-7.

Table 3.3.5 (b) AC Characteristics of H8S/2655

Item	Symbol	Min	Max	Unit
Address delay time	t_{AD}	—	20	ns
Address hold time	t_{AH}	$0.5 \times t_{cyc} - 10$	—	ns
$\overline{\text{CS}}$ delay time 1	t_{CSD1}	—	20	ns
$\overline{\text{CS}}$ delay time 2	t_{CSD2}	—	20	ns
$\overline{\text{RD}}$ delay time 1	t_{RSD1}	—	20	ns
$\overline{\text{CAS}}$ delay time	t_{CASD}	—	20	ns
Read data setup time	t_{RDS}	15	—	ns
Read data hold time	t_{RDH}	0	—	ns
$\overline{\text{WR}}$ delay time 1	t_{WRD1}	—	20	ns
Write data setup time	t_{WDS}	$0.5 \times t_{cyc} - 20$	—	ns
Write data hold time	t_{WDH}	$0.5 \times t_{cyc} - 10$	—	ns
$\overline{\text{WR}}$ setup time	t_{WCS}	$0.5 \times t_{cyc} - 10$	—	ns

Table 3.3.5 (c) AC Characteristics of HM51S4800C-7

Item	Symbol	Min	Max	Unit
Random read/write cycle time	t_{RC}	130	—	ns
$\overline{RAS}$ precharge time	t_{RP}	50	—	ns
$\overline{RAS}$ pulse width	t_{RAS}	70	10000	ns
Row address setup time	t_{ASR}	0	—	ns
Row address hold time	t_{RAH}	10	—	ns
Column address setup time	t_{ASC}	0	—	ns
Column address hold time	t_{CAH}	15	—	ns
$\overline{RAS}$-$\overline{CAS}$ delay time	t_{RCD}	20	50	ns
$\overline{RAS}$-column address delay time	t_{RAD}	15	35	ns
Access time from $\overline{RAS}$	t_{RAC}	—	70	ns
Access time from $\overline{CAS}$	t_{CAC}	—	20	ns
Access time from address	t_{AA}	—	35	ns
Access time from $\overline{OE}$	t_{OAC}	—	20	ns
Output buffer turn-off time	t_{OFF1}	0	15	ns
Write command setup time	t_{WCS}	0	—	ns
Write command hold time	t_{WCH}	15	—	ns
Data input setup time	t_{DS}	0	—	ns
Data input hold time	t_{DH}	15	—	ns
$\overline{CAS}$ setup time	t_{CSR}	10	—	ns
$\overline{CAS}$ hold time	t_{CHR}	10	—	ns
Normal mode $\overline{CAS}$ precharge time	t_{CPN}	10	—	ns
Fast page mode cycle time	t_{PC}	45	—	ns
Fast page mode $\overline{CAS}$ precharge time	t_{CP}	10	—	ns
Access time from $\overline{CAS}$ precharge	t_{ACP}	—	40	ns
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{RHCP}	40	—	ns
Self-refresh $\overline{RAS}$ pulse width	t_{RASS}	100	—	ns
Self-refresh $\overline{RAS}$ precharge time	t_{RPS}	130	—	ns
Self-refresh $\overline{CAS}$ hold time	t_{CHS}	–50	—	ns

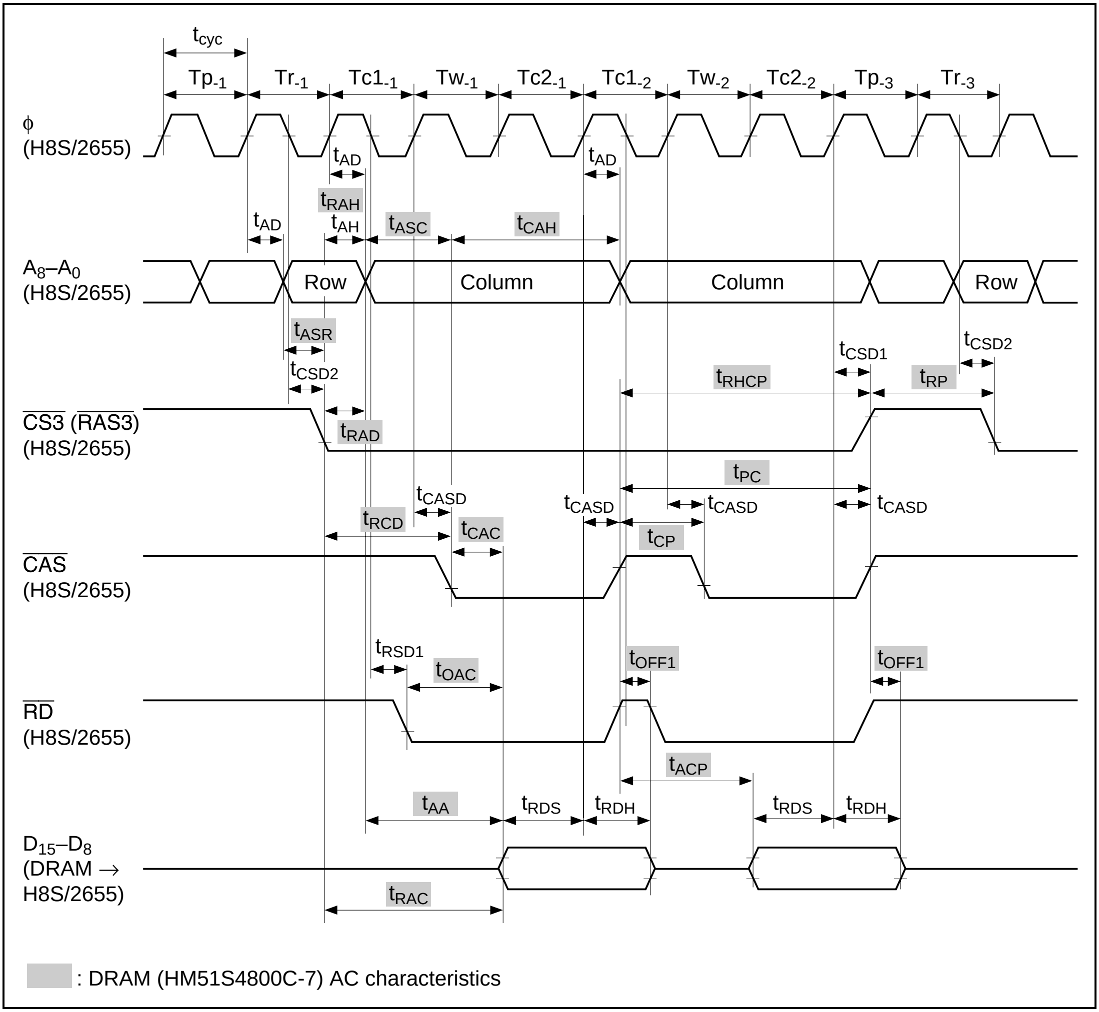


Figure 3.3.5 (c) DRAM Read Timing Chart

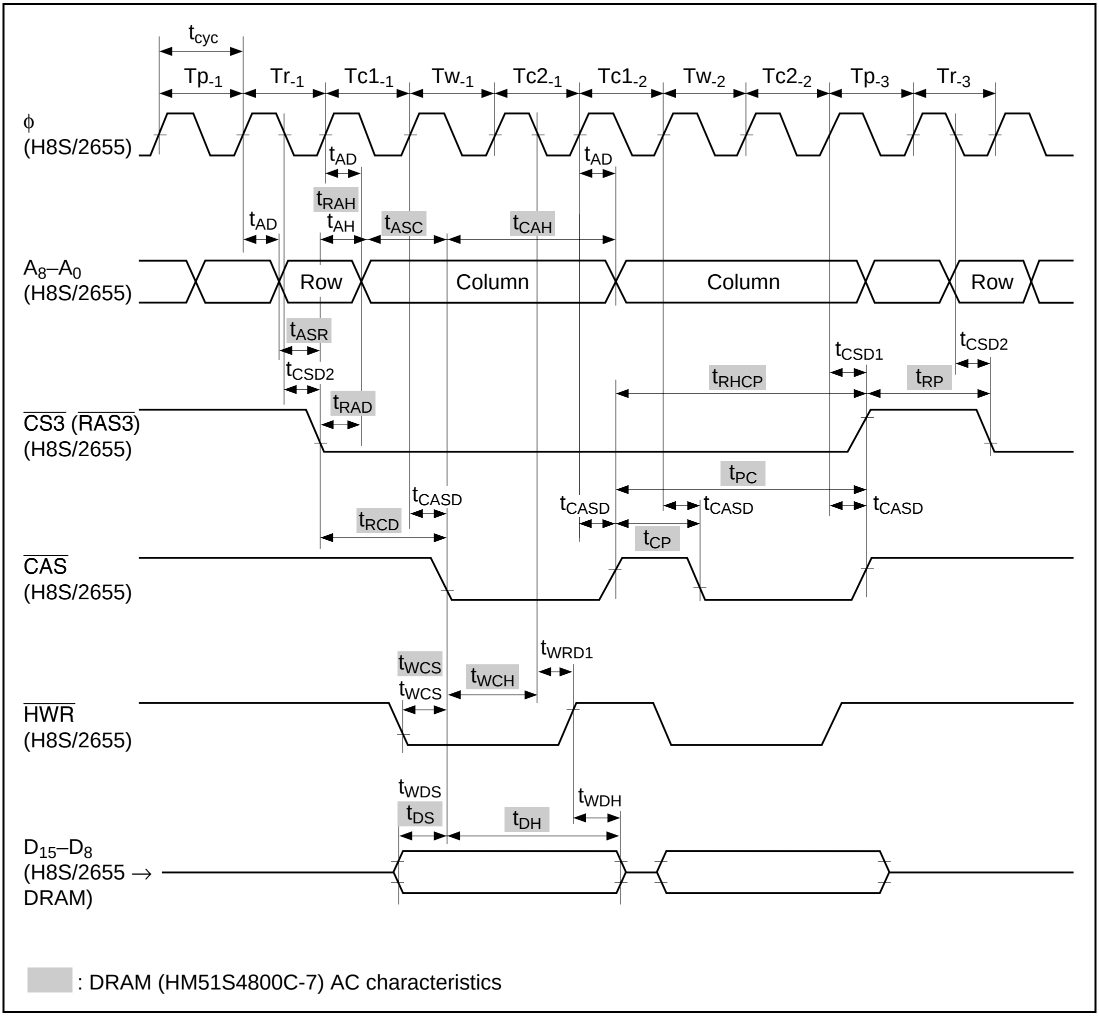


Figure 3.3.5 (d) DRAM Write Timing Chart

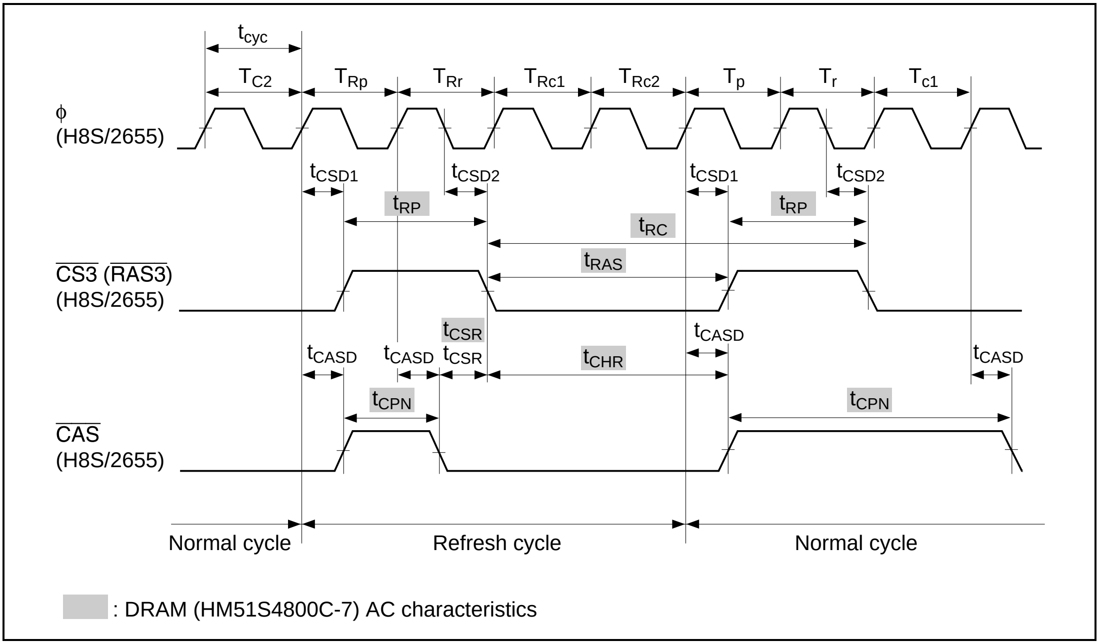


Figure 3.3.5 (e) $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Timing Chart (BCRL.LCASS = 0 and MCR.CW2 = 0 or MCR.CW2 = 1)

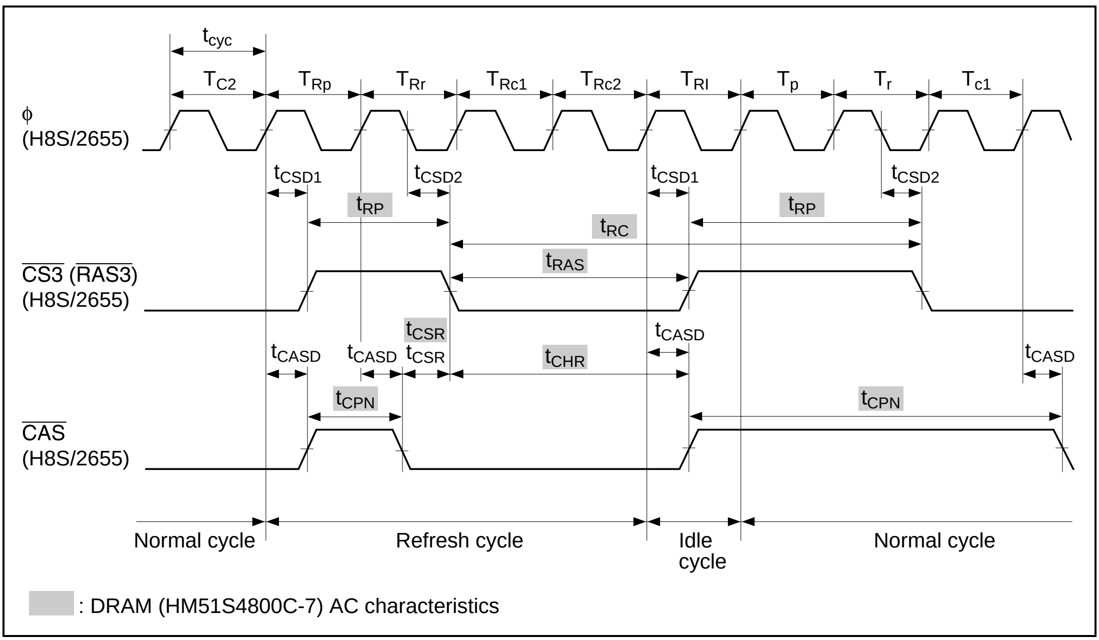


Figure 3.3.5 (f) $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Timing Chart (BCRL.LCASS = 1 and MCR.CW2 = 0)

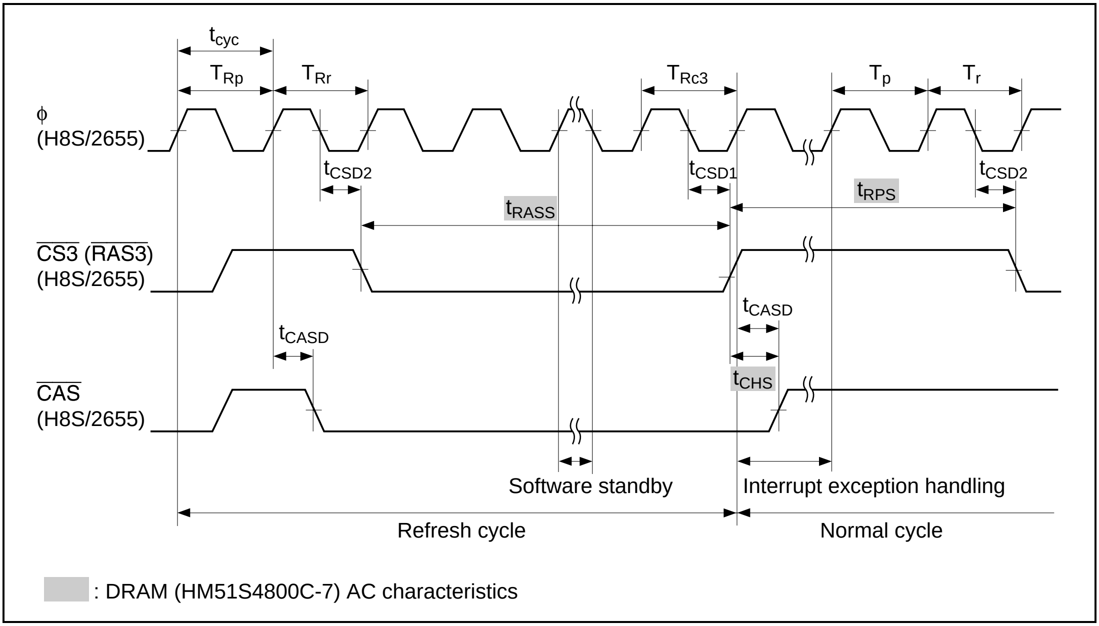


Figure 3.3.5 (g) Self-Refresh Timing Chart

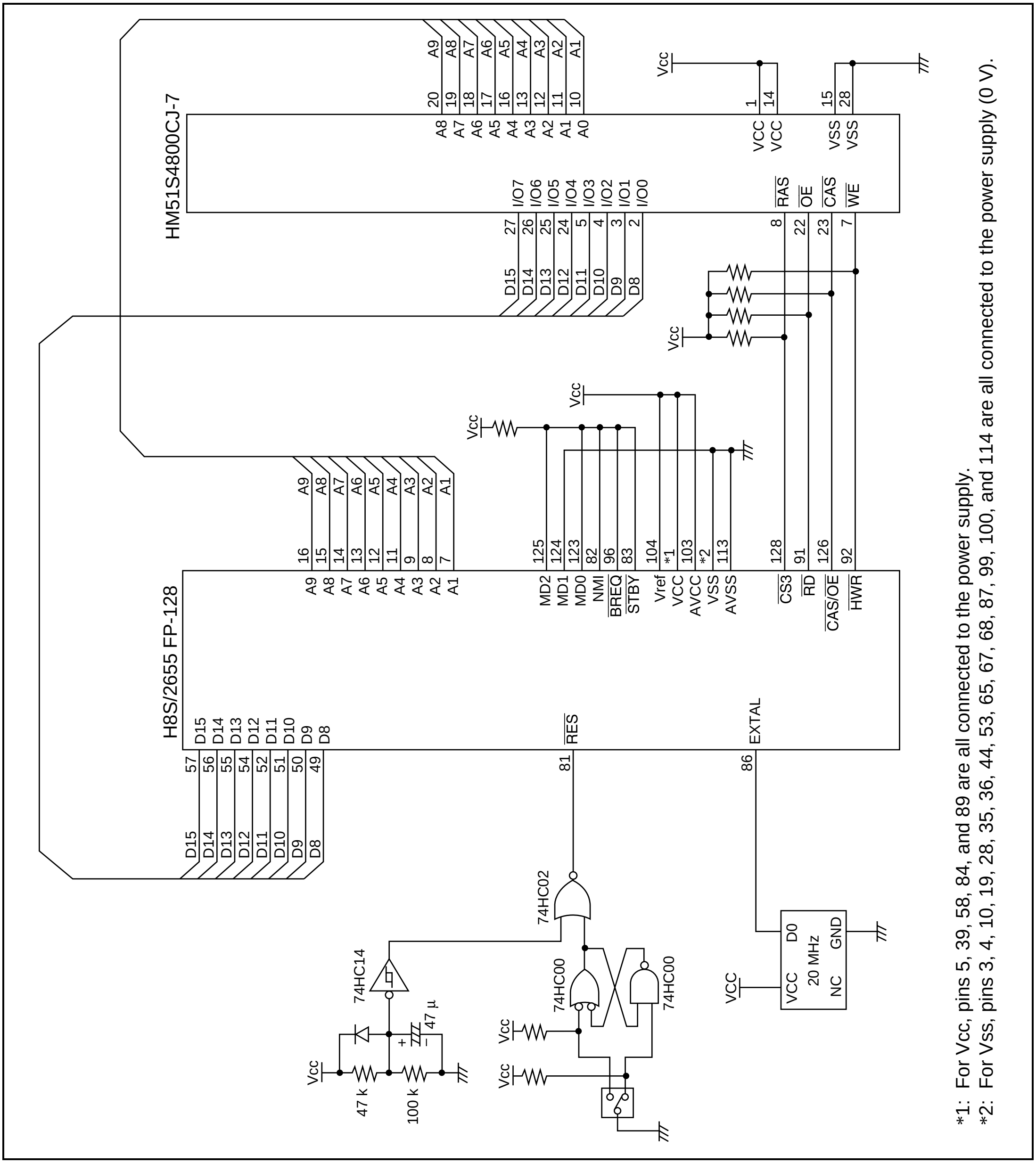


Figure 3.3.5 (h) HM51S4800CJ-7 Interface

3.12 EDO DRAM (HM51W16165J-6) Interface Using 2-CAS Control

EDO DRAM (HM51W16165J-6) Interface	MCU: H8S/2655	Functions Used: Mode 4

Specifications

1. Figure 3.3.5 (a) shows a block diagram of the connection between an H8S/2655 and an HM51W16165J-6 using mode 4 (16-Mbyte access, 16-bit data bus, on-chip ROM disabled).

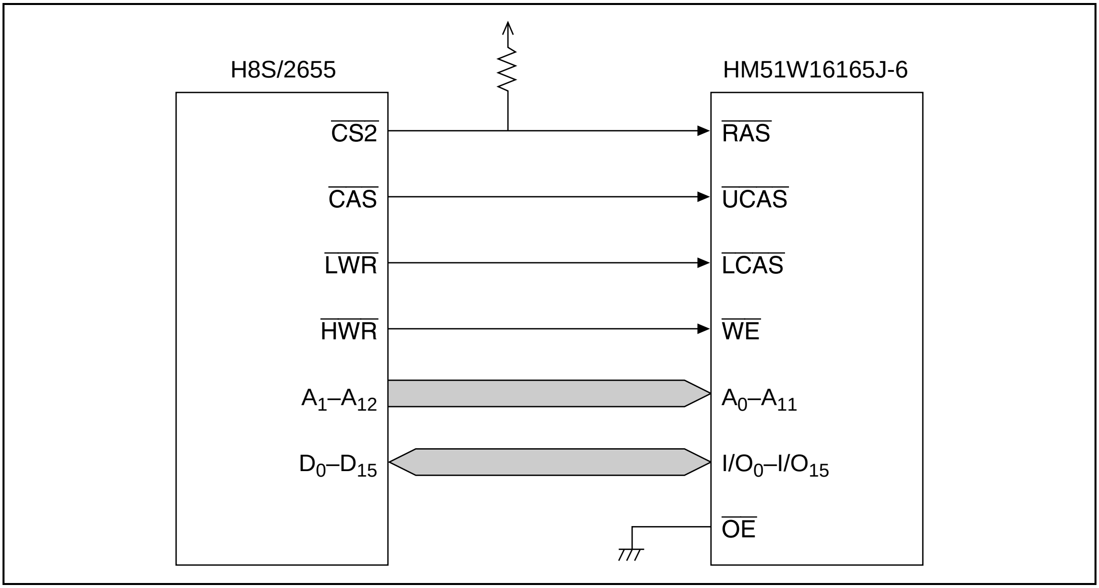


Figure 3.3.5 (a) Block Diagram of Connection between H8S/2655 and HM51W16165J-6

2. Figure 3.3.5 (b) shows the DRAM area designation.

   Area 2 (H'40 0000–H'5F FFFF) in the H8S/2655's external address space (16-Mbyte memory space) is designated as DRAM (HM51W16165J-6).

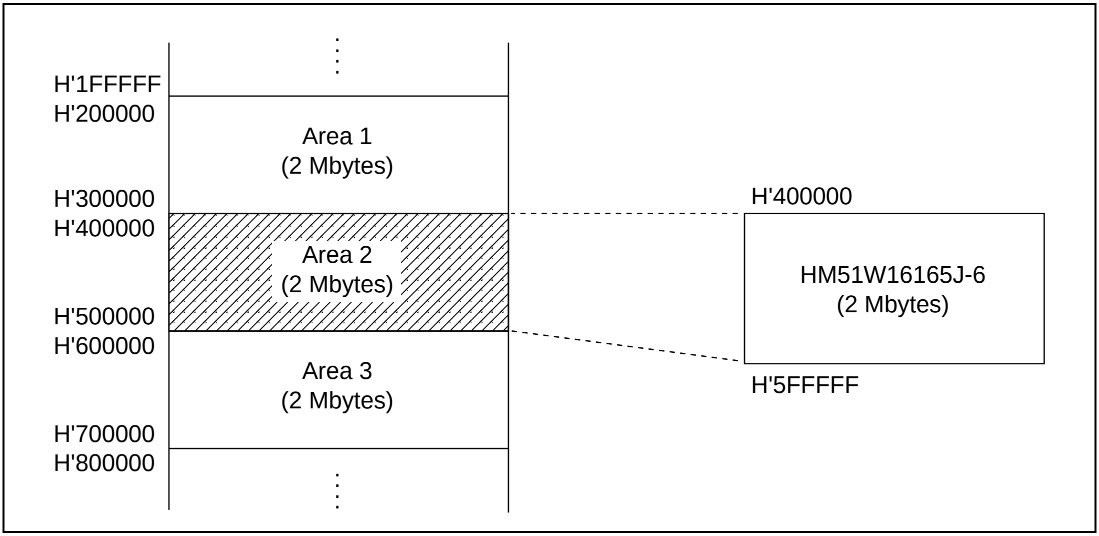


Figure 3.3.5 (b)   Designated DRAM Area (Memory Map)

Operation

Figures 3.3.5 (c) and 3.3.5 (d) show the EDO page mode read cycle and EDO page mode write cycle.

When an HM51W16165J-6 is connected to the H8S/2655, check whether the following timing conditions can be satisfied.

1. EDO Page Mode Read Cycle
   a. Read data setup time from RAS

      $t_{RAC} = 2\phi + t_{CL\ (max)} - t_{CSD2\ (max)} - t_{RDS\ (min)}$
      $= 100\ ns + 20\ ns - 20\ ns - 15\ ns$
      $= 85\ ns \geq 60\ ns$ (memory, max)

   b. Read data access time from CAS

      $t_{CAC} = t_{ACC1\ (max)}$
      $= 25\ ns \geq 15\ ns$ (memory, max)

   c. Read data access time from address

      $t_{AA} = t_{ACC3\ (max)}$
      $= 75\ ns \geq 30\ ns$ (memory, max)

   d. Read data access time from RAS

      $t_{DS} = t_{ACC4\ (max)}$
      $= 100\ ns \geq 60\ ns$ (memory, max)

2. EDO Page Mode Early Write Cycle
   a. Write data setup time from CAS

      $t_{DS} = t_{WDS\ (min)}$
      $= 5\ ns \geq 0\ ns$ (memory, min)

   b. Write data hold time from CAS

      $t_{DH} = t_{CH\ (min)} + t_{CF\ (min)} + t_{WRD1\ (min)} + t_{WDH\ (min)} - t_{CASD\ (max)}$
      $= 20\ ns + 0\ ns + 0\ ns + 15\ ns - 20\ ns$
      $= 15\ ns \geq 10\ ns$ (memory, min)

   c. Write command setup time from CAS

      $t_{WCS} = t_{WCS\ (min)}$
      $= 5\ ns \geq 0\ ns$ (memory, min)

   d. Write command hold time from CAS

      $t_{WCH} = t_{WCH\ (min)}$
      $= 15\ ns \geq 10\ ns$ (min)

3. Common to Read and Write Accesses

a. RAS setup time

$t_{ASR} = t_{AS\,(min)}$
$= 10\text{ ns} \geq 0\text{ ns (memory, min)}$

b. RAS hold time

$t_{RAH} = t_{AH\,(min)}$
$= 15\text{ ns} \geq 10\text{ ns (memory, min)}$

c. EDO page mode RAS pulse width

$t_{RASP} = 2\phi + t_{CSD1\,(min)} + t_{CL\,(min)} - t_{CSD2\,(max)}$
$= 100\text{ ns} + 0\text{ ns} + 20\text{ ns} - 20\text{ ns}$
$= 100\text{ ns} \geq 0\text{ ns (memory, min)}$

d. CAS pulse width

$t_{CAS} = \phi + t_{CASD\,(min)} - t_{CASD\,(max)} + t_{CR\,(min)}$
$= 50\text{ ns} + 0\text{ ns} - 20\text{ ns} + 0\text{ ns}$
$= 30\text{ ns} \geq 10\text{ ns (memory, min)}$

e. CAS hold time

$t_{CSH} = 1.5\phi + t_{CASD\,(min)} - t_{CSD2\,(max)}$
$= 75\text{ ns} + 0\text{ ns} - 20\text{ ns}$
$= 55\text{ ns} \geq 40\text{ ns (memory, min)}$

f. RAS hold time

$t_{RSH} = \phi + t_{CSD1\,(min)} - t_{CASD\,(max)}$
$= 50\text{ ns} + 0\text{ ns} - 20\text{ ns}$
$= 30\text{ ns} \geq 13\text{ ns (memory, min)}$

g. RAS precharge time

$t_{RP} = t_{PCH\,(min)}$
$= 55\text{ ns} \geq 40\text{ ns (memory, min)}$

As it has been confirmed that the above EDO page mode/early write cycle timing conditions are satisfied, interfacing is performed with no wait.

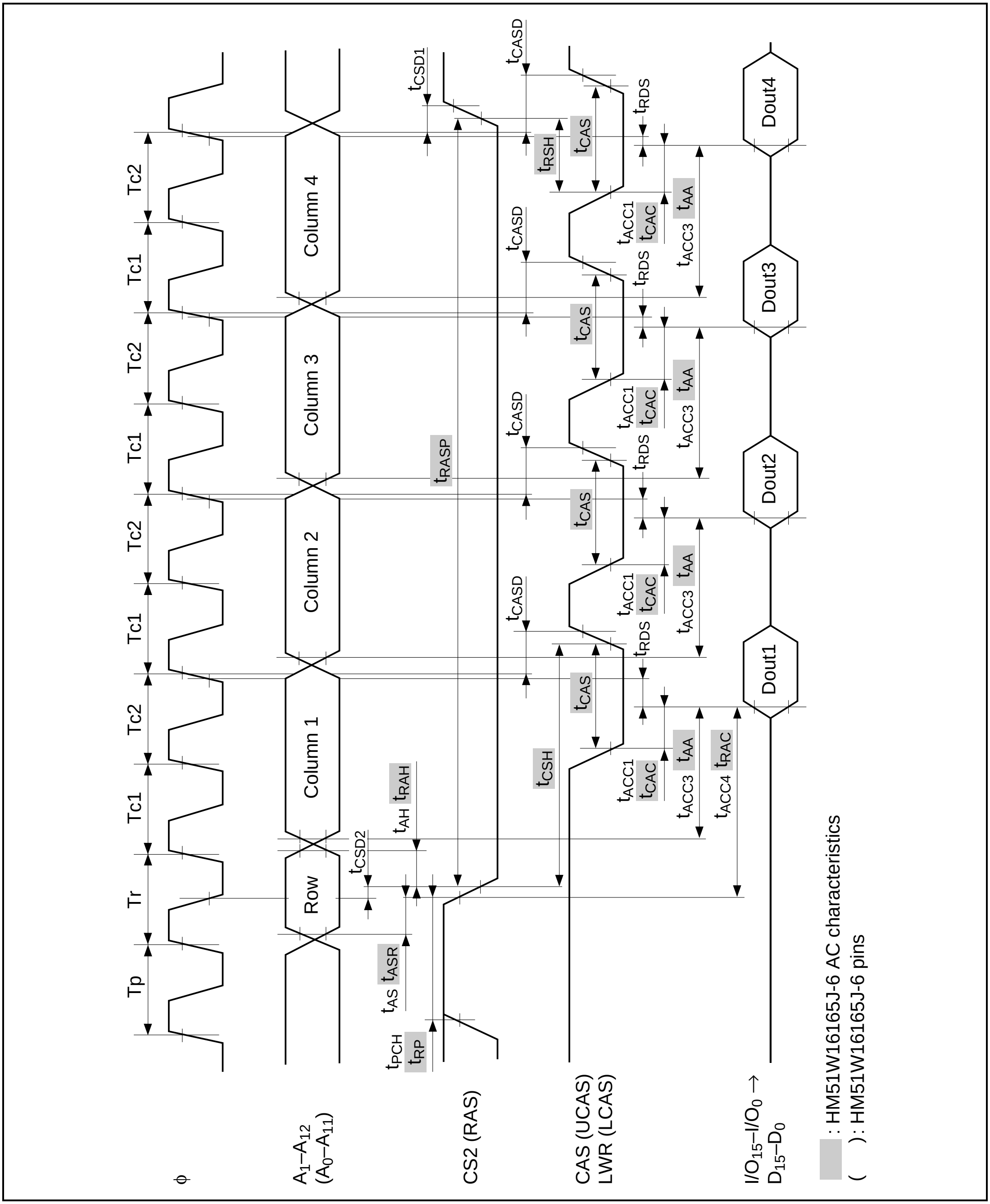


Figure 3.3.5 (c) EDO Page Mode Read Cycle

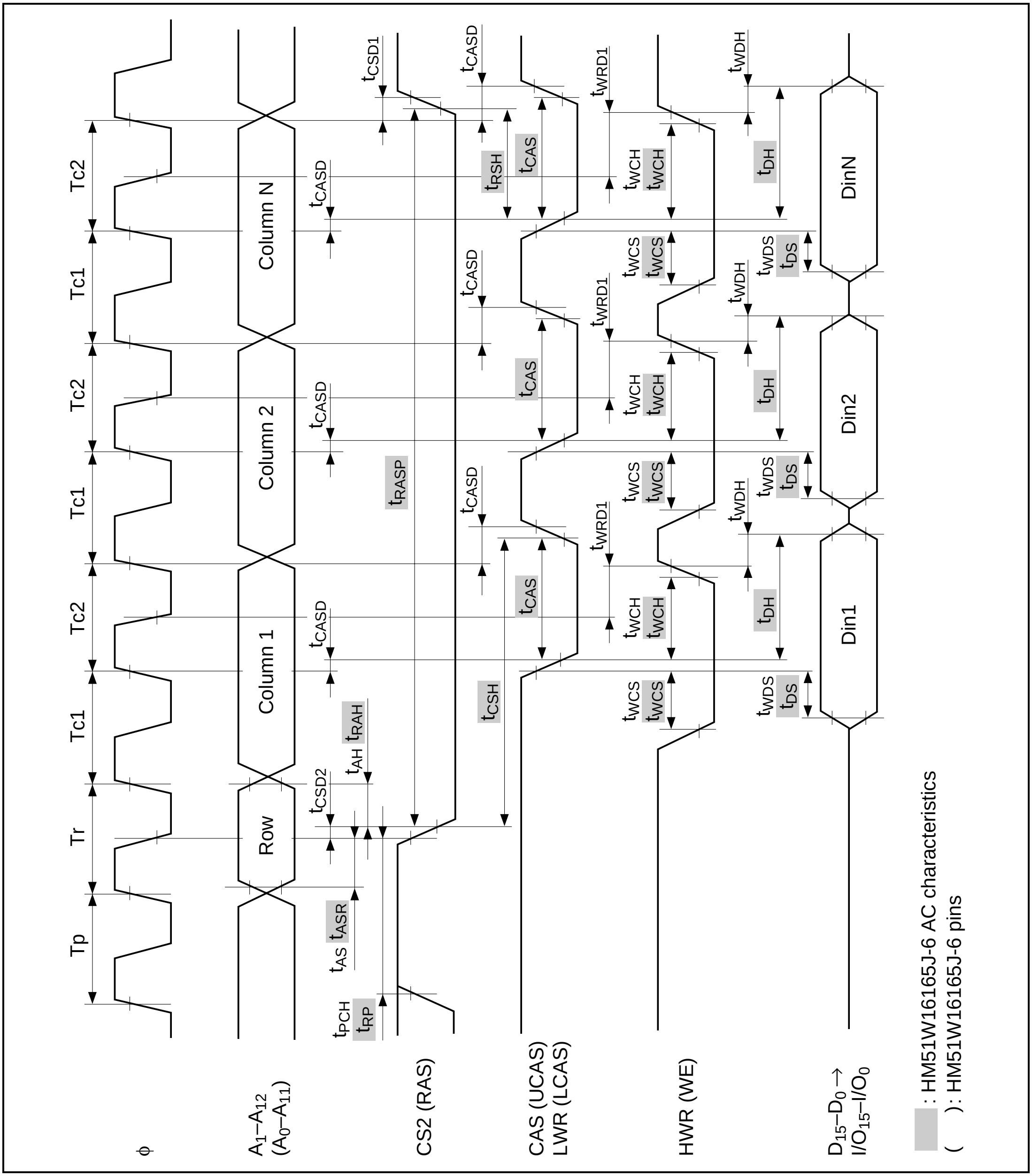


Figure 3.3.5 (d) EDO Page Mode Early Write Cycle

Figure 3.3.5 (e) shows the CAS-before-RAS refresh cycle.

When an HM51W16165J-6 is connected to the H8S/2655, check whether the following timing conditions can be satisfied.

4. CAS-Before-RAS Refresh
   a. CAS setup time

      $t_{CSR} = t_{CSR\,(min)}$
      $= 15\text{ ns} \geq 5\text{ ns (memory, min)}$

   b. CAS hold time

      $t_{CHR} = 2\phi + t_{CASD\,(min)} + t_{CL\,(min)} + t_{CR\,(min)} - t_{CSD2\,(max)} - t_{CR\,(min)}$
      $= 100\text{ ns} + 0\text{ ns} + 20\text{ ns} + 0\text{ ns} - 20\text{ ns}$
      $= 100\text{ ns} \geq 10\text{ ns (memory, min)}$

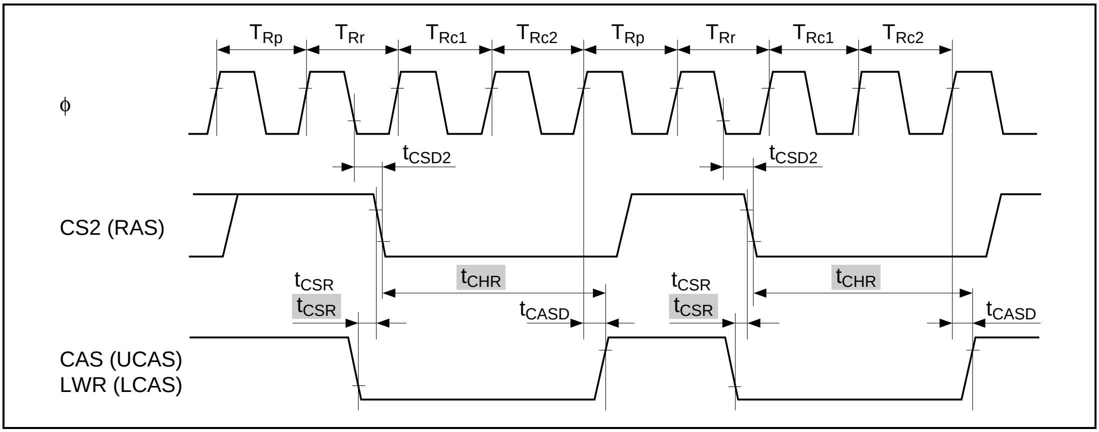


Figure 3.3.5 (e) CAS-Before-RAS Refresh Cycle

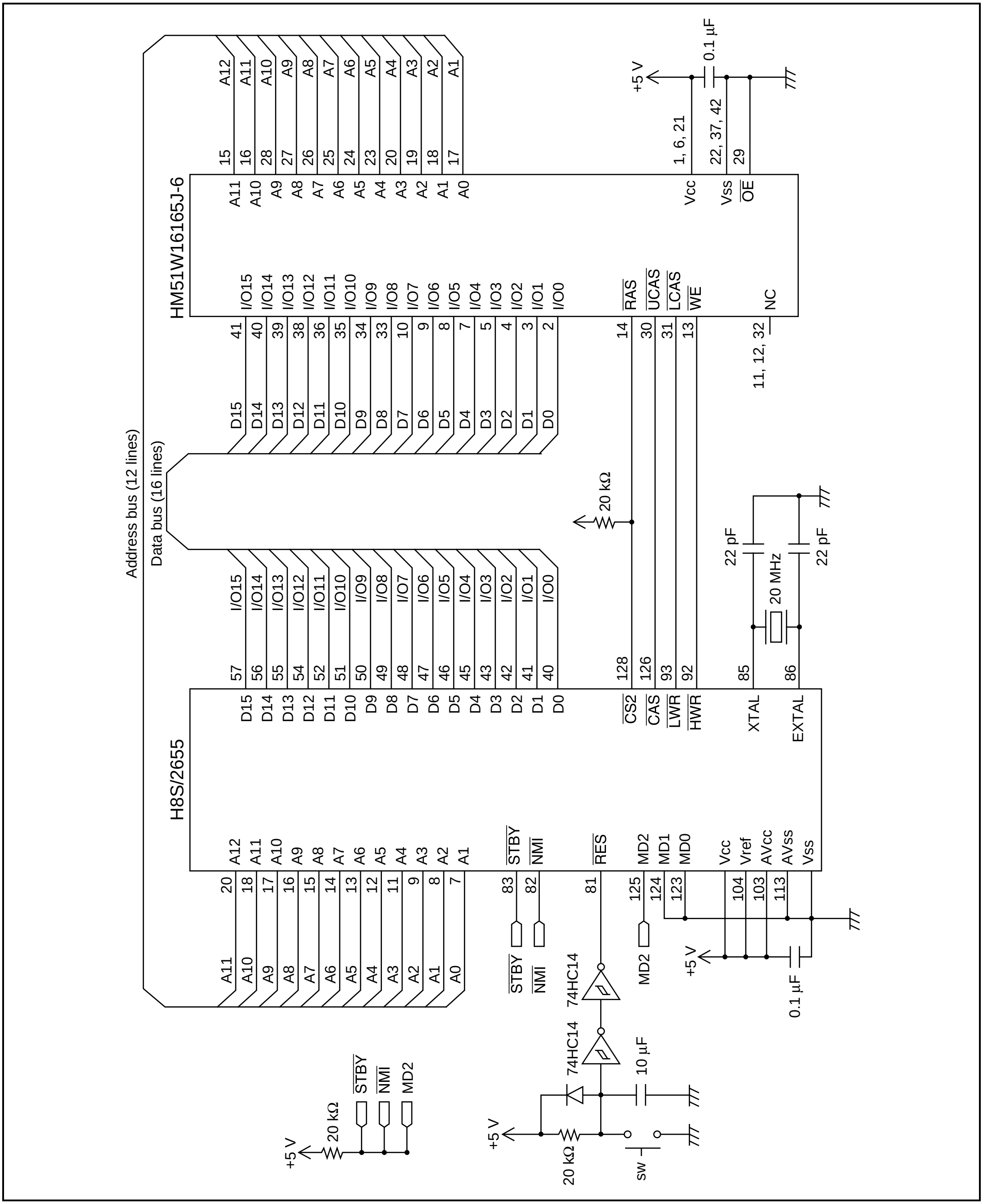


Figure 3.3.5 (f) HM51W16165J-6 Interface

3.13 Pseudo-SRAM (HM658512A-10) Interface Using 16-Bit Bus Mode

Pseudo-SRAM (HM658512A-10) Interface	MCU: H8S/2655	Functions Used: Mode 4 (16-Bit Bus Mode)

Specifications

1. Figure 3.4.1 (a) shows an example of the connection between an H8S/2655 and ×8-bit configuration pseudo-SRAMs (HM658512A-10s). The H8S/2655 is set to mode 4 16-bit bus mode, and the pseudo-SRAMs are allocated to area 2.

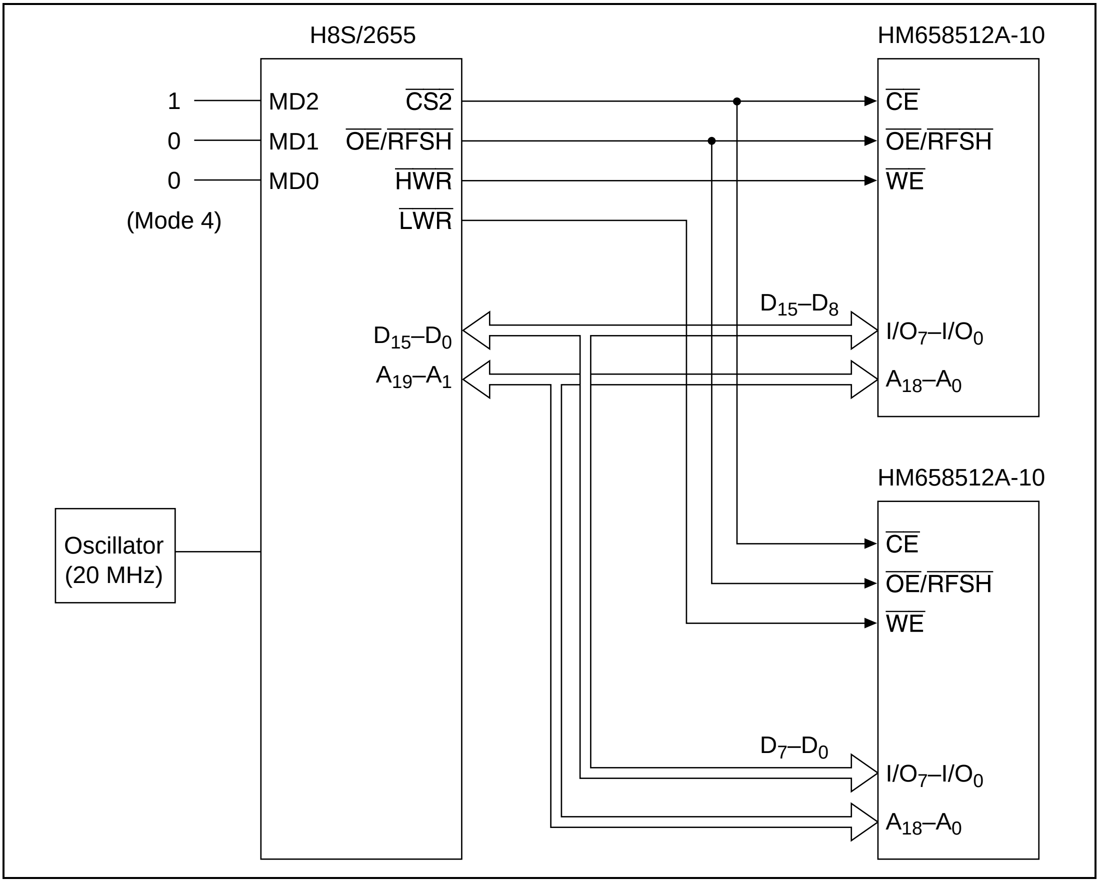


Figure 3.4.1 (a) Example of Connection between H8S/2655 and Pseudo-SRAMs

2. Figure 3.4.1 (b) shows the memory map. When the 16-Mbyte address space is divided into areas in 2-Mbyte units, the pseudo-SRAM area is H'40 0000–H'4F FFFF.

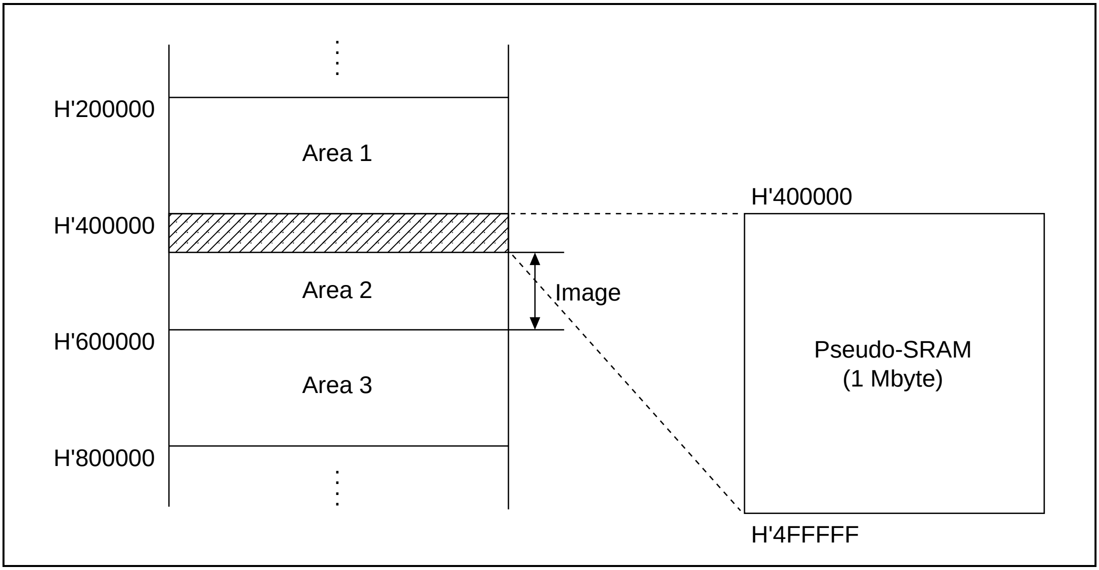


Figure 3.4.1 (b) Memory Map

3. Table 3.4.1 (a) shows the bus controller settings.

Table 3.4.1 (a) Bus Controller Settings

Name	Abbrev.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Setting
Bus width control register	ABWCR	ABW7 *	ABW6 *	ABW5 *	ABW4 *	ABW3 *	ABW2 0	ABW1 *	ABW0 *	Area 2: 16-bit access space
Access state control register	ASTCR	AST7 *	AST6 *	AST5 *	AST4 *	AST3 *	AST2 1	AST1 *	AST0 *	Area 2: 3-state access space
Wait control register H	WCRH	W71 *	W70 *	W61 *	W60 *	W51 *	W50 *	W41 *	W40 *	—
Wait control register L	WCRL	W31 *	W30 *	W21 0	W20 1	W11 *	W10 *	W01 *	W00 *	Area 2: 1 program wait state inserted
Bus control register H	BCRH	ICIS1 *	ICIS0 *	BRSTRM *	BRSTS1 *	BRSTS0 *	RMTS2 1	RMTS1 0	RMTS0 1	Area 2 only: Pseudo-SRAM space; areas 3–5: ordinary space
Bus control register L	BCRL	BRLE *	BREQOE *	EAE *	LCASS *	DDS *	ASS 1	WDBE *	WAITE *	Area partition unit: 2 Mbytes (16 Mbytes)
Memory control register	MCR	TPC 1	BE 0	RCDM *	CW2 *	MXC1 *	MXC0 *	RLW1 *	RLW0 *	2 precharge states Burst access disabled (always full access)
DRAM control register	DRAMCR	RFSHE 1	RCW 0	RMODE 0	CMF *	CMIE 0	CKS2 0	CKS1 0	CKS0 1	Refresh control performed RCW bit fixed at 0 Refresh mode: Auto-refresh Compare-match interrupts disabled Refresh counter clock: ϕ/2
Refresh time constant register	RTCOR	0	1	0	0	1	1	1	1	H'4F*1

*: Don't care

*1: Refresh time constant register (RTCOR) setting

Pseudo-SRAM (HM658512A-10) auto-refresh spec: 2048 cycles/32 ms

ϕ/2 (100 ns) is used as the CPU refresh counter clock. Although the pseudo-SRAM auto-refresh spec is 2048 cycles/32 ms, 4096/32 ms is used to provide a margin.

$\therefore$ RTCOR = (32 ms/4906 cycles) / 100 ns $\cong$ D'79 (= H'4F)

Operation

The calculations used to check whether the AC characteristics are satisfied in pseudo-SRAM access are shown below. The t_{cyc} value, unspecified min value, and unspecified max value are as follows.

- t_{cyc}: 50 ns (20 MHz oscillator (= ϕ))
- Unspecified min value: 0 ns
- Unspecified max value: min value

In the times obtained based on ϕ, the reference timing is shown in [ ].

For the timing values, see 5. AC Characteristics below.

1. Read Access

   Figure 3.4.1 (c) shows the pseudo-SRAM read timing chart. Confirm that the following items are satisfied.

Item		Symbol
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}
PSRAM (HM658512A-10)	Chip enable precharge time	t_P
	Address setup time	t_{AS}
	Address hold time	t_{AH}
	Output enable hold time	t_{OHC}

   a. H8S/2655 t_{RDS}

      i. When CS is critical

         - Setup time calculation [$T_{1\text{-}1}$ cycle fall]

           $3.5\ t_{cyc} - t_{CSD\ (max)} - t_{CEA\ (max)} = 55\ \text{ns} \geq 15\ \text{ns}\ (t_{RDS})$

      ii. When OE is critical

         - Setup time calculation [$T_{1\text{-}2}$ cycle rise]

           $3\ t_{cyc} - t_{CASD\ (max)} - t_{OEA\ (max)} = 100\ \text{ns} \geq 15\ \text{ns}\ (t_{RDS})$

   b. H8S/2655 t_{RDH}

         - Hold time calculation [$T_{P1\text{-}2}$ cycle rise]

           $t_{CASD\ (min)} + t_{OHZ\ (min)} = 0\ \text{ns} \geq 0\ \text{ns}\ (t_{RDH})$

c. Pseudo-SRAM t_P, t_{AS}, t_{AH}, and t_{OHC}

- Chip enable precharge time calculation [T_{P1-1} cycle rise]

  $2.5\ t_{cyc} - t_{CSD1\ (max)} + t_{CSD2\ (min)} = 105$ ns ≥ 50 ns (t_P)
- Address setup time calculation [T_{P1-1} cycle rise]

  $2.5\ t_{cyc} - t_{AD\ (max)} + t_{CSD2\ (min)} = 105$ ns ≥ 0 ns (t_{AS})
- Address hold time calculation [T_{P1-1} cycle fall]

  $3.5\ t_{cyc} - t_{CSD2\ (max)} + t_{AD\ (min)} = 155$ ns ≥ 30 ns (t_{AH})
- Output enable hold time calculation [T_{P1-1} cycle fall]

  $0.5\ t_{cyc} - t_{CSD2\ (max)} + t_{CASD\ (min)} = 5$ ns ≥ 0 ns (t_{OHC})

2. Write Access

Figure 3.4.1 (d) shows the pseudo-SRAM write timing chart. Confirm that the following items are satisfied.

Item		Symbol
PSRAM (HM658512A-10)	Input data setting timer	t_{DW}
	Input data hold time	t_{DH}
	Write command pulse width	t_{WP}
	Chip enable time	t_{CW}

- Input data setting time calculation [T_{2-1} cycle fall]

  $2\ t_{cyc} - t_{WDD\ (max)} + t_{WRD1\ (min)} = 70$ ns ≥ 25 ns (t_{DW})
- Input data hold time calculation

  $t_{WDH\ (min)} = 15$ ns ≥ 0 ns (t_{DH})
- Write command pulse width calculation [T_{2-1} cycle fall]

  $3\ t_{cyc} - t_{WRD1\ (max)} + t_{WRD1\ (min)} = 80$ ns ≥ 30 ns (t_{WP})
- Chip enable time calculation [T_{1-1} cycle fall]

  $3\ t_{cyc} - t_{CSD2\ (max)} + t_{WRD1\ (min)} = 130$ ns ≥ 100 ns (t_{CW})

3. Auto-Refresh Cycle

Figure 3.4.1 (e) shows the auto-refresh timing chart. Confirm that the following items are satisfied.

Item		Symbol
PSRAM (HM658512A-10)	Refresh precharge time	t_{FP}
	Refresh command pulse width	t_{FAP}
	Refresh command delay time	t_{RFD}
	Auto-refresh cycle time	t_{FC}

- Refresh precharge time calculation [T_{RP1-1} cycle rise]

  $2\ t_{cyc} - t_{CASD\,(max)} + t_{CASD\,(min)} = 80$ ns ≥ 40 ns (t_{FP})
- Refresh command pulse width calculation [T_{R1-1} cycle rise]

  $3\ t_{cyc} - t_{CASD\,(max)} + t_{CASD\,(min)} = 130$ ns ≥ 80 ns (t_{FAP})
- Refresh command delay time calculation [T_{RP1-1} cycle rise]

  $2\ t_{cyc} - t_{CSD2\,(max)} + t_{CASD\,(min)} = 80$ ns ≥ 30 ns (t_{RFD})
- Auto-refresh cycle time calculation [T_{RP1-1} cycle rise]

  $5\ t_{cyc} - t_{CSD2\,(max)} + t_{CASD\,(min)} = 230$ ns ≥ 160 ns (t_{FC})

4. Self-Refresh Cycle

Figure 3.4.1 (f) shows the self-refresh timing chart. Confirm that pseudo-SRAM t_{FAS} (refresh command pulse width) is satisfied.

- Refresh command pulse width calculation [T_{R1} cycle rise]

  $3\ t_{cyc}$ + (software standby time) (min) + $t_{CASD\,(min)}$

  = 100 ns + (software standby time) (min)

  ≥ 8 µs (t_{FAS})

Notes:
- t_{FAS} (refresh command pulse width)

  Set the software standby time so that the specified value of 8 µs (min) is satisfied.
- t_{RFS} (refresh reset time)

  Make a setting by software so that the specified value of 600 ns (min) is satisfied. During this time, an access should be made to a different area so that the $\overline{\text{CS2}}$ ($\overline{\text{CE}}$) signal is not asserted.

5. AC Characteristics

a. H8S/2655

Item	Symbol	Min	Max	Unit
Address delay time	t_{AD}	—	20	ns
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	ns
$\overline{CS}$ delay time 2	t_{CSD2}	—	20	ns
$\overline{CS}$ pulse width	t_{CSW}	$2.5 \times t_{cyc} - 20$	—	ns
$\overline{CAS}$ delay time	t_{CASD}	—	20	ns
Read data setup time	t_{RDS}	15	—	ns
Read data hold time	t_{RDH}	0	—	ns
Read data access time 3	t_{ACC3}	—	$2.0 \times t_{cyc} - 25$	ns
Read data access time 4	t_{ACC4}	—	$2.5 \times t_{cyc} - 25$	ns
$\overline{WR}$ delay time 1	t_{WRD1}	—	20	ns
Write data delay time	t_{WDD}	—	30	ns
Write data hold time	t_{WDH}	$0.5 \times t_{cyc} - 10$	—	ns

b. HM658512A-10

Item	Symbol	Min	Max	Unit
Chip enable access time	t_{CEA}	—	100	ns
Output enable access time	t_{OEA}	—	40	ns
Output disable-output delay (when Hi-Z)	t_{OHZ}	—	25	ns
Chip enable pulse width	t_{CE}	100 n	10 µ	s
Chip enable precharge time	t_{P}	50	—	ns
Address setup time	t_{AS}	0	—	ns
Address hold time	t_{AH}	25	—	ns
Write command pulse width	t_{WP}	30	—	ns
Chip enable time	t_{CW}	100	—	ns
Output enable hold time	t_{OHC}	0	—	ns
Input data setting time	t_{DW}	25	—	ns
Input data hold time	t_{DH}	0	—	ns
Refresh command delay time	t_{RFD}	50	—	ns
Refresh precharge time	t_{FP}	40	—	ns
Refresh command pulse width (auto-refresh)	t_{FAP}	80 n	18 µ	s
Auto-refresh cycle time	t_{FC}	160	—	ns
Auto-refresh cycle time (self-refresh)	t_{FAS}	8	—	µs
Refresh reset time (self-refresh)	t_{RFS}	600	—	ns

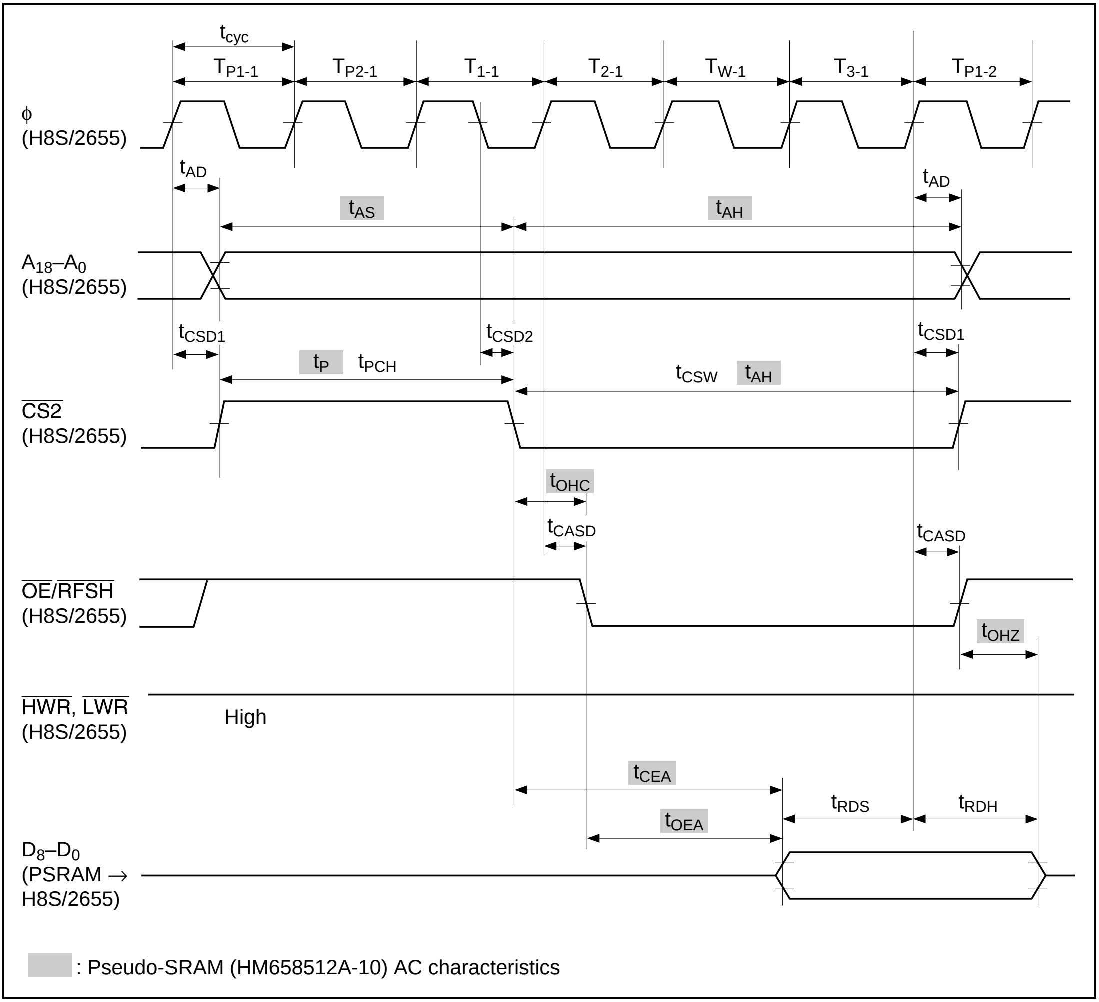


Figure 3.4.1 (c) Pseudo-SRAM Read Timing Chart

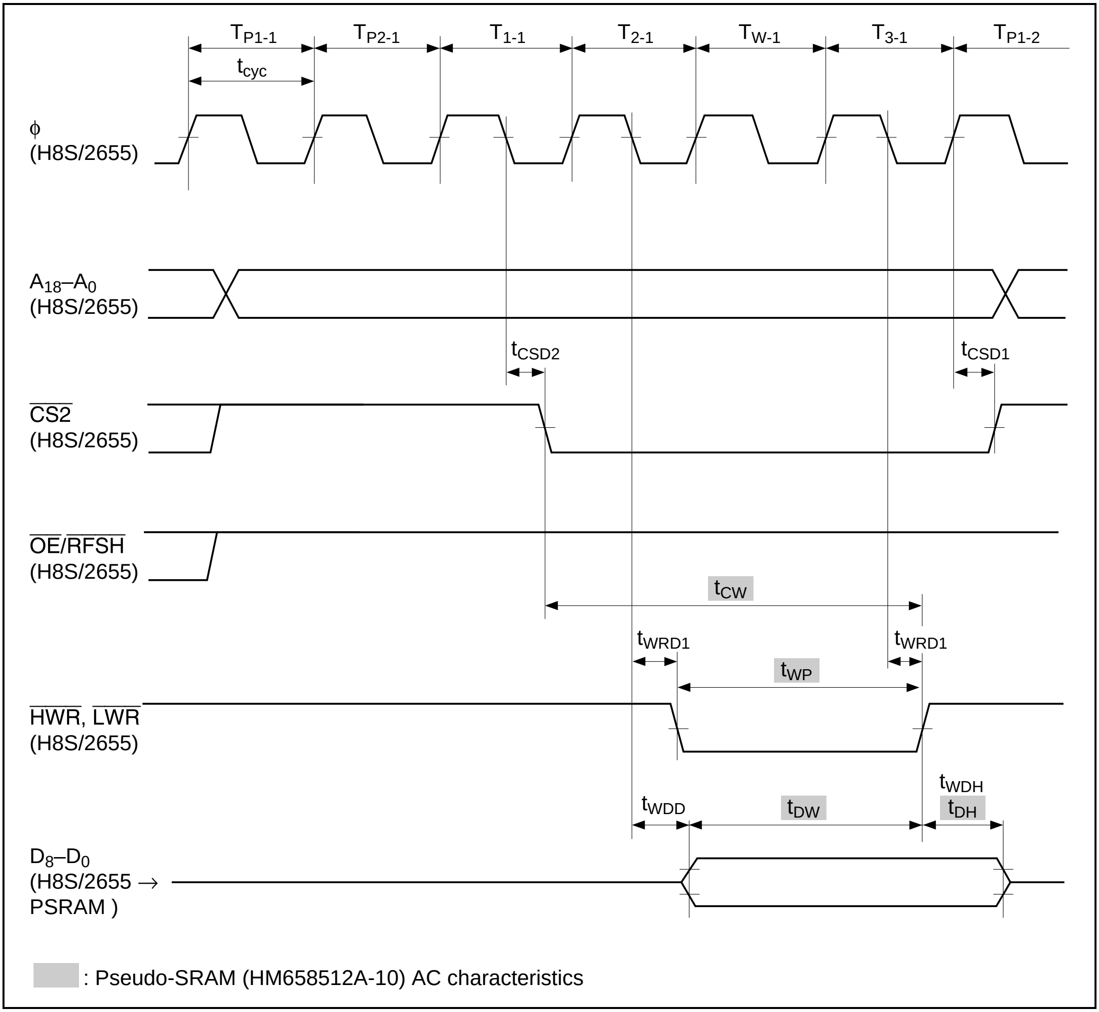


Figure 3.4.1 (d) Pseudo-SRAM Write Timing Chart

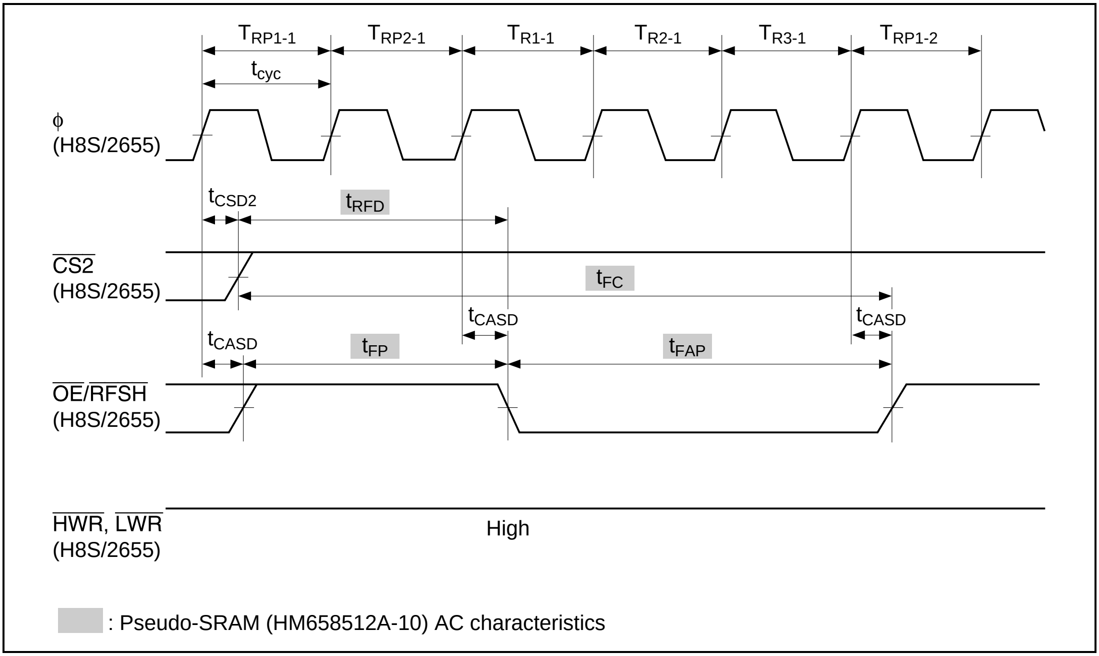


Figure 3.4.1 (e) Auto-Refresh Timing Chart

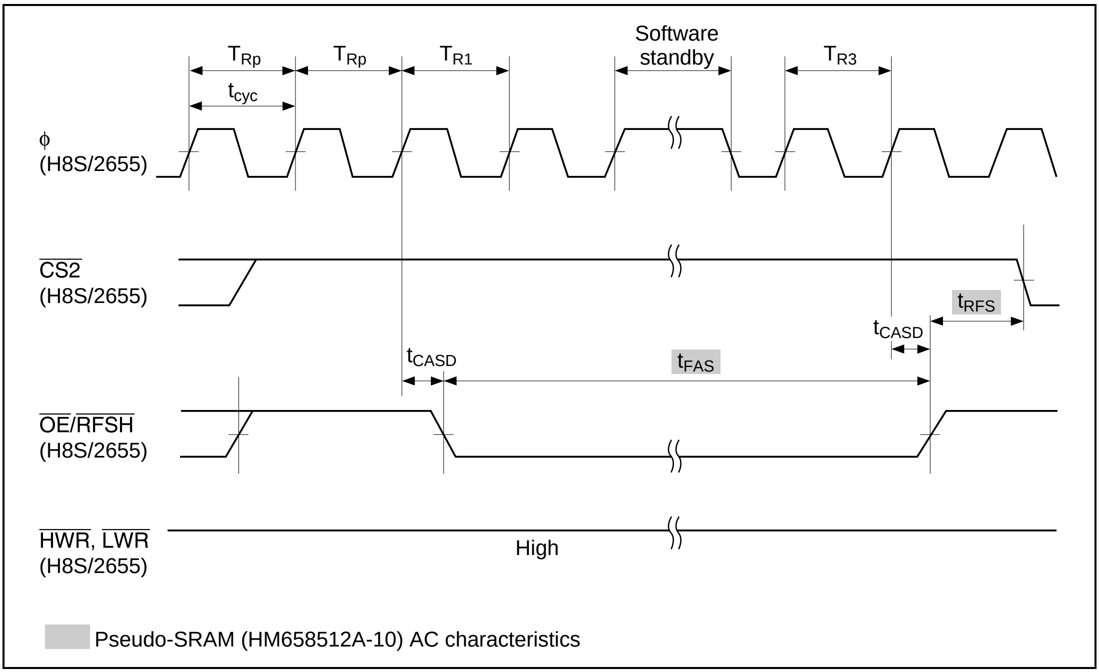


Figure 3.4.1 (f) Self-Refresh Timing Chart

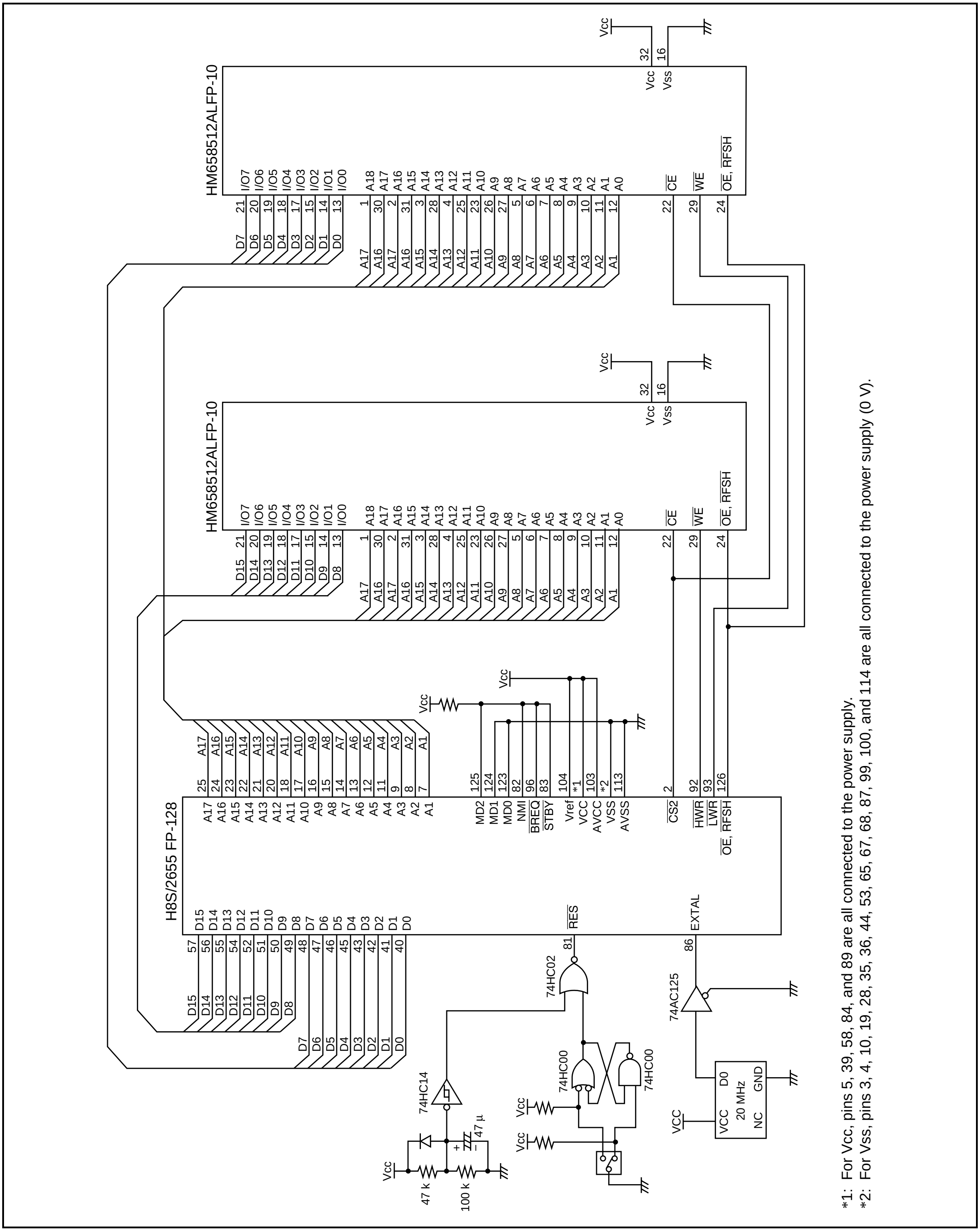


Figure 3.4.1 (g) HM658512A-12 Interface

3.14 Burst ROM (HN27C4000G-15) Interface Using 16-Bit Bus Mode

EPROM (HN27C4000G-15) Interface	MCU: H8S/2655	Functions Used: Mode 4 (16-Bit Bus Mode)

Specifications

1. Figure 3.5.1 (a) shows an example of the connection between an H8S/2655 and ×16-bit configuration burst ROM (HN27C4000G-15). The H8S/2655 is set to mode 4 16-bit bus mode, and the burst ROM is allocated to area 0.

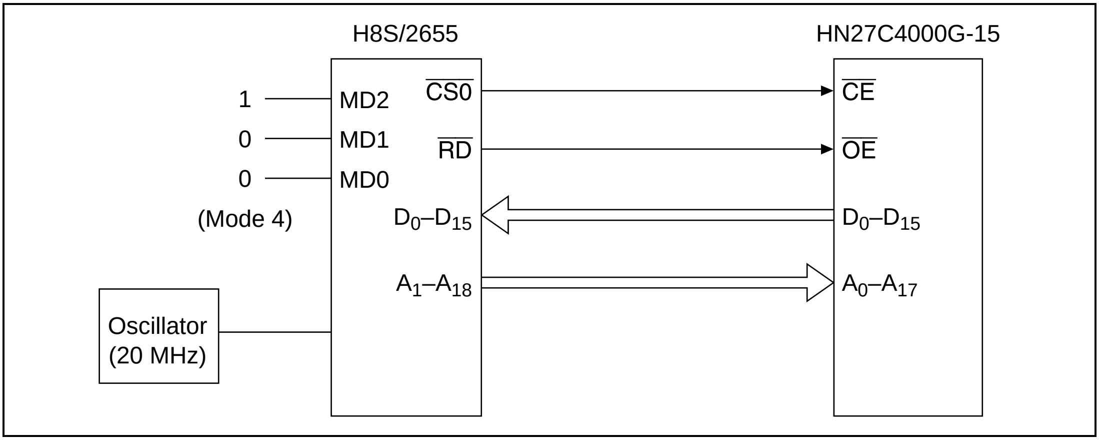


Figure 3.5.1 (a) Example of Connection between H8S/2655 and Burst ROM

2. Figure 3.5.1 (b) shows the memory map. When the 16-Mbyte address space is divided into areas in 2-Mbyte units, the burst ROM area is H'00 0000–H'07 FFFF.

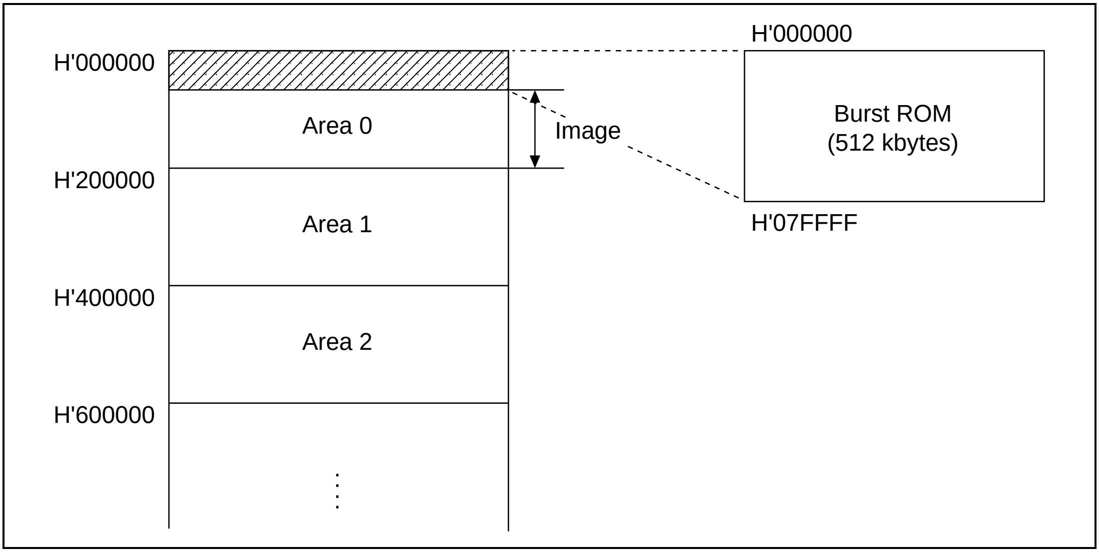


Figure 3.5.1 (b) Memory Map

3. Table 3.5.1 (a) shows the bus controller settings.

Table 3.5.1 (a) Bus Controller Settings

Name	Abbrev.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Setting
Bus width control register	ABWCR	ABW7 *	ABW6 *	ABW5 *	ABW4 *	ABW3 *	ABW2 *	ABW1 *	ABW0 0	Area 0: 16-bit access space
Access state control register	ASTCR	AST7 *	AST6 *	AST5 *	AST4 *	AST3 *	AST2 *	AST1 0	AST0 0	Full access states: 3
Wait control register H	WCRH	W71 *	W70 *	W61 *	W60 *	W51 *	W50 *	W41 *	W40 *	—
Wait control register L	WCRL	W31 *	W30 *	W21 *	W20 *	W11 *	W10 *	W01 0	W00 1	Area 0: 1 program wait inserted
Bus control register H	BCRH	ICIS1 *	ICIS0 *	BRSTRM 1	BRSTS1 1	BRSTS0 0	RMTS2 *	RMTS1 *	RMTS0 *	Burst ROM selection: Enabled Burst cycles: 2 states Burst words: Max. 4
Bus control register L	BCRL	BRLE *	BREQOE *	EAE *	LCASS *	DDS *	ASS 1	WDBE *	WAITE *	Area partition unit: 2 Mbytes (16 Mbytes)
Memory control register	MCR	TPC *	BE *	RCDM *	CW2 *	MXC1 *	MXC0 *	RLW1 *	RLW0 *	—
DRAM control register	DRAMCR	RFSHE *	RCW *	RMODE *	CMF *	CMIE *	CKS2 *	CKS1 *	CKS0 *	—
Refresh time constant register	RTCOR	*	*	*	*	*	*	*	*	—

*: Don’t care

Operation

The calculations used to check whether the AC characteristics are satisfied in burst ROM access are shown below. The t_{cyc} value, unspecified min value, and unspecified max value are as follows.

- t_{cyc}: 50 ns (20 MHz oscillator (= ϕ))
- Unspecified min value: 0 ns
- Unspecified max value: min value

In the times obtained based on ϕ, the reference timing is shown in [ ].

For the timing values, see 3. AC Characteristics below.

1. Read Access

   Figure 3.5.1 (c) shows the burst ROM read timing chart.

   Confirm that the following AC characteristics are satisfied.

Item		Symbol
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}

a. H8S/2655 t_{RDS}

i. When address is critical

- Setup time calculation [$T_{1\text{-}1}$ cycle rise]

  $4\ t_{cyc} - t_{AD\,(max)} - t_{ACC\,(max)} = 30\text{ ns} \geq 15\text{ ns }(t_{RDS})$

ii. When CS is critical

- Setup time calculation [$T_{1\text{-}1}$ cycle rise]

  $3\ t_{cyc} - t_{CSD1\,(max)} - t_{CE\,(max)} = 30\text{ ns} \geq 15\text{ ns }(t_{RDS})$

iii. When RD is critical

- Setup time calculation [$T_{1\text{-}1}$ cycle rise]

  $3.5\ t_{cyc} - t_{RSD1\,(max)} - t_{OE\,(max)} = 85\text{ ns} \geq 15\text{ ns }(t_{RDS})$

b. H8S/2655 t_{RDH}

i. Hold time calculation [$T_{3\text{-}1}$ cycle fall]

$\{t_{AH\,(max)} - (0.5\ t_{cyc} - t_{ASD\,(max)})\} + t_{OH\,(min)} = 15\text{ ns} \geq 0\text{ ns }(t_{RDH})$

2. Burst Access Mode

Confirm that the following AC characteristics are satisfied. See figure 3.5.1 (c).

Item		Symbol
H8S/2655	Read data setup time	t_{RDS}
	Read data hold time	t_{RDH}

a. H8S/2655 t_{RDS}

- Setup time calculation [$T_{1\text{-}2}$ cycle rise]

  $2\ t_{cyc} - t_{AD\,(max)} - t_{ACC\,(max)} = 20\ ns \geq 15\ ns\ (t_{RDS})$

b. H8S/2655 t_{RDH}

- Hold time calculation [$T_{2\text{-}2}$ cycle fall]

  $\{t_{AH\,(max)} - (0.5\ t_{cyc} - t_{ASD\,(max)})\} + t_{OH\,(min)} = 15\ ns \geq 0\ ns\ (t_{RDH})$

3. AC Characteristics

a. H8S/2655

Item	Symbol	Min	Max	Unit
Address delay time	t_{AD}	—	20	ns
Address hold time	t_{AH}	$0.5 \times t_{cyc} - 10$	—	ns
$\overline{CS}$ delay time 1	t_{CSD1}	—	20	ns
$\overline{AS}$ delay time	t_{ASD}	—	20	ns
$\overline{RD}$ delay time 1	t_{RSD1}	—	20	ns
$\overline{RD}$ delay time 2	t_{RSD2}	—	20	ns
Read data setup time	t_{RDS}	15	—	ns
Read data hold time	t_{RDH}	0	—	ns

b. HN27C4000G-15

Item	Symbol	Min	Max	Unit
Access Time	t_{ACC}	—	150	ns
$\overline{CE}$-output delay time	t_{CE}	—	150	ns
$\overline{OE}$-output delay time	t_{OE}	—	70	ns
Burst access time	t_{BAC}	—	60	ns
Data output hold time	t_{OH}	5	—	ns

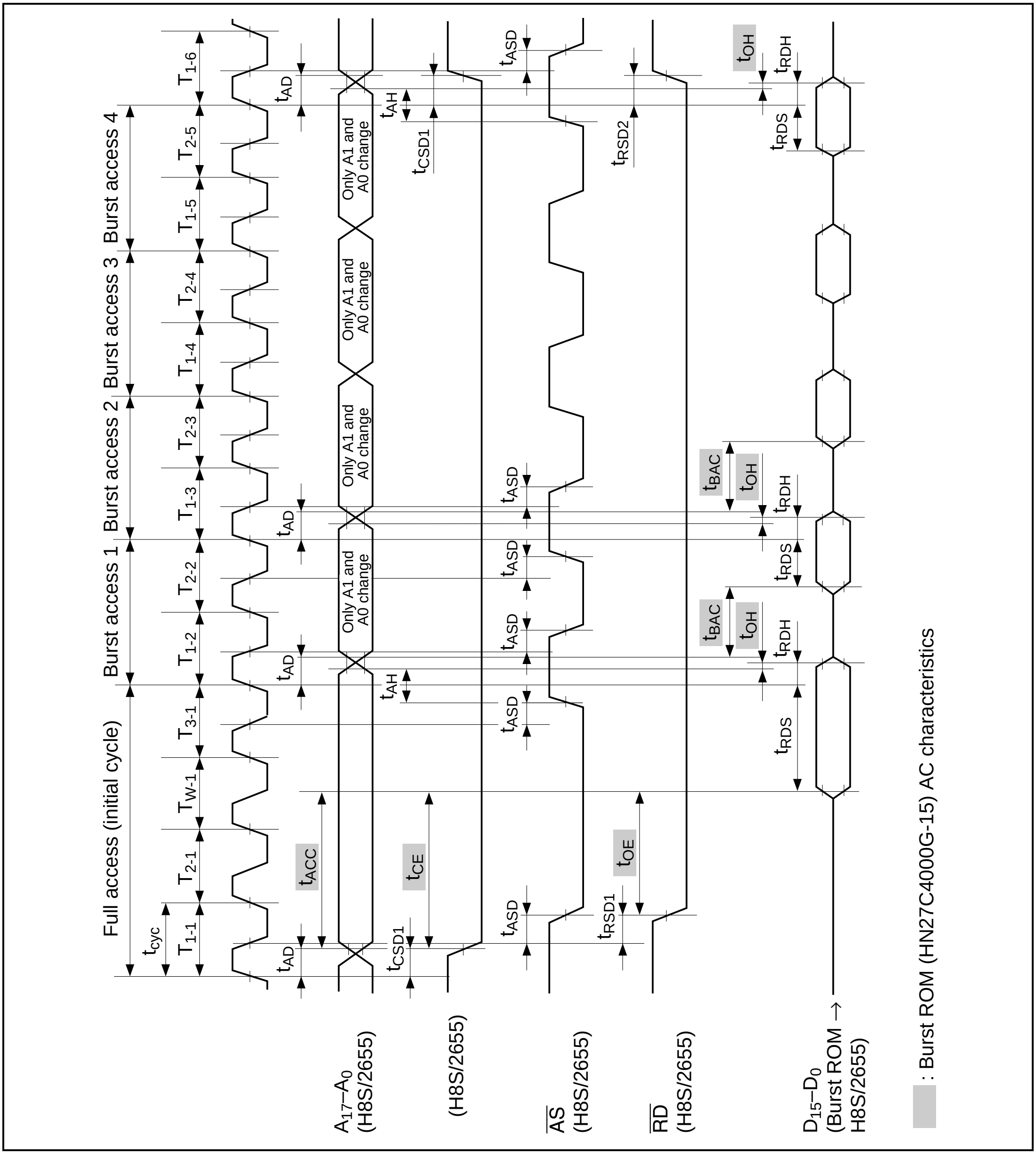


Figure 3.5.1 (c) Burst ROM Read Timing Chart

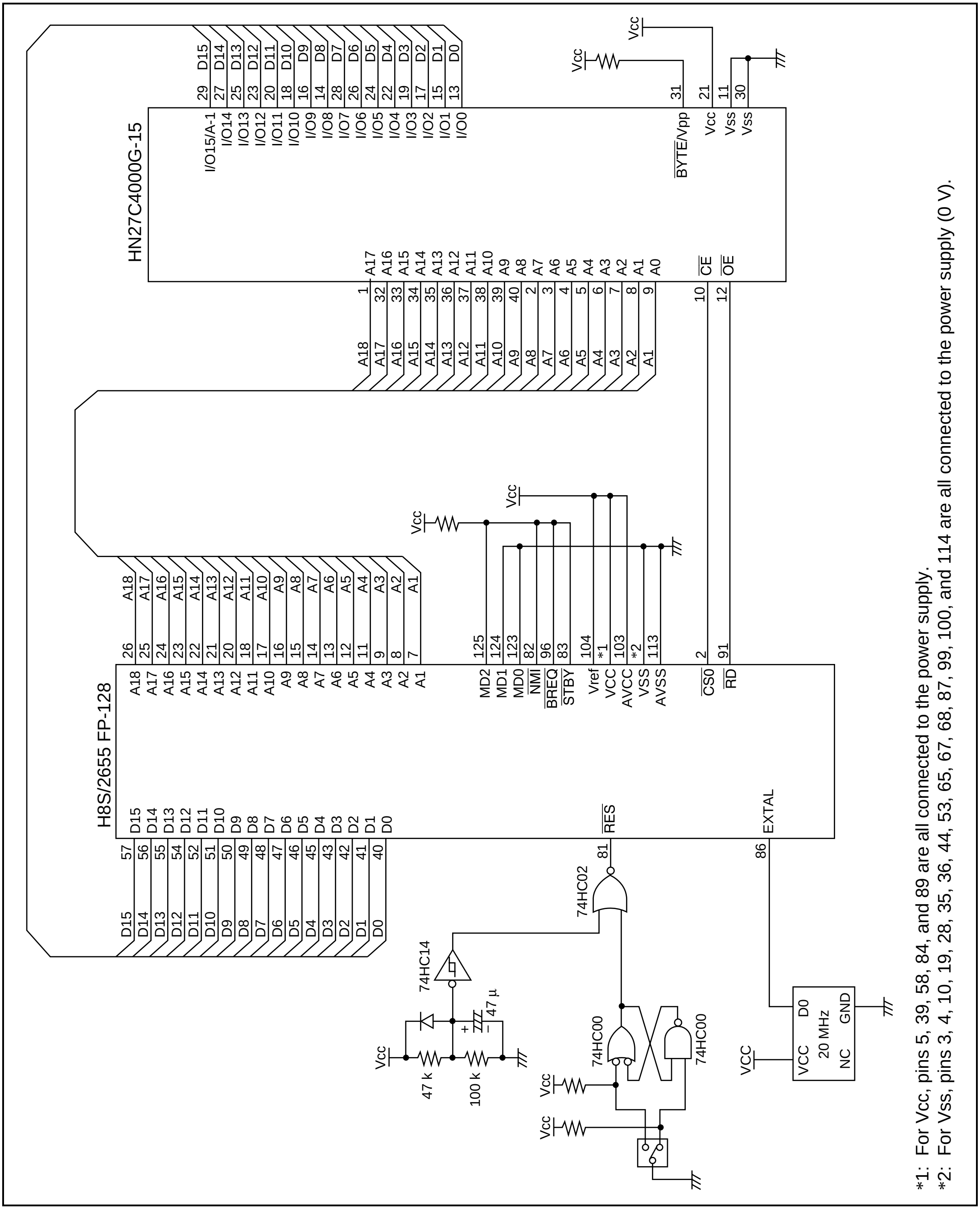


Figure 3.5.1 (d) HN27C4000G-15 Interface

3.15 Flash Memory (HN29WB800T-12) Interface Using 16-Bit Bus Mode

Flash Memory (HN29WB800T-12) Interface	MCU: H8S/2655	Functions Used: Mode 4

Specifications

1. Figure 3.6.1 (a) shows a block diagram of the connection between an H8S/2655 and an HN29WB800T-12 using mode 4 (16-Mbyte access, 16-bit data bus).

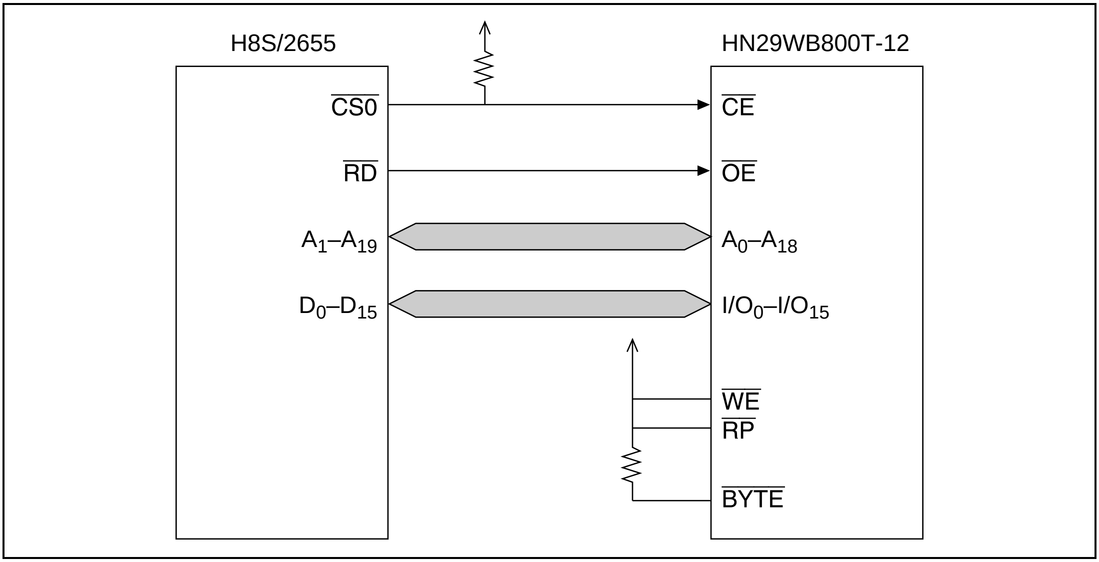


Figure 3.6.1 (a) Block Diagram of Connection between H8S/2655 and HN29WB800T-12

2. Figure 3.6.1 (b) shows the flash memory area designation.

   Area 0 (H'00 0000–H'1F FFFF) in the H8S/2655's external address space (16-Mbyte memory space) is designated as flash memory (HN29WB800T-12).

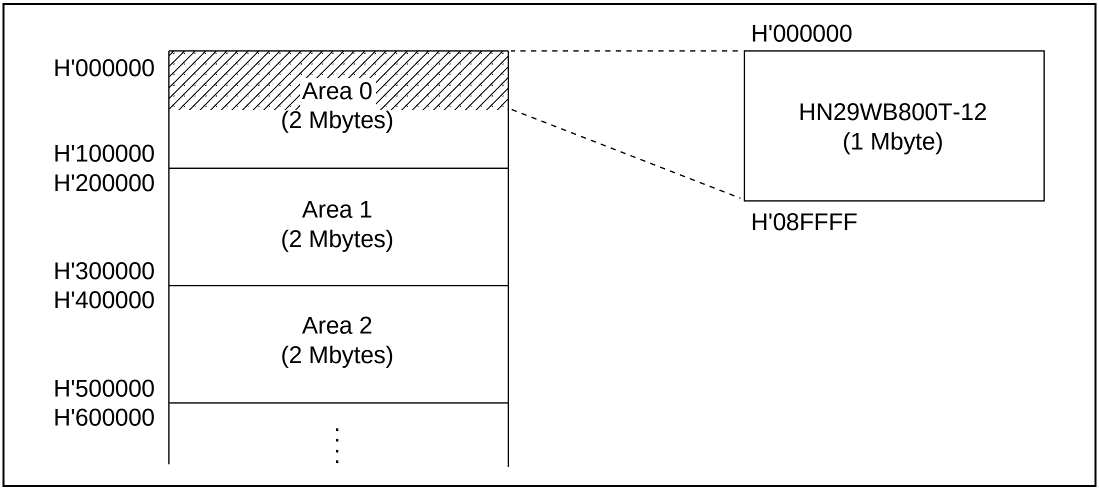


Figure 3.6.1 (b) Designated Flash Memory Area (Memory Map)

Operation

1. Read Timing

   Figure 3.6.1 (c) shows the read timing chart. Check whether the read data hold time (t_{OH}), and data access times (t_{ACC}, t_{CE}, t_{OE}) are satisfied.

   a. Data hold time

   $$t_{OH} = t_{RDH\,(min)} - t_{RSD2\,(max)}$$
   $$= -20\text{ ns} \le 0\text{ ns (memory, min)}$$

   b. Data access time from address

   $$t_{ACC} = t_{ACC5\,(max)}$$
   $$= 125\text{ ns} \ge 120\text{ ns (memory, max)}$$

   c. Data access time from $\overline{CS}$ ($\overline{CE}$)

   $$t_{CE} = t_{ACC5\,(max)}$$
   $$= 125\text{ ns} \ge 120\text{ ns (memory, max)}$$

   d. Data access time from $\overline{RD}$ ($\overline{OE}$)

   $$t_{OE} = t_{ACC4\,(max)}$$
   $$= 100\text{ ns} \ge 60\text{ ns (memory, max)}$$

   As there is no problem with the above four timing conditions, the H8S/2655 performs 3-state-access, no-wait interfacing.

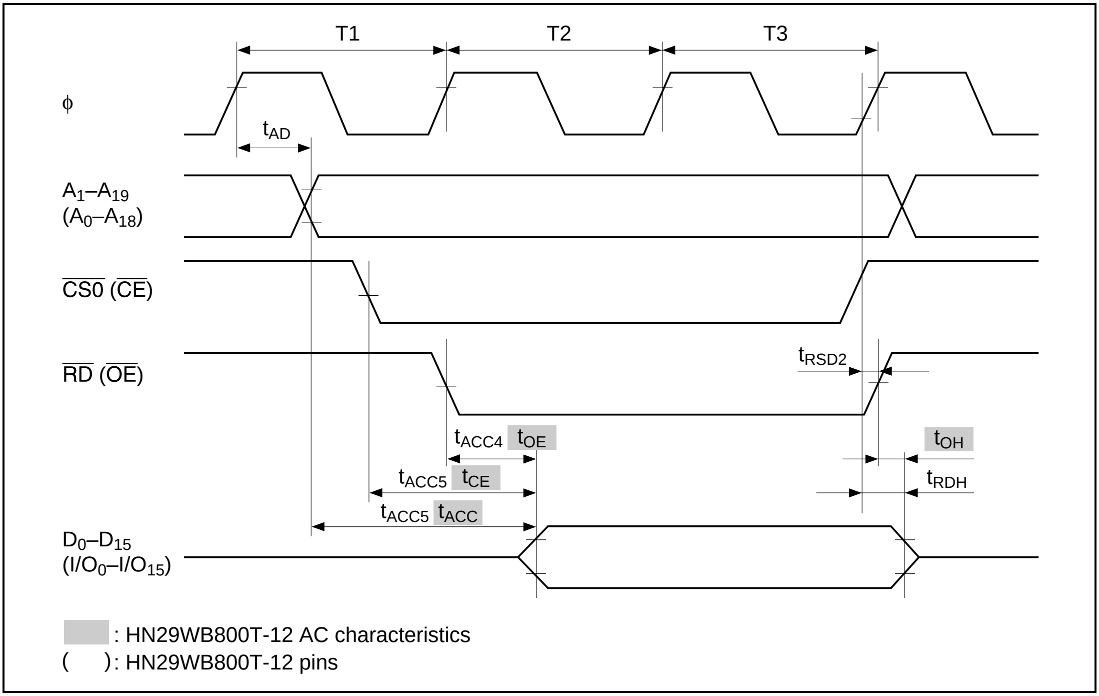


Figure 3.6.1 (c) Read Timing Chart

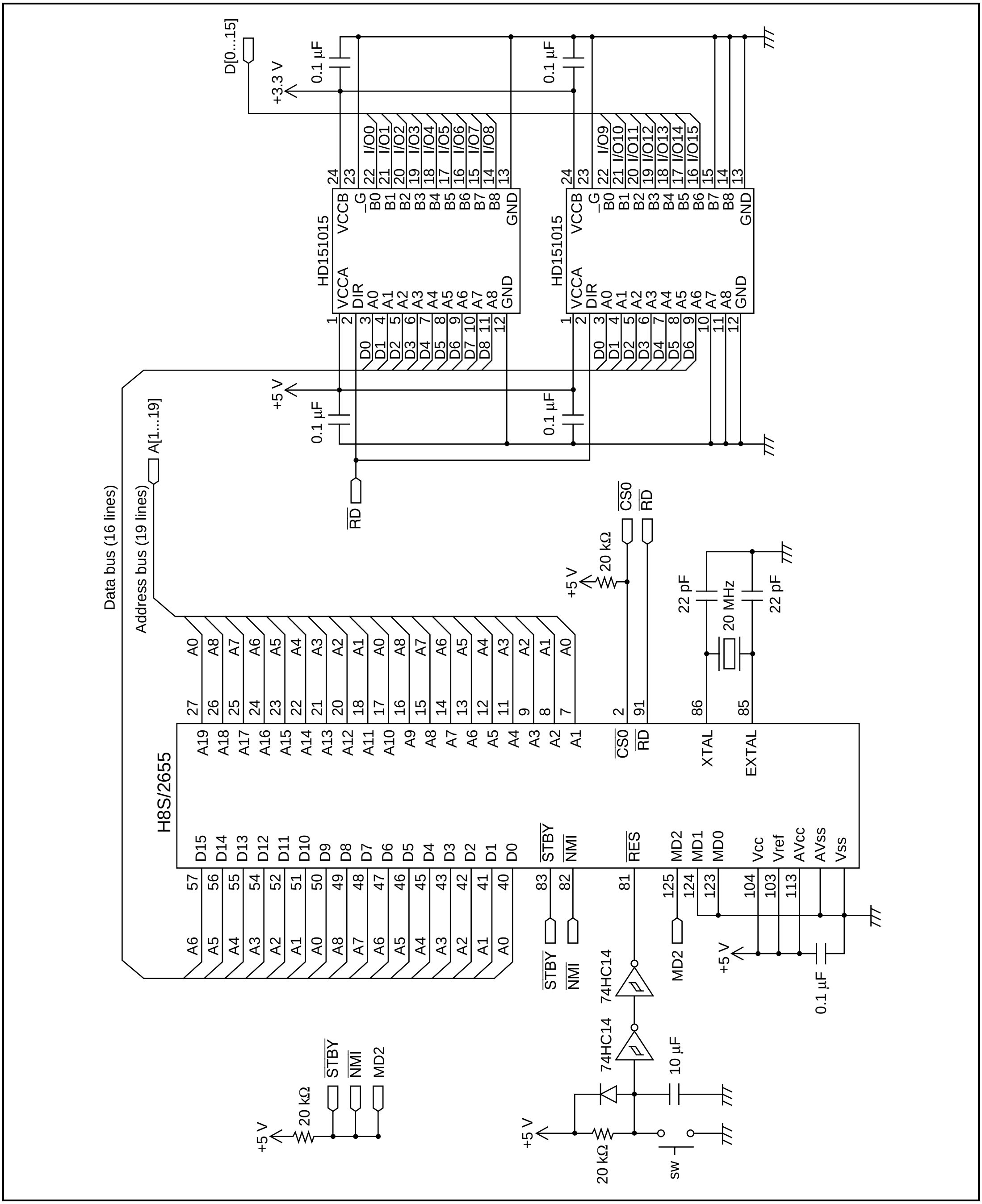


Figure 3.6.1 (d) HN29WB800T-12 Interface 1

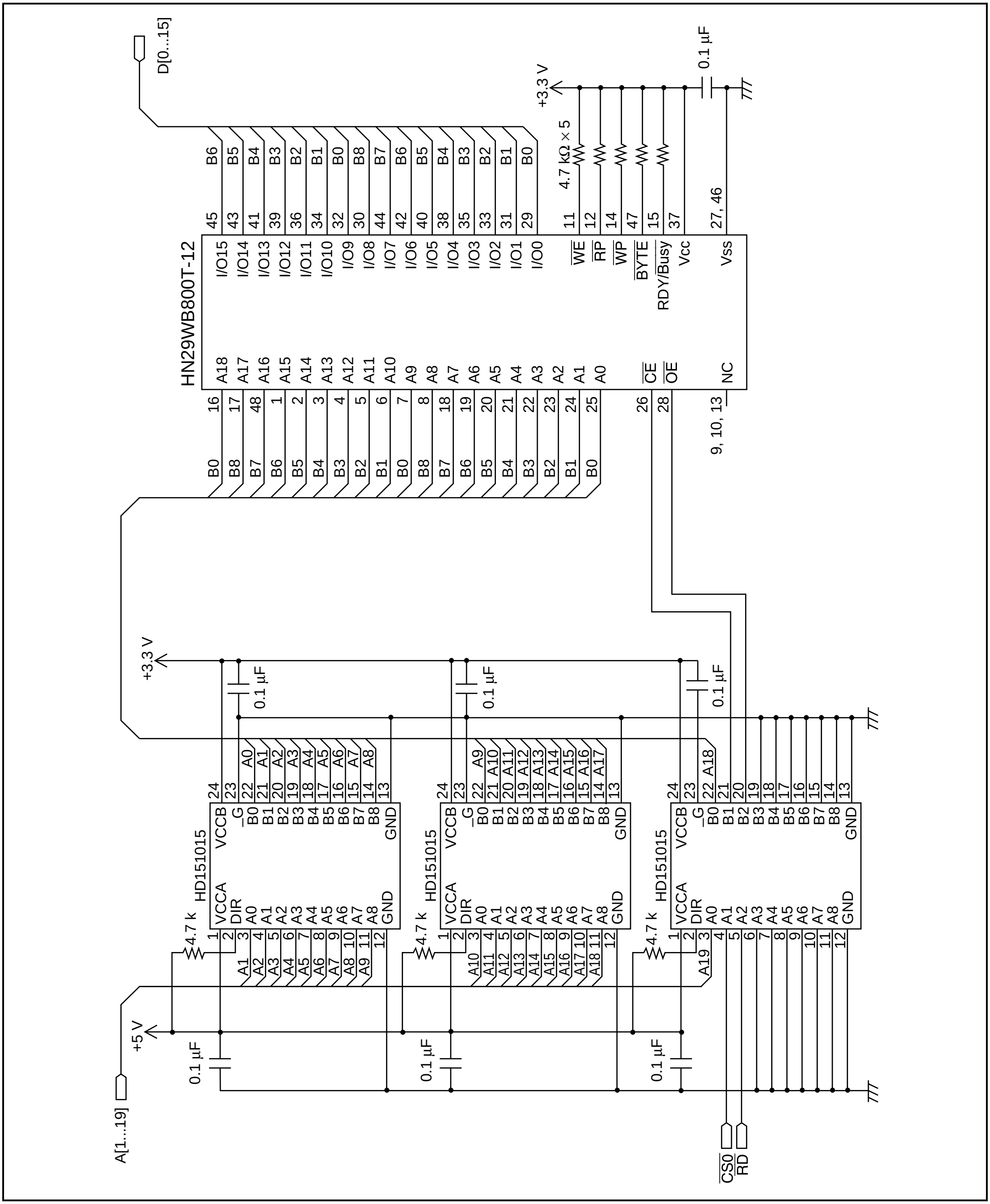


Figure 3.6.1 (e) HN29WB800T-12 Interface 2

H8S/2655 Application Note

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