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H8S/2200 Series

Using Interrupt Controller in Mode 0/2

Introduction

This application note demonstrates how to set interrupt control mode, interrupt priorities, and the interrupt-latching condition.

Target Device

H8S/2215

Contents

1. Overview

This sample task demonstrates how to set interrupt control mode, interrupt priorities, and the interrupt-latching condition.

2. Configuration

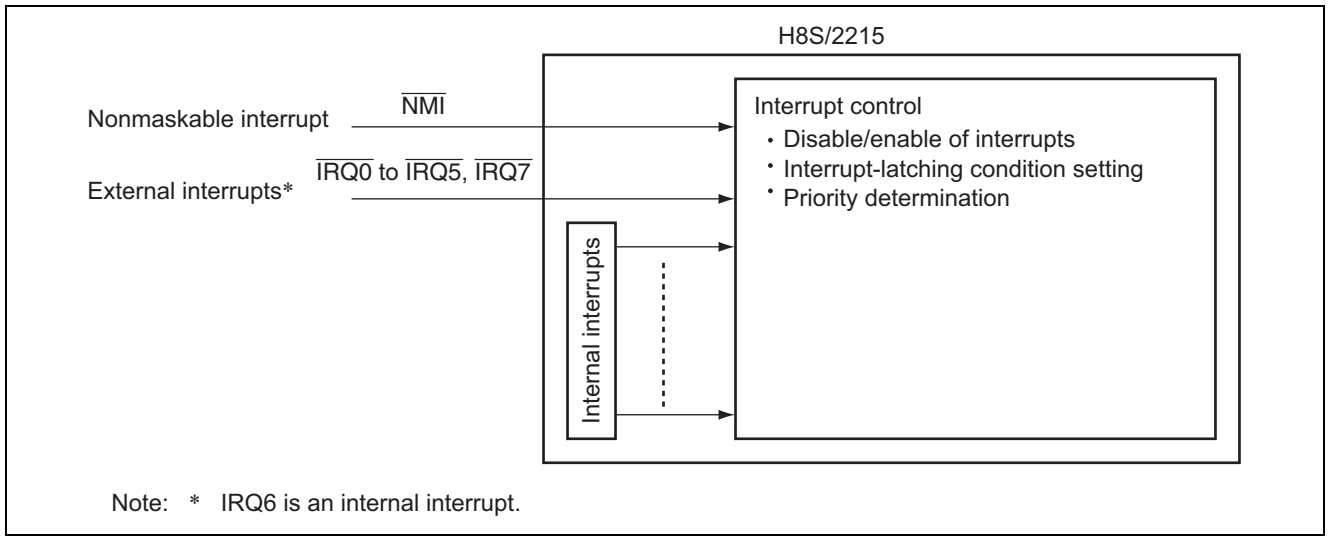


Figure 1 Interrupt Processing

Table 1 Pin Configuration

Signal Name	Description
NMI	Nonmaskable external interrupt pin The rising or falling edge can be selected.
IRQ0 to IRQ5 and IRQ7	Seven maskable external interrupt pins The rising edge, falling edge, both edges or low-level sense can be selected independently.

3. Sample Programs

3.1 Functions

The sample programs provide subroutines for setting registers often used in interrupt processing.

1. Sets interrupt control mode 0 or 2 and globally enables/disables interrupts.
2. Sets interrupt priority for interrupt control mode 2.
3. Sets the IRQ interrupt-latching condition and enables/disables IRQ interrupts.
4. Sets the NMI interrupt-latching condition.

3.2 Program Incorporation

1. Incorporate sample program 4-A: #define definitions.
2. Incorporate sample program 4-B: common variable definitions.
3. Incorporate sample program 4-C: prototype declarations.
4. Incorporate sample program 4-D: common subroutines.

3.3 Modifications to Sample Programs

Without modifications to the sample program, the system may not run. Modifications must be made according to your program and system environment.

1. The sample programs can be used without further changes if you use the I/O register structure definition file, which is available free of charge from the following Renesas web site:
   http://www.renesas.com
   When you create structure definitions by yourself, modify the I/O register structures used in the sample program as appropriate.

3.4 Using the Sample Programs

Subroutines for setting registers often used in interrupt processing are provided in the sample programs. Below are the descriptions of the subroutines.

1. Sets interrupt control mode 0 or 2.

- Subroutine name: **void** com_int_mode_control **(int** mode **, int** control **)**

Argument	Setting
mode	Specifies interrupt control mode. INT_MODE_0 (0): Interrupt control mode 0 INT_MODE_2 (2): Interrupt control mode 2 Note: Interrupt control mode 1 does not exist.
control	Globally enables/disables interrupts. In interrupt control mode 0: INT_DISABLE (0): Interrupts are globally disabled. - However, the NMI interrupt cannot be disabled even if INT_DISABLE is set. INT_ENABLE (1): Interrupts are globally enabled. In interrupt control mode 2: INT_MASK_LEVEL_0 to INT_MASK_LEVEL_7 (0 to 7): Mask level - When INT_MASK_LEVEL_7 is set, all interrupts other than NMI are disabled.

Note: Before this subroutine is executed, interrupt control mode 0 is selected and interrupts are globally disabled, which are the microcomputer's initial settings.

2. Sets interrupt priority for interrupt control mode 2.

- Subroutine name: **void** com_int_set_priority **(void)**
  Before this subroutine is called, priorities (levels 1 to 7) of individual interrupts should be set in the common variable table int_pri_tbl. '1' sets the lowest priority and '7' sets the highest. When 0 is set for the priority level, the corresponding interrupt is disabled.
  This subroutine and settings in the table are only valid when interrupt control mode 2 has been set by the subroutine com_int_mode_control.

Int_pri_tbl	Name	Applicable Interrupts
[0]	INT_IRQ0	IRQ0
[1]	INT_IRQ1	IRQ1
[2]	INT_IRQ2_3	IRQ2 and IRQ3 (Priority when both interrupts coincide: IRQ2 > IRQ3)
[3]	INT_IRQ4_5	IRQ4 and IRQ5 (Priority when both interrupts coincide: IRQ4 > IRQ5)
[4]	INT_IRQ6_7	IRQ6 and IRQ7 (Priority when both interrupts coincide: IRQ6 > IRQ7)
[5]	INT_SWDTEND	DTC software-activation interrupt (SWDTEND)
[6]	INT_WOVI	WDT interval timer interrupt
[7]	INT_ADI	AD conversion end interrupt
[8]	INT_TPU0	TGI0A, TGI0B, TGI0C, TGI0D and TCI0V interrupts of the TPU0 (Priority when multiple interrupts coincide: TGI0A > TGI0B > TGI0C > TGI0D > TCI0V)
[9]	INT_TPU1	TGI1A, TGI1B, TCI1V and TCI1U interrupts of the TPU1 (Priority when multiple interrupts coincide: TGI1A > TGI1B > TCI1V > TCI1U)
[10]	INT_TPU2	TGI2A, TGI2B, TCI2V and TCI2U interrupts of the TPU2 (Priority when multiple interrupts coincide: TGI2A > TGI2B > TCI2V > TCI2U)
[11]	INT_TMR0	CMIA0, CMIB0 and OVI0 interrupts of the 8-bit timer 0 (Priority when multiple interrupts coincide: CMIA0 > CMIB0 > OVI0)
[12]	INT_TMR1	CMIA1, CMIB1 and OVI1 interrupts of the 8-bit timer 1 (Priority when multiple interrupts coincide: CMIA1 > CMIB1 > OVI1)
[13]	INT_DMAC	DEND0A, DEND0B, DEND1A and DEND1B interrupts of the DMAC (Priority when multiple interrupts coincide: DEND0A > DEND0B > DEND1A > DEND1B)
[14]	INT_SCI0	ERI0, RXI0, TXI0 and TEI0 interrupts of the SCI0 (Priority when multiple interrupts coincide: ERI0 > RXI0 > TXI0 > TEI0)
[15]	INT_SCI1	ERI1, RXI1, TXI1 and TEI1 interrupts of the SCI1 (Priority when multiple interrupts coincide: ERI1 > RXI1 > TXI1 > TEI1)
[16]	INT_SCI2	ERI2, RXI2, TXI2 and TEI2 interrupts of the SCI2 (Priority when multiple interrupts coincide: ERI2 > RXI2 > TXI2 > TEI2)
[17]	INT_USB	EXIRQ0 and EXIRQ1 interrupts of the USB (Priority when both interrupts coincide: EXIRQ0 > EXIRQ1)

Note: Before this subroutine is executed, level 7 is set for all interrupts as the microcomputer's initial settings.

3. Sets the IRQ interrupt-latching condition and enables/disables IRQ interrupts.

- Subroutine name: **void** com_irq_control **(int** kind **, int** method **, int** control**)**

Argument	Setting
kind	Specifies an IRQ interrupt. INT_IRQ0 to INT_IRQ7 (0 to 7): IRQ0 to IRQ7
method	Specifies the interrupt-latching condition. INT_LOW_LEVEL (0): An interrupt is generated with low-level sense INT_LOW_EDGE_TRG (1): An interrupt is generated at the falling edge INT_HIGH_EDGE_TRG (2): An interrupt is generated at the rising edge INT_HIGH_LOW_EDGE_TRG (3): An interrupt is generated at both edges
control	Globally enables/disables interrupts. INT_DISABLE (0): Interrupts are disabled. The NMI interrupt cannot be disabled even if INT_DISABLE is set. INT_ENABLE (1): Interrupts are enabled.

Note: Before this subroutine is executed, all IRQ interrupts are disabled and low-level sense is selected as the mode of interrupt latch, which are the microcomputer's initial settings.

4. Sets the NMI interrupt-latching condition.

- Subroutine name: **void** com_nmi_control **(int** method **)**

Argument	Setting
method	Specifies the interrupt-latching condition. INT_LOW_EDGE_TRG (1): An interrupt is generated at the falling edge INT_HIGH_EDGE_TRG (2): An interrupt is generated at the rising edge

Note: Before this subroutine is executed, the rising edge is selected as the microcomputer's initial setting.

3.5 Description of Operation

3.5.1 Interrupt Control Mode 0

In interrupt control mode 0, interrupt requests other than NMI are masked by the I bit in CCR of the CPU. This setting is easily made by using the sample program routine com_int_mode_control.

The priority level for each interrupt is fixed. When multiple interrupts are generated at a time, the processing of lower priority interrupts is suspended until the higher priority interrupts have been processed. The priority of each interrupt is shown in table 3.

When an interrupt is generated, the microcomputer starts the interrupt processing from the address written in the vector address corresponding to the interrupt. During the interrupt processing, the I bit in CCR is set to 1 to disable all interrupts other than NMI. Therefore, in interrupt control mode 0, any interrupt other than NMI cannot be processed while an interrupt is processed.

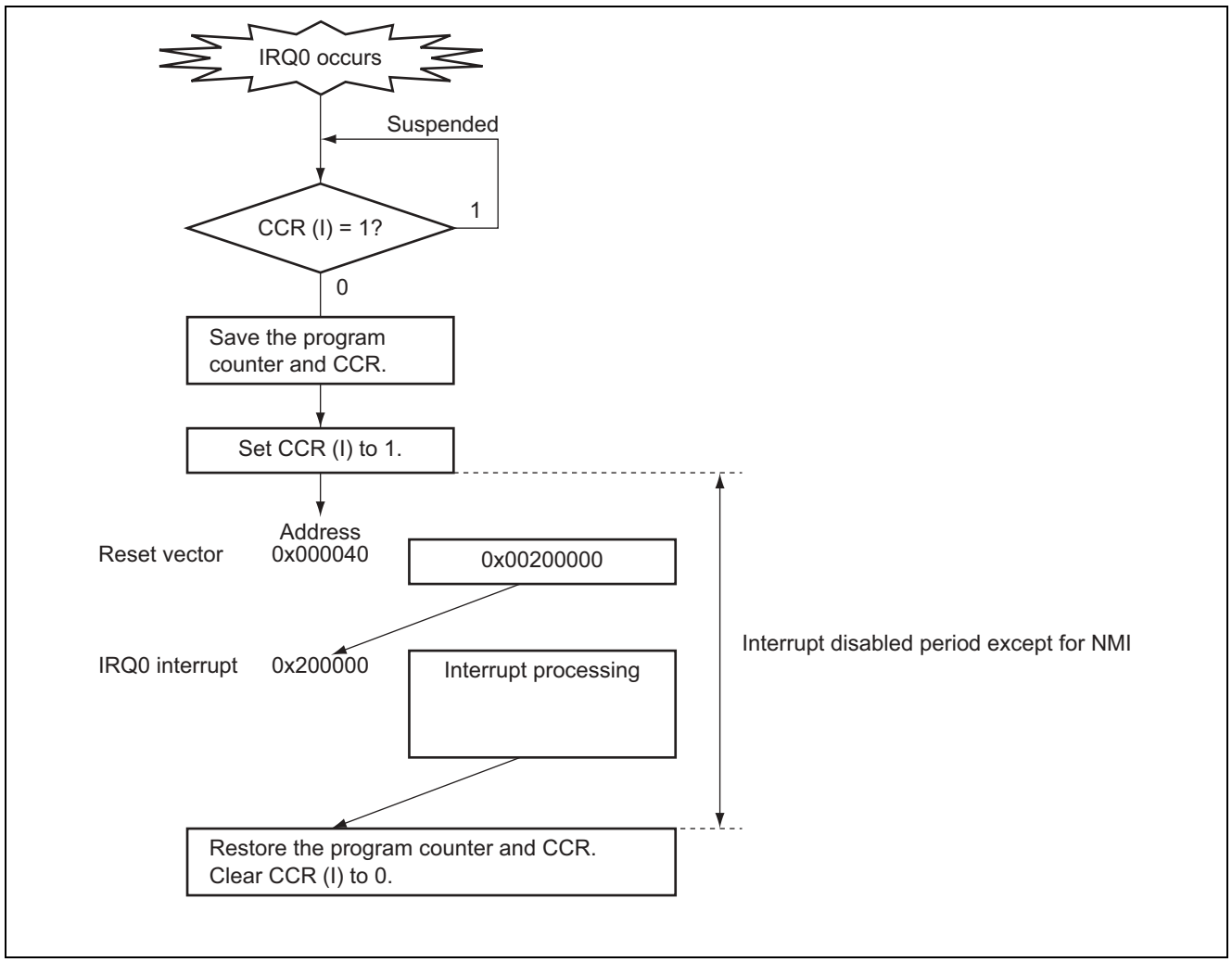


Figure 2 Example of Interrupt Processing (IRQ0 Interrupt)

3.5.2 Interrupt Control Mode 2

In interrupt control mode 2, interrupt requests other than NMI can be masked with eight masking levels by comparing the IPR setting with the mask level set with the I2 to I0 bits of the EXR register of the CPU. This masking is easily set by using subroutine com_int_mode_control provided in the sample program.

The priority of each interrupt is set using the IPR register. IPR can be set for each interrupt source. Correspondences between IPR settings and interrupts are shown in table 3. IPR interrupt priority setting is easily made by using the sample program subroutine com_int_set_priority. When multiple interrupts are generated at a time, the processing of lower priority interrupts is suspended until the higher priority interrupts have been processed.

When an interrupt is generated, the microcomputer compares the interrupt level set in the IPR register that corresponds to the interrupt with the mask level set in the EXR (I2 to I0) register. If the IPR interrupt level is higher than the mask level, the interrupt processing is started. If it is lower than the mask level, the processing for that interrupt is suspended.

The interrupt processing starts with the address written in the vector address corresponding to the interrupt. During the interrupt processing, the mask level in EXR (I2 to I0) is rewritten with the level of the interrupt being processed and another interrupt whose level is lower than that of the interrupt being processed (lower priority interrupt) is not accepted. On the other hand, another interrupt whose level is higher than that of the interrupt being processed (higher priority interrupt) can be accepted. Therefore, in interrupt control mode 2, another interrupt processing may be performed while an interrupt is processed. In the case of NMI, the mask level is fixed to 7 and another interrupt is not accepted during NMI interrupt processing.

Figure 2 shows the above-described processing flow. Table 2 shows correspondence between the mask levels and acceptable interrupt levels.

Table 2 Mask Levels and Acceptable Interrupt Levels

EXR (I2 to I0) Mask Level	Acceptable Interrupt Level
0	1 to 7
1	2 to 7
2	3 to 7
3	4 to 7
4	5 to 7
5	6 to 7
6	7
7	None

When the mask level is set to 7, all interrupts other than NMI can be disabled.

When interrupt level 0 is set with IPR, interrupts can be disabled for each interrupt source.

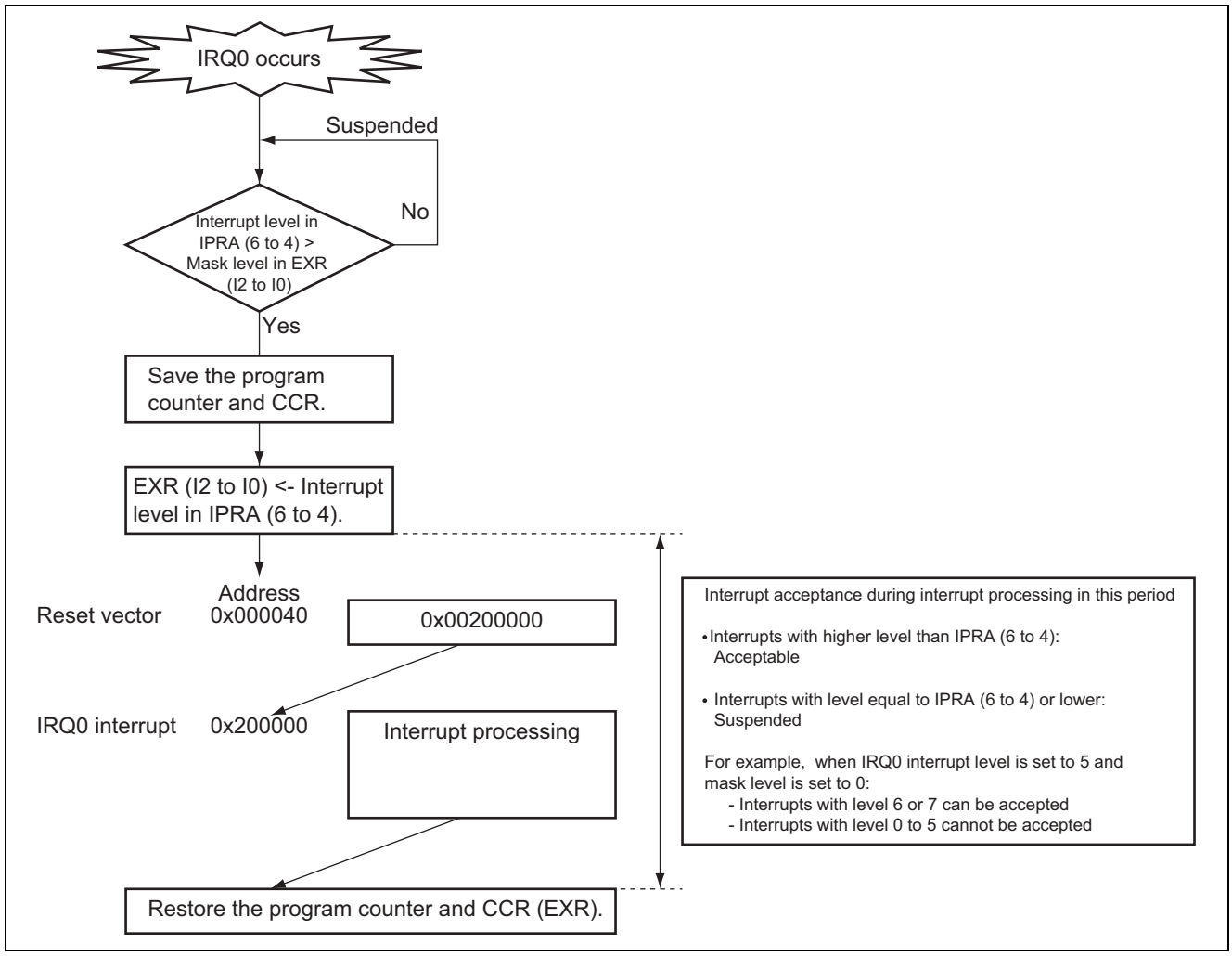


Figure 3 Example of Processing in Interrupt Control Mode 2 (IRQ0 Interrupt)

Table 3 Interrupt Priority

Interrupt Source	Name	Vector Number	Vector Address* Advanced Mode	IPR	Priority
External pin	NMI	7	H'001C		High
	IRQ0	16	H'0040	IPRA6 to IPRA4	
	IRQ1	17	H'0044	IPRA2 to IPRA0	
	IRQ2	18	H'0048	IPRB6 to IPRB4	
	IRQ3	19	H'004C		
	IRQ4	20	H'0050	IPRB2 to IPRB0	
	IRQ5	21	H'0054		
USB	IRQ6	22	H'0058	IPRC6 to IPRC4	
External pin	IRQ7	23	H'005C	IPRC6 to IPRC4	
DTC	SWDTEND	24	H'0060	IPRC2 to IPRC0	
Watchdog timer	WOVI	25	H'0064	IPRD6 to IPRD4	
A/D	ADI	28	H'0070	IPRE2 to IPRE0	
TPU channel 0	TGI0A	32	H'0080	IPRF6 to IPRF4	
	TGI0B	33	H'0084		
	TGI0C	34	H'0088		
	TGI0D	35	H'008C		
	TCI0V	36	H'0090		
TPU channel 1	TGI1A	40	H'00A0	IPRF2 to IPRF0	
	TGI1B	41	H'00A4		
	TCI1V	42	H'00A8		
	TCI1U	43	H'00AC		
TPU channel 2	TGI2A	44	H'00B0	IPRG6 to IPRG4	
	TGI2B	45	H'00B4		
	TCI2V	46	H'00B8		
	TCI2U	47	H'00BC		
8-bit timer channel 0	CMIA0 (Compare-match A)	64	H'0100	IPRI6 to IPRI4	
	CMIB0 (Compare-match B)	65	H'0104		
	OVI0 (Overflow)	66	H'0108		
8-bit timer channel 1	CMIA1 (Compare-match A)	68	H'0110	IPRI2 to IPRI0	
	CMIB1 (Compare-match B)	69	H'0114		
	OVI1 (Overflow)	70	H'0118		
DMAC	DEND0A	72	H'0120	IPRJ6 to IPRJ4	
	DEND0B	73	H'0124		
	DEND1A	74	H'0128		
	DEND1B	75	H'012C		Low

Interrupt Source	Name	Vector Number	Vector Address* Advanced Mode	IPR	Priority
SCI channel 0	ERI0	80	H'0140	IPRJ2 to IPRJ0	High
	RXI0	81	H'0144		
	TXI0	82	H'0148		
	TEI0	83	H'014C		
SCI channel 1	ERI1	84	H'0150	IPRK6 to IPRK4	
	RXI1	85	H'0154		
	TXI1	86	H'0158		
	TEI1	87	H'015C		
SCI channel 2	ERI2	88	H'0160	IPRK2 to IPRK0	
	RXI2	89	H'0164		
	TXI2	90	H'0168		
	TEI2	91	H'016C		
USB	EXIRQ0	104	H'01A0	IPRM6 to IPRM4	
	EXIRQ1	105	H'01A4		Low

Note: The vector address indicates lower 16 bits of the start address.

3.5.3 NMI Interrupt

The nonmaskable interrupt request NMI is an external interrupt request with the highest priority. This is accepted at any time regardless of interrupt control mode or CPU interrupt mask bit status. The rising or falling edge can be selected for the NMI pin to generate an interrupt request with the NMIEG bit in SYSCR. The NMI interrupt setting is easily made by using the sample program routine com_nmi_control.

3.5.4 IRQ Interrupts

IRQ7 and IRQ5 to IRQ0 interrupts generate interrupt requests by input signal on each pin. Though IRQ6 is an internal interrupt of the USB, the function is the same as other IRQ pins. IRQ interrupts have the following features:

- Low level, falling edge, rising edge or both edges can be selected with ISCR for generation of interrupt requests.
- $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ interrupt requests can be masked with the IER register.
- Interrupt priorities can be set with IPR registers.

The above settings can be easily made by using the sample program routines com_irq_control and com_int_set_priority.

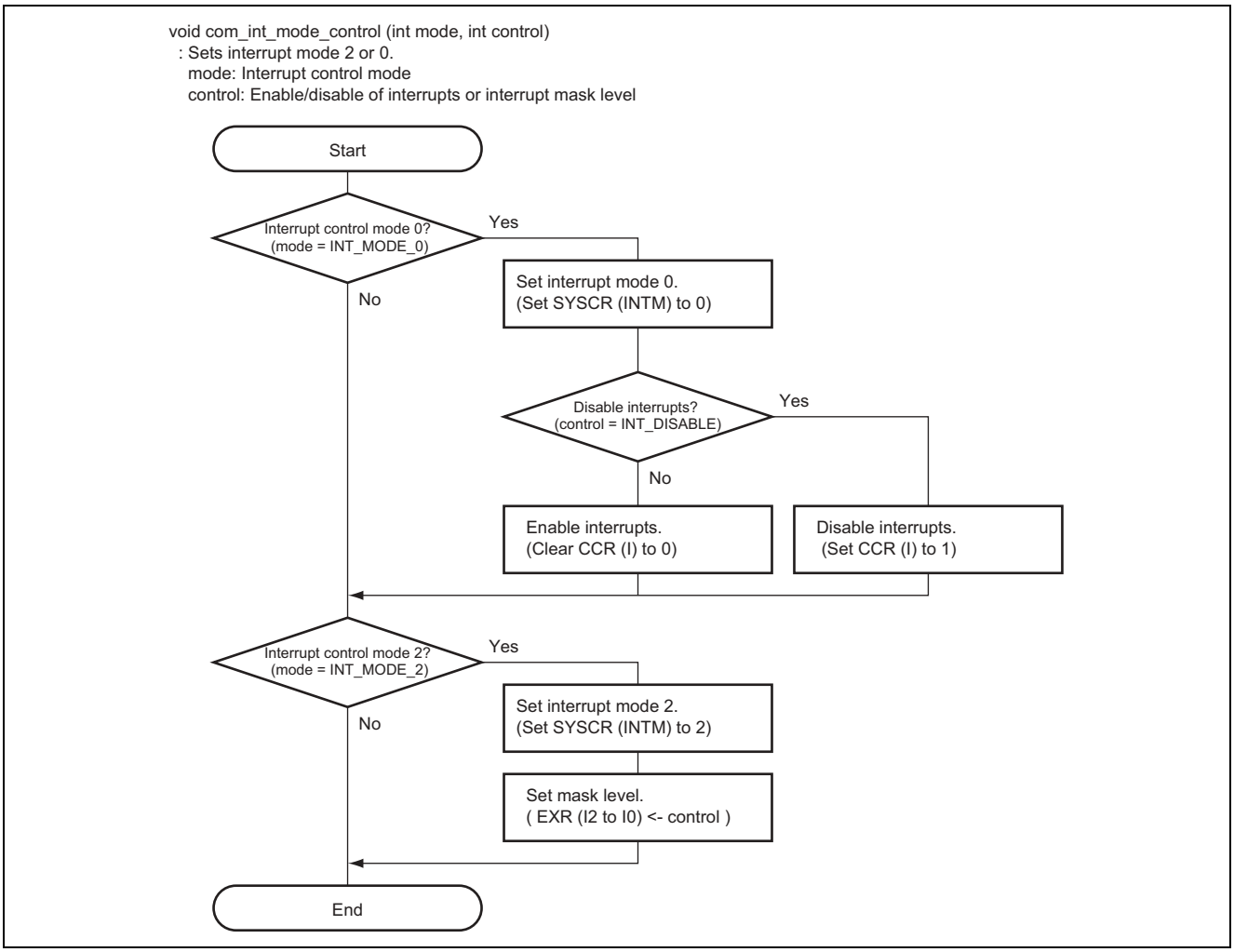
3.6 List of Registers Used

The internal registers of the H8 microcomputer used in the sample program are listed below. For detailed information, refer to the H8S/2215 Hardware Manual.

Name	Summary
System control register (SYSCR)	• Sets interrupt control mode • Sets the conditions for latching NMI interrupt • Enables/disables manual resets • Enables/disables the on-chip RAM
Interrupt priority registers (IPRA to IPRG, IPRI to IPRK and IPRM)	• Sets interrupt priorities
IRQ enable register (IER)	• Enables/disables external interrupts (IRQ)
IRQ sense control registers (ISCRH and ISCRL)	• Sets the conditions for latching external interrupts (IRQ) (Low-level sense, falling edge, rising edge or both edges)

3.7 Flowchart

The sample program processing flow is shown below.



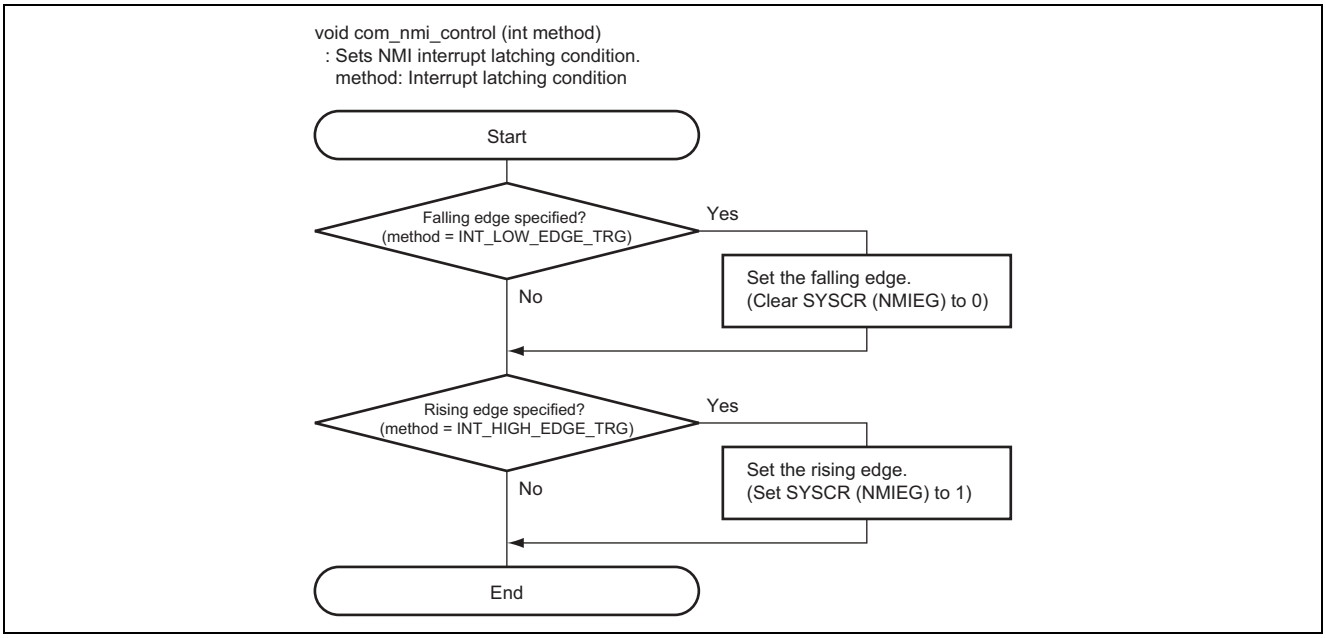
void com_int_set_priority (void)
: Sets interrupt priority for interrupt control mode 2.
Sets the priority data in the common variable table (int_pri_tbl) into the corresponding IPR register.

int_pri_tbl

Array Element	Name	Description	Register to be Set	
[0]	INT_IRQ0	IRQ0	IPRA	bit6 to 4
[1]	INT_IRQ1	IRQ1	IPRA	bit2 to 0
[2]	INT_IRQ2_3	IRQ2 and IRQ3	IPRB	bit6 to 4
[3]	INT_IRQ4_5	IRQ4 and IRQ5	IPRB	bit2 to 0
[4]	INT_IRQ6_7	IRQ6 and IRQ7	IPRC	bit6 to 4
[5]	INT SWDTEND	DTC software activation interrupt (SWDTEND)	IPRC	bit2 to 0
[6]	INTWOVI	WDT interval timer mode interrupt	IPRD	bit6 to 4
[7]	INT_ADI	AD conversion end interrupt	IPRE	bit2 to 0
[8]	INT_TPU0	TGI0A, TGI0B, TGI0C, TGI0D and TCI0V interrupts for the TPU0	IPRF	bit6 to 4
[9]	INT_TPU1	TGI1A, TGI1B, TCI1V and TCI1U interrupts for the TPU1	IPRF	bit2 to 0
[10]	INT_TPU2	TGI2A, TGI2B, TCI2V and TCI2U interrupts for the TPU2	IPRG	bit6 to 4
[11]	INT_TMR0	CMIA0, CMIB0 and OVI0 interrupts for the 8-bit timer 0	IPRI	bit6 to 4
[12]	INT_TMR1	CMIA1, CMIB1 and OVI1 interrupts for the 8-bit timer 1	IPRI	bit2 to 0
[13]	INT_DMAC	DEND0A, DEND0B, DEND1A and DEND1B interrupts for the DMAC	IPRJ	bit6 to 4
[14]	INT_SCI0	ERI0, RXI0, TXI0 and TEI0 interrupts for the SCI0	IPRJ	bit2 to 0
[15]	INT_SCI1	ERI1, RXI1, TXI1 and TEI1 interrupts for the SCI1	IPRK	bit6 to 4
[16]	INT_SCI2	ERI2, RXI2, TXI2 and TEI2 interrupts for the SCI2	IPRK	bit2 to 0
[17]	INT_USB	EXIRQ0 and EXIRQ1 interrupts for the USB	IPRM	bit6 to 4

void com_irq_control
: Enables/disables IRQ interrupts and selects interrupt generation mode
kind: Kinds of interrupts
method: Interrupt acceptance condition
control: Enabling/disabling of interrupts

"kind"	Register to set "method" (0: Low-level sense, 1: Falling edge, 2: Rising, 3: Falling and rising edges)	Register to set "control" (0: Interrupts are disabled 1: Interrupts are enabled)
INT_IRQ0	ICSR(IRQ0SC)	IER(IRQ0E)
INT_IRQ1	ICSR(IRQ1SC)	IER(IRQ1E)
INT_IRQ2	ICSR(IRQ2SC)	IER(IRQ2E)
INT_IRQ3	ICSR(IRQ3SC)	IER(IRQ3E)
INT_IRQ4	ICSR(IRQ4SC)	IER(IRQ4E)
INT_IRQ5	ICSR(IRQ5SC)	IER(IRQ5E)
INT_IRQ6	ICSR(IRQ6SC)	IER(IRQ6E)
INT_IRQ7	ICSR(IRQ7SC)	IER(IRQ7E)



4. Reference Documents

- H8S/2215 Series Hardware Manual (published by Renesas Technology Corporation)

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16, 2004	—	First edition issued

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