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H8S/2200 Series

Using Input Capture Function of 16-Bit Timer Pulse Unit

Introduction

The period of the pulses input through an external input pin is measured using the compare-match function of the 16-bit timer pulse unit.

Target Device

H8S/2215

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1. Specifications

- As shown in figure 1, by using the input capture function of the 16-bit timer pulse unit, the TCNT value is transferred to TGR when an edge signal is input from the TIOCA pin (35 pin).
- In 16-MHz operation, the period of TCNT counting can be set to 4.096 ms, 16.384 ms, 65.536 ms or 262 ms. In this sample task, it is set to 16.384 ms.
- The maximum measurable pulse period is 0.26 seconds, for which the measurement accuracy is 4 μ s.

$$\text{Pulse period} = (\text{Count value transferred to TGRA}_0) \times (\text{Period of the input clock of TCNT})$$
 Note: The input clock for TCNT is set with the timer prescaler bits in TCR.

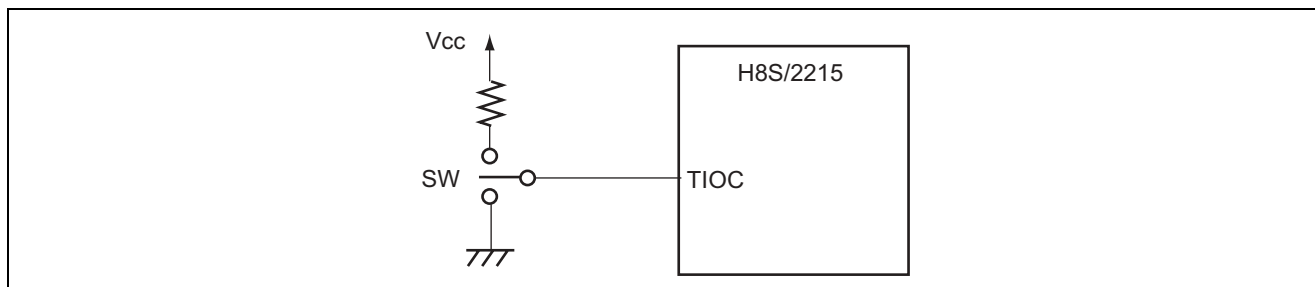


Figure 1 Example of Input for TPU Input Capture Function

2. Description of Functions

- Figure 2 shows a block diagram of the 16-bit timer pulse unit (TPU), and the following is the description for the block diagram:
 - The timer control register (TCR) controls settings for TCNT on each channel, such as counter clearing conditions based on TGR registers, etc.
 - The timer mode register (TMDR) sets operating mode, for example, normal operating mode and buffer operating mode, for each channel.
 - The timer I/O control register (TIOR: TIORH and TIORL) controls output signals by setting the initial output value and output value in compare-match/input-capture operation for each TGR.
 - The timer interrupt enable register (TIER) enables/disables interrupts for each channel.
 - The timer status register (TSR) indicates the status for each channel.
 - The timer counter (TCNT) is a 16-bit counter that can be read or written to. This counter is always accessed in 16-bit units.
 - The timer general registers (four registers from TGRA to TGRD) are 16-bit readable/writable registers that are used for output compare or input capture. These registers are always accessed in 16-bit units.
 - The timer start register (TSTR) selects to start or stop TCNT operation for channels 0 to 2.
 - The timer synchro register (TSYR) selects independent or synchronous operation of TCNTs on channels 0 to 2.

Note that the description above has focused on the channel 0 registers.

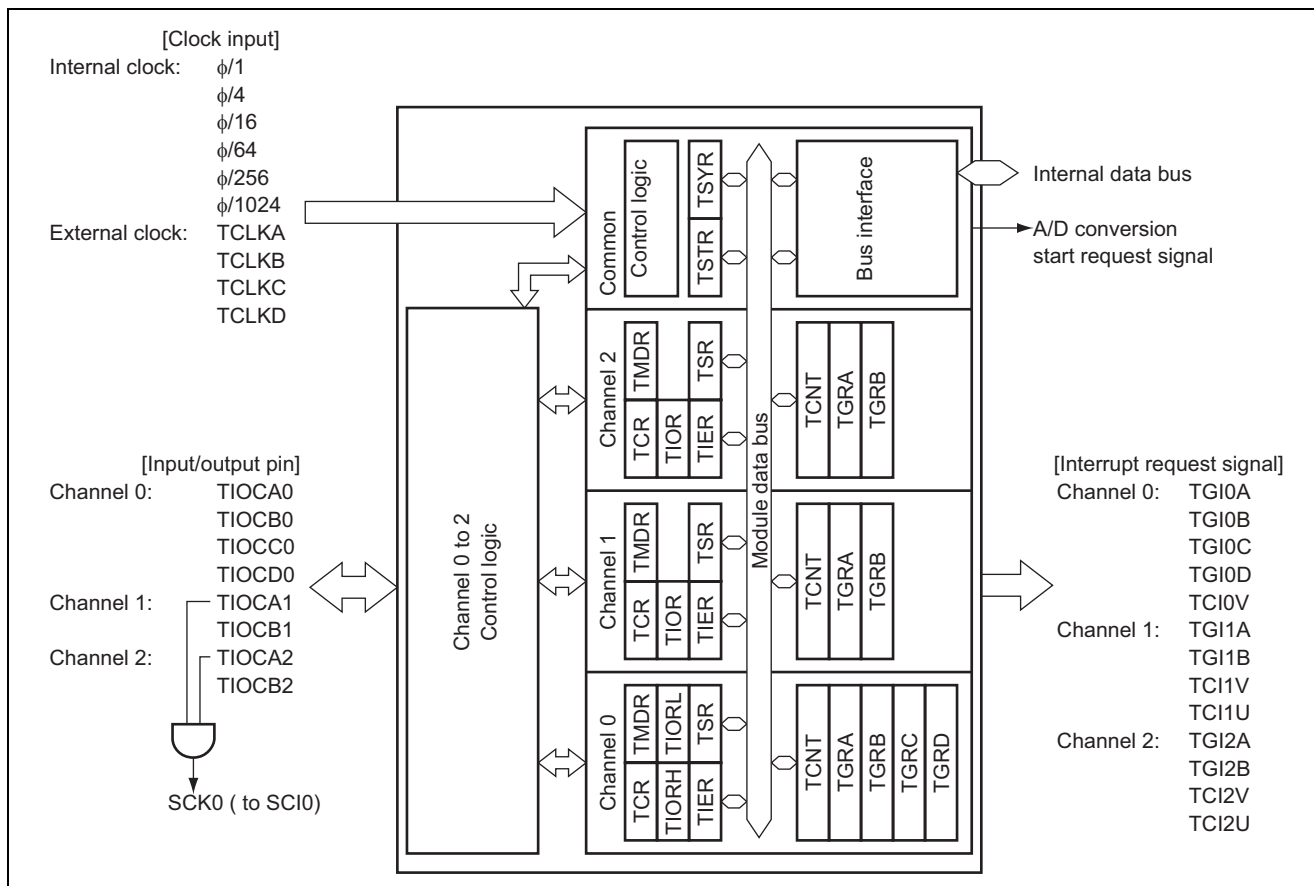


Figure 2 Block Diagram of TPU

2. Table 1 shows the assignment of functions used in this sample task.

Table 1 Assignment of Functions

Elements	Description
TCR	Controls TCNT for each channel (counter clearing condition, clock edge selection, etc.).
TMDR	Sets the operating mode for each channel: normal operation, PWM operation, etc.
TIOR	Sets output level on compare-match, etc.
TIER	Enables/disables interrupt requests.
TSR	Consists of flags indicating overflow, input capture/output compare, etc.
TCNT	16-bit counter that can be read or written to.
TGR	Registers used for input capture or output compare.
TSTR	Starts or stops counting by TCNT.
TSYR	Selects independent operation or synchronous operation of TCNTs on channels 0 to 2.

3. Principles of Operation

Figure 3 illustrates the operation of this sample task. The counter value of TCNT_0 is captured through the hardware and software processing shown in the figure.

1. Counting starts by setting TSTR to start counting on channel 0.
2. The TCNT_0 count value is transferred to TGRA every time an edge signal is input from the TIOCA0 pin.

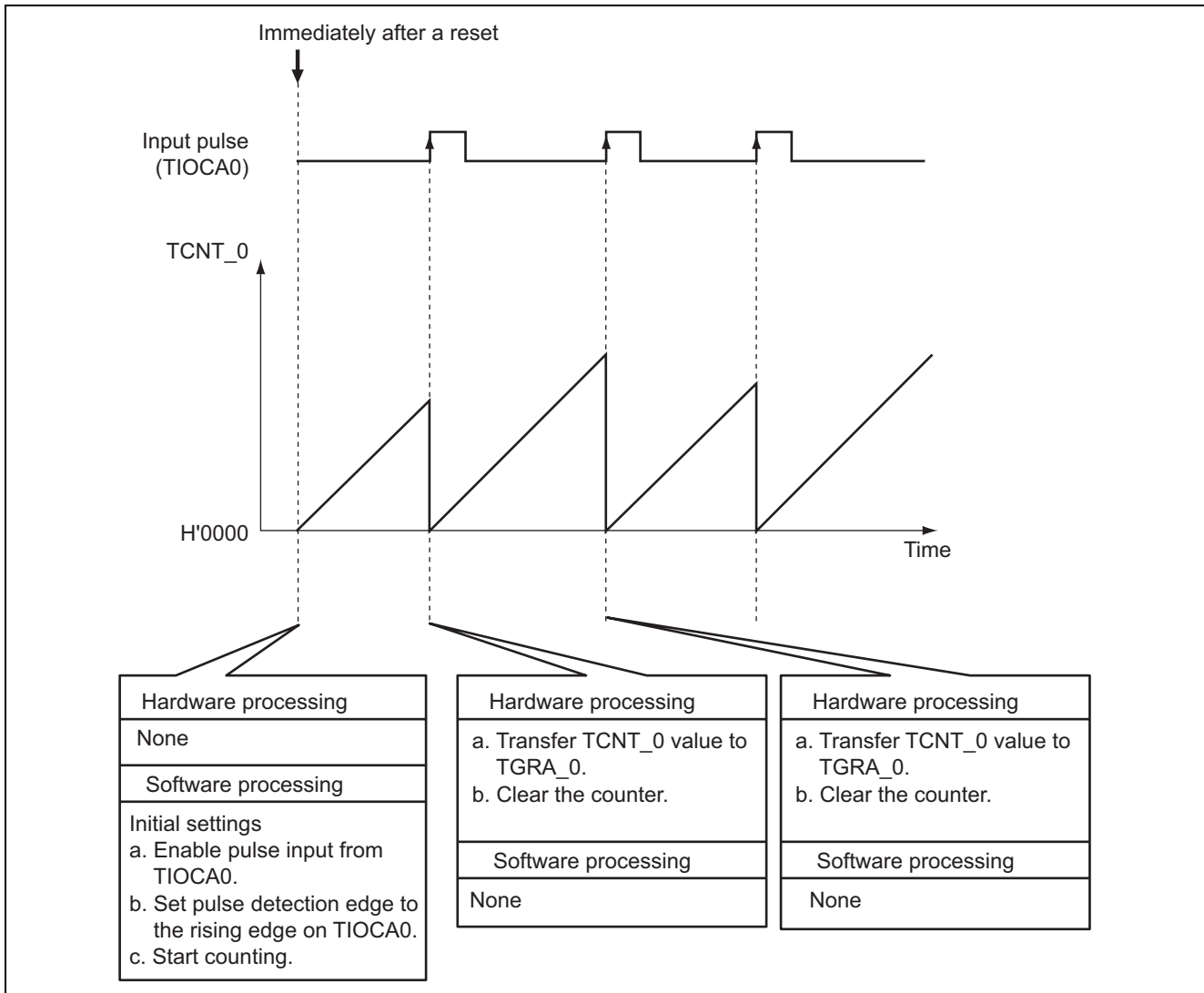


Figure 3 Input Capture Operation with Edge Input

4. Description of Software

4.1 Module

Table 2 describes the module used in this sample task.

Table 2 Description of Modules

Module	Label	Function
Main routine	main	Transfers the value of TCNT_0 that is in counting operation to TGRA_0 whenever an edge signal is input to the TIOCA0 pin.

4.2 Arguments

This sample program does not use arguments.

4.3 Internal Registers

The internal registers used in this sample task are described in table 3.

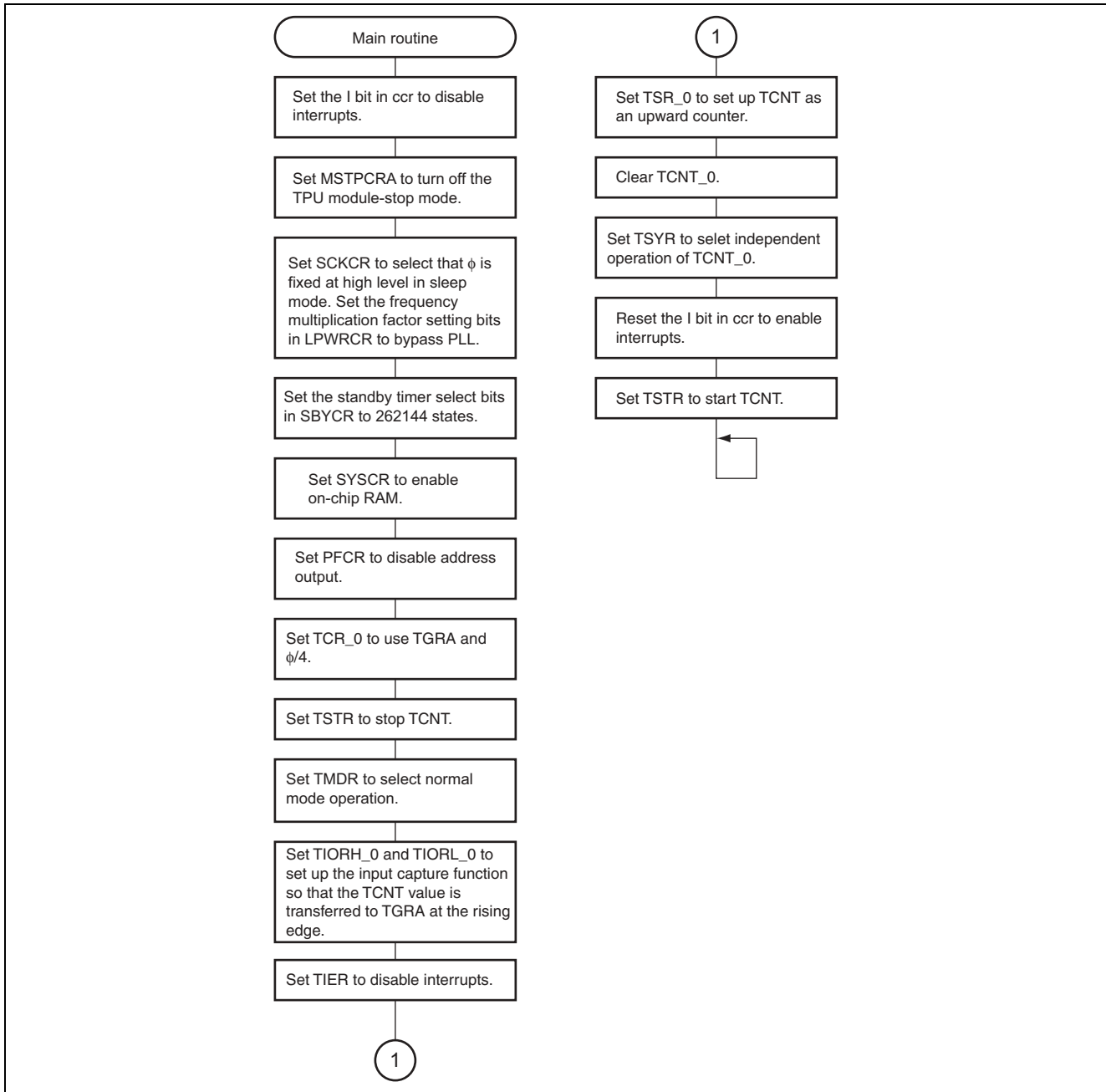
Table 3 Description of Internal Registers

Register	Function	Address	Setting
TCR_0	CCLR2	Timer Control Register_0 (Counter Clear 2 to 0)	H'FFFF10
	CCLR1	When CCLR2, CCLR1 and CCLR0 = 001, TCNT is cleared on	Bits 7 to 5
	CCLR0	TGRA compare-match or input capture.	
CKEG1	CKEG1	Timer Control Register_0 (Clock Edge 1, 0)	H'FFFF10
	CKEG0	When CKEG1 and CKEG0 = 00, TCNT is incremented at the rising edge.	Bit 4
		When CKEG1 and CKEG0 = 01, TCNT is incremented at the falling edge.	Bit 3
TPSC2	TPSC2	When CKEG1 and CKEG0 = 1X, TCNT is incremented at both edges (X: Don't care).	
	TPSC1	Timer Control Register_0 (Timer Prescaler 2 to 0)	H'FFFF10
	TPSC0	When TPSC2 to TPSC0 = 001, TCNT is incremented by the internal clock $\phi/4$.	Bits 2 to 0
TMDR_0	BFB	Timer Mode Register_0 (Buffer Operation B)	H'FFFF11
		When BFB = 0, TGRB performs normal operation.	Bit 5
		When BFB = 1, TGRB and TGRD perform buffer operation.	
BFA	BFA	Timer Mode Register_0 (Buffer Operation A)	H'FFFF11
		When BFA = 0, TGRA performs normal operation.	Bit 4
		When BFA = 1, TGRA and TGRC perform buffer operation.	
MD3	MD3	Timer Mode Register_0 (Mode 3 to 0)	H'FFFF11
	MD2	When MD3 to MD0 = 0000, the timer operates in normal mode.	Bits 3 to 0
	MD1	Note: MD3 is a reserved bit. Only 0 should be written to this bit.	
	MD0		0, 0, 0, 0
TIORH_0	IOB3	Timer I/O Control Register H_0 (I/O Control B3 to B0)	H'FFFF12
	IOB2	When IOB3 to IOB0 = 0000, output is disabled.	Bits 7 to 4
	IOB1		
	IOB0		0, 0, 0, 0
IOA3	IOA3	Timer I/O Control Register H_0 (I/O Control A3 to A0)	H'FFFF12
	IOA2	When IOA3 to IOA0 = 1000, input capture is performed at the rising edge on the TIOCA0 pin.	Bits 3 to 0
	IOA1		
	IOA0		1, 0, 0, 0

Register	Function	Address	Setting
TSR_0	TCFD	Timer Status Register (Count Direction Flag) TCFD = 0 indicates that TCNT is a downward counter. TCFD = 1 indicates that TCNT is an upward counter.	H'FFFF15 1 Bit 7
	TCFU	Timer Status Register (Underflow Flag) TCFU = 0 indicates that a TCNT underflow has not occurred. TCFU = 1 indicates that a TCNT underflow has occurred.	H'FFFF15 0 Bit 5
	TCFV	Timer Status Register (Overflow Flag) TCFU = 0 indicates that a TCNT overflow has not occurred. TCFU = 1 indicates that a TCNT overflow has occurred.	H'FFFF15 0 Bit 4
	TGFA	Timer Status Register (Interrupt Capture/Output Compare Flag A) TGFA = 0 indicates that TCNT value does not match TGFA value. TGFA = 1 indicates that TCNT value matches TGFA value.	H'FFFF15 0 Bit 0
TCNT	Timer Counter 16-bit counter that can be read or written to	H'FFFF16	H'0000
TGRA_0	Timer General Register A_0 16-bit readable/writable register that is used for output compare or input capture	H'FFFF18	H'0000
TSTR	CST2	Timer Start Register (Counter Start 2 to 0) When CSTn = 0, count operation of the corresponding TCNT is stopped. When CSTn = 1, count operation of the corresponding TCNT is performed. Note: Bits 7 to 3 are reserved. Only 0 should be written to these bits.	H'FFFE B0 0, 0, 0 Bits 2 to 0
	CST1		
	CST0		
TSYR	SYNC2	Timer Synchro Register (Timer Synchronization 2 to 0) When SYNCn = 0, the corresponding TCNTn operates independently. When SYNCn = 1, the corresponding TCNTn operates synchronously.	H'FFFE B1 0, 0, 0 Bits 2 to 0
	SYNC1		
	SYNC0		
TIER_0	TCIEU	Timer Interrupt Enable Register (Underflow Interrupt Enable) When TCIEU = 0, an interrupt request (TCIU) by the TCFU flag is disabled. When TCIEU = 1, an interrupt request (TCIU) by the TCFU flag is enabled.	H'FFFF14 0 Bit 5
	TCIEV	Timer Interrupt Enable Register (Overflow Interrupt Enable) When TCIEV = 0, an interrupt request (TCIV) by the TCFV flag is disabled. When TCIEV = 1, an interrupt request (TCIV) by the TCFV flag is enabled.	H'FFFF14 0 Bit 4
	TGIEA	Timer Interrupt Enable Register (TGR Interrupt Enable A) When TGIEA = 0, an interrupt request (TGIA) by the TGFA flag is disabled. When TGIEA = 1, an interrupt request (TGIA) by the TGFA flag is enabled.	H'FFFF14 0 Bit 0

5. Flowchart

1. Main routine



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16, 2004	—	First edition issued

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