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# H8S/2200 Series

## Using 16-Bit Timer Pulse Unit to Produce PWM Output

### Introduction

PWM waveforms are output using the 16-bit timer pulse unit in PWM mode 2. The period and duty cycle can be set to desired values.

### Target Device

H8S/2215

### Contents

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## 1. Specifications

1. As shown in figure 1, PWM waveforms of various duty cycles are output by changing the high-level width of the pulses.
2. In 16-MHz operation, the period of the PWM waveform can be set within the range from 250 ns to 16 μs.

   The period f and duty cycle are set according to the following formulae.

   f = (TGRA_0 setting value + 1) × (1/(ϕ/1))
   When TGRA_0 = 0x00FF,
   f = (255 + 1) × 62.5 ns
   = 16 μs

   Duty cycle = (high-level pulse width × (1/(ϕ/1))/f) × 100 %
   When TGRB_0 = 0x0055,
   Duty cycle = (((85 + 1) × 62.5 μs)/16 μs) × 100 %
   = (5.38 μs/16 μs) × 100 %
   = 33.6 %

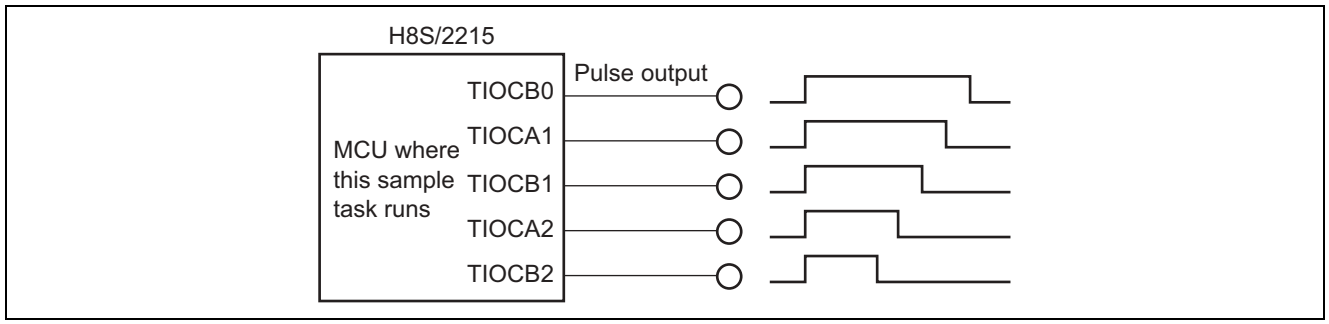



**Figure 1.1 Example of PWM Pulse Output**

## 2. Description of Functions

1. Figure 2 shows a block diagram of the 16-bit timer pulse unit (TPU), and the following is the description for the block diagram:
   - The timer control register (TCR) controls settings for TCNT on each channel, such as counter clearing conditions based on TGR registers, etc.
   - The timer mode register (TMDR) sets operating mode, for example, normal operating mode and buffer operating mode, for each channel.
   - The timer I/O control register (TIOR: TIORH and TIORL) controls output signals by setting the initial output value and output value in compare-match/input-capture operation for each TGR.
   - The timer interrupt enable register (TIER) enables/disables interrupts for each channel.
   - The timer status register (TSR) indicates the status for each channel.
   - The timer counter (TCNT) is a 16-bit counter that can be read or written to. This counter is always accessed in 16-bit units.
   - The timer general registers (four registers from TGRA to TGRD) are 16-bit readable/writable registers that are used for output compare or input capture. These registers are always accessed in 16-bit units.
   - The timer start register (TSTR) selects to start or stop TCNT operation for channels 0 to 2.
   - The timer synchro register (TSYR) selects independent or synchronous operation of TCNTs on channels 0 to 2.

Note that the description above has focused on the channel 0 registers.

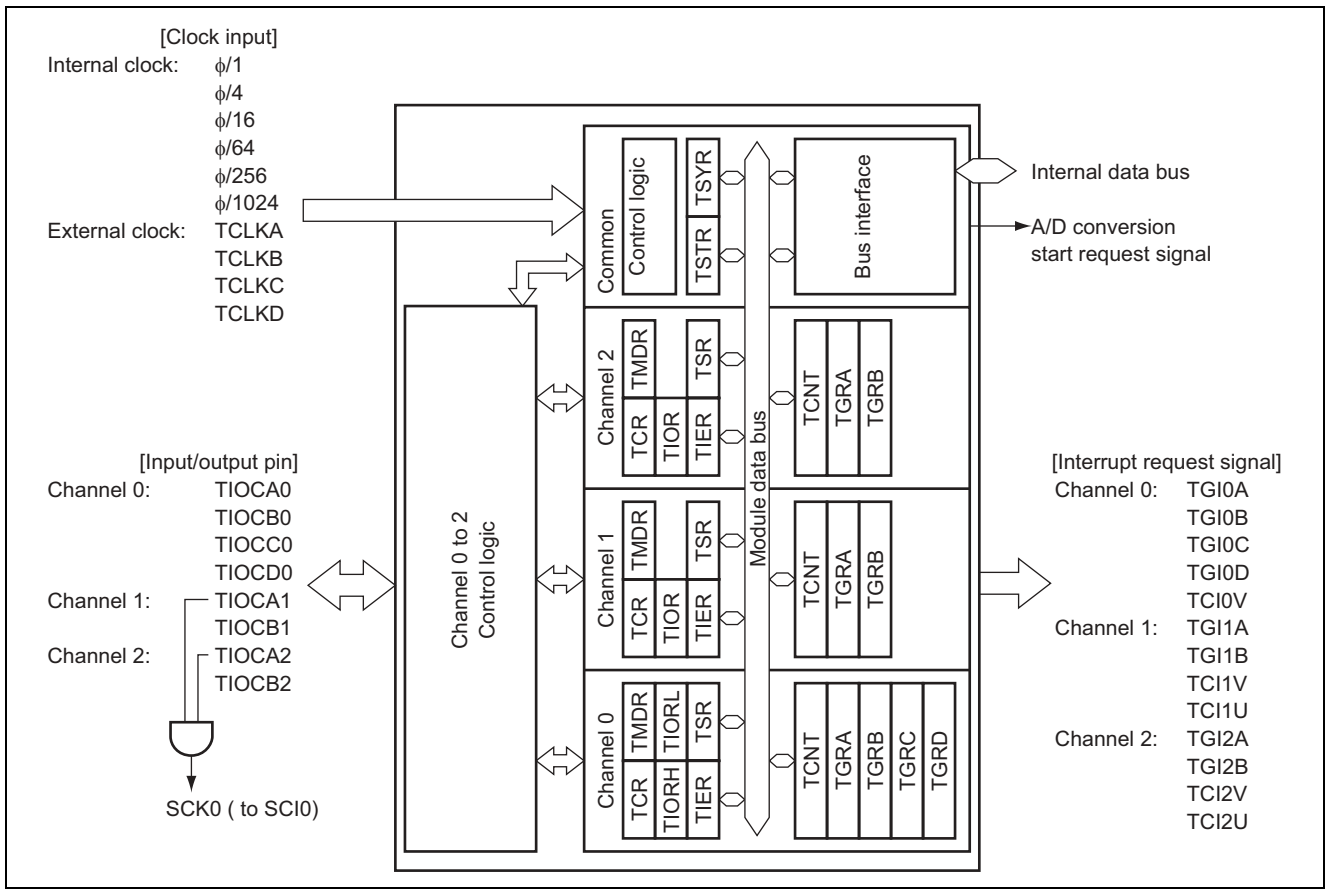



**Figure 2.1 Block Diagram of TPU**

2. Table 1 shows the assignment of functions used in this sample task.

**Table 1 Assignment of Functions**

| Elements | Description |
|---|---|
| TCR | Controls TCNT for each channel (counter clearing condition, clock edge selection, etc.). |
| TMDR | Sets the operating mode for each channel: normal operation, PWM operation, etc. |
| TIOR | Sets output level on compare-match, etc. |
| TIER | Enables/disables interrupt requests. |
| TSR | Consists of flags indicating overflow, input capture/output compare, etc. |
| TCNT | 16-bit counter that can be read or written to. |
| TGR | Registers used for input capture or output compare. |
| TSTR | Starts or stops counting by TCNT. |
| TSYR | Selects independent operation or synchronous operation of TCNTs on channels 0 to 2. |

## 3. Principles of Operation

Figure 3 illustrates the operation of this sample task. PWM waveforms of different duty cycles, which is obtained by varying the high-level widths, are output through the hardware and software processing shown in the figure.

1. The operating mode of the timer is set to PWM mode 2 with the pulse period set in TGRA_0 and duty cycles in other TGRs. The initial output values and output levels are set in TIOR.
2. Synchronous operation of the timer counters and start of counting are set to initiate the PWM output operation.

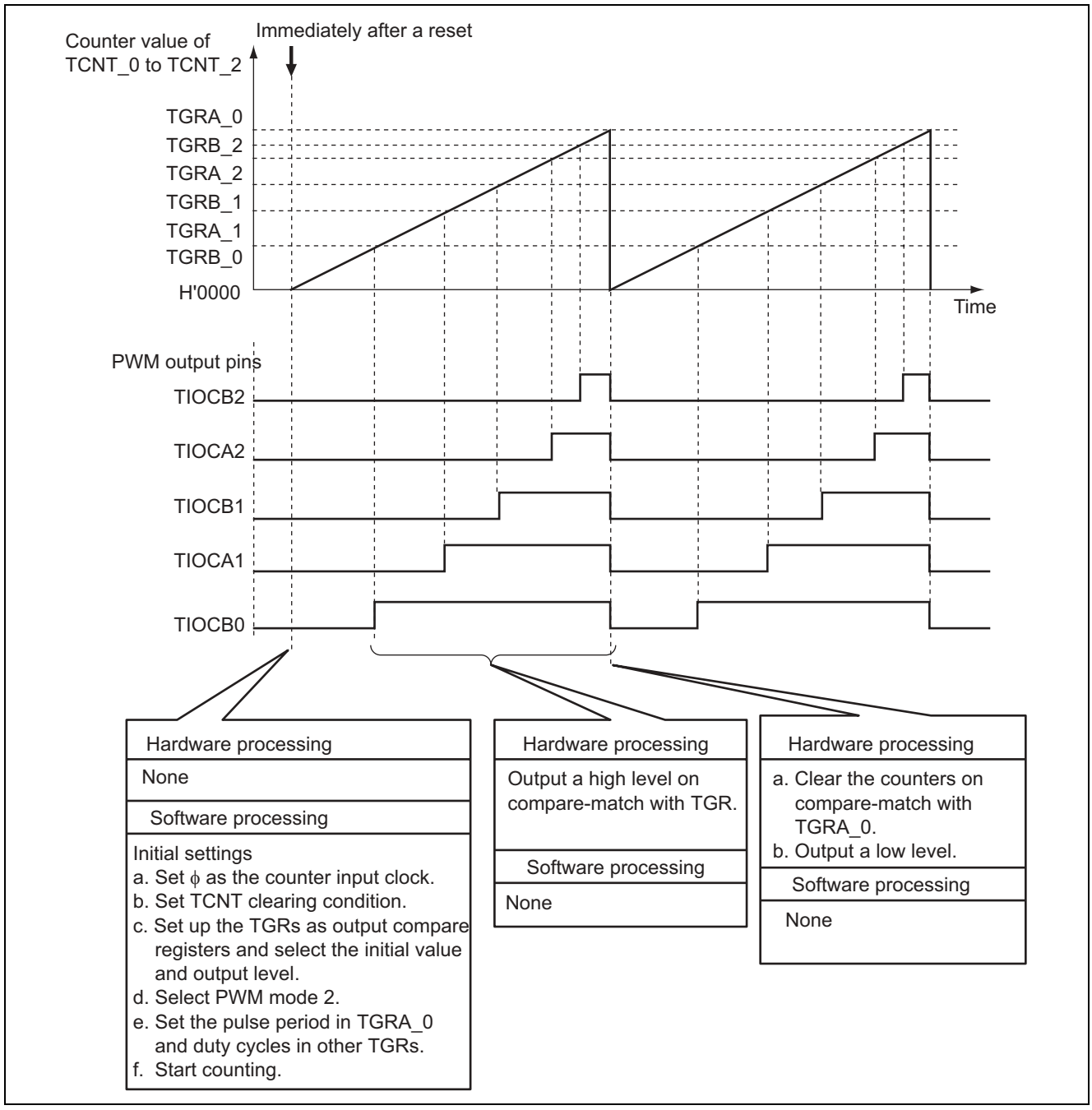



**Figure 3 PWM Pulse Output Operation**

# 4. Description of Software

## 4.1 Module

Table 2 describes the module used in this sample task.

**Table 2 Description of Modules**

| Module | Label | Function |
|---|---|---|
| Main routine | main | Synchronously clears TCNTs on channels 0 to 2, and outputs PWM waveforms as specified. |

## 4.2 Arguments

This sample program does not use arguments.

## 4.3 Internal Registers

The internal registers used in this sample task are described in table 3.

**Table 3 Description of Internal Registers**

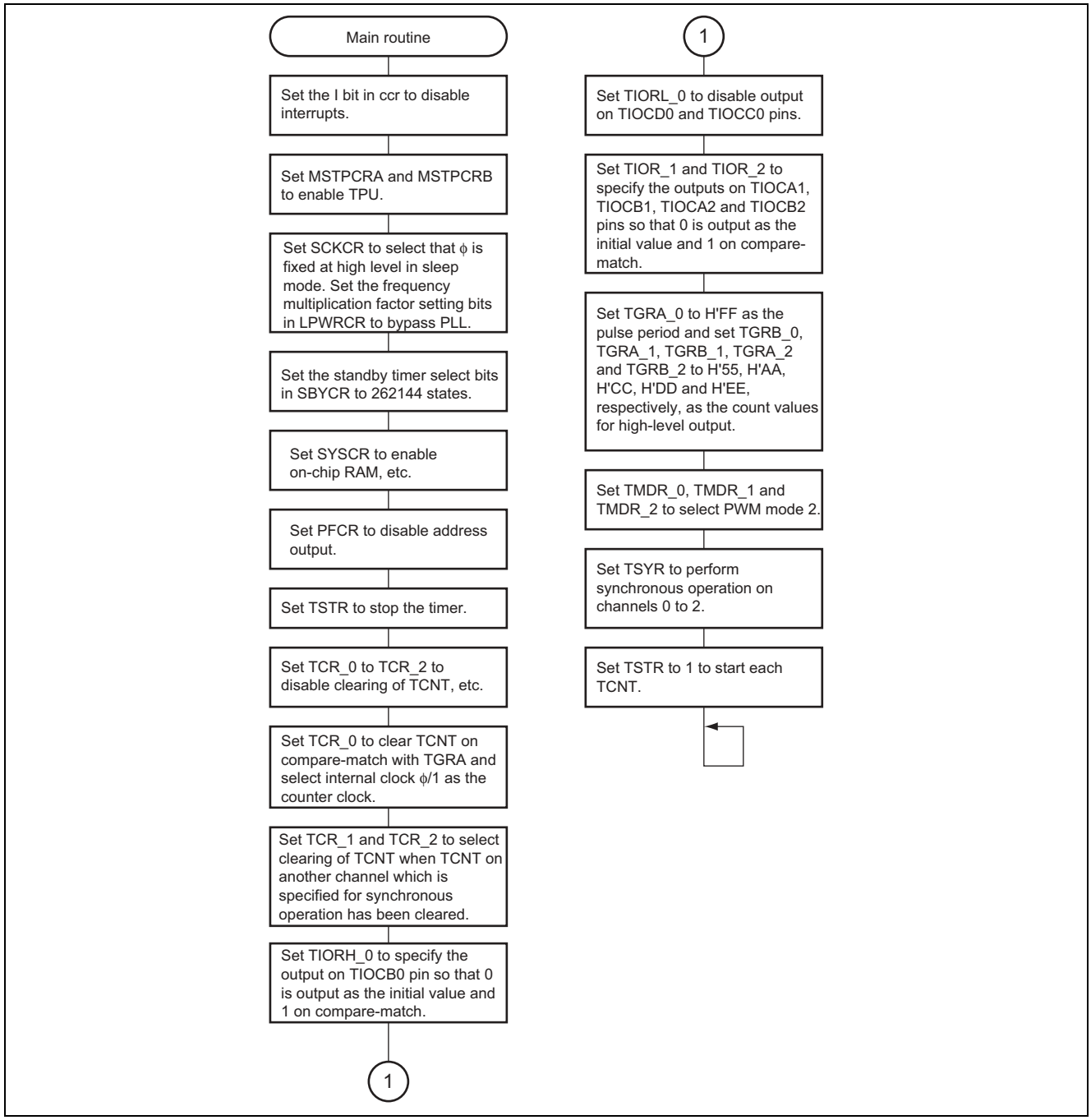
| Register | | Function | Address | Setting |
|---|---|---|---|---|
| TCR_0 | CCLR2<br>CCLR1<br>CCLR0 | Timer Control Register_0 (Counter Clear 2 to 0)<br>When CCLR2, CCLR1 and CCLR0 = 001, TCNT is cleared on TGRA compare-match or input capture. | H'FFFF10<br>Bits 7 to 5 | 0, 0, 1 |
| | CKEG1<br>CKEG0 | Timer Control Register_0 (Clock Edge 1, 0)<br>When CKEG1 and CKEG0 = 00, TCNT is incremented at the rising edge.<br>When CKEG1 and CKEG0 = 01, TCNT is incremented at the falling edge.<br>When CKEG1 and CKEG0 = 1X, TCNT is incremented at both edges (X: Don't care). | H'FFFF10<br>Bit 4<br>Bit 3 | 0, 0 |
| | TPSC2<br>TPSC1<br>TPSC0 | Timer Control Register_0 (Timer Prescaler 2 to 0)<br>When TPSC2 to TPSC0 = 000, TCNT is incremented by the internal clock $\phi$/1. | H'FFFF10<br>Bits 2 to 0 | 0, 0, 0 |
| TCR_1 | CCLR1<br>CCLR0 | Timer Control Register_1 (Counter Clear 1, 0)<br>When CCLR1 and CCLR0 = 11, the TCNT of this channel is cleared when TCNT on another channel which has been set up for synchronous operation is cleared. | H'FFFF20<br>Bit 6<br>Bit 5 | 1, 1 |
| | CKEG1<br>CKEG0 | Timer Control Register_1 (Clock Edge 1, 0)<br>When CKEG1 and CKEG0 = 00, TCNT is incremented at the rising edge.<br>When CKEG1 and CKEG0 = 01, TCNT is incremented at the falling edge.<br>When CKEG1 and CKEG0 = 1X, TCNT is incremented at both edges (X: Don't care). | H'FFFF20<br>Bit 4<br>Bit 3 | 0, 0 |
| | TPSC2<br>TPSC1<br>TPSC0 | Timer Control Register_1 (Timer Prescaler 2 to 0)<br>When TPSC2 to TPSC0 = 000, TCNT is incremented by the internal clock $\phi$/1. | H'FFFF20<br>Bits 2 to 0 | 0, 0, 0 |

| Register | | Function | Address | Setting |
|---|---|---|---|---|
| TCR_2 | CCLR1<br>CCLR0 | Timer Control Register_2 (Counter Clear 1, 0)<br>Same as TCR_1 above | H'FFFF30<br>Bit 6<br>Bit 5 | 1, 1 |
| | CKEG1<br>CKEG0 | Timer Control Register_2 (Clock Edge 1, 0)<br>Same as TCR_1 above | H'FFFF30<br>Bit 4<br>Bit 3 | 0, 0 |
| | TPSC2<br>TPSC1<br>TPSC0 | Timer Control Register_2 (Timer Prescaler 2 to 0)<br>Same as TCR_1 above | H'FFFF30<br>Bits 2 to 0 | 0, 0, 0 |
| TMDR_0 | BF8 | Timer Mode Register_0 (Buffer Operation B)<br>When BFB = 0, TGRB performs normal operation.<br>When BFB = 1, TGRB and TGRD perform buffer operation. | H'FFFF11<br>Bit 5 | 0 |
| | BFA | Timer Mode Register_0 (Buffer Operation A)<br>When BFA = 0, TGRA performs normal operation.<br>When BFA = 1, TGRA and TGRC perform buffer operation. | H'FFFF11<br>Bit 4 | 0 |
| | MD3<br>MD2<br>MD1<br>MD0 | Timer Mode Register_0 (Mode 3 to 0)<br>When MD3 to MD0 = 0011, the timer operates in PWM mode 2.<br>Note: MD3 is a reserved bit. Only 0 should be written to this bit. | H'FFFF11<br>Bits 3 to 0 | 0, 0, 1, 1 |
| TMDR_1 | MD3<br>MD2<br>MD1<br>MD0 | Timer Mode Register_1 (Mode 3 to 0)<br>Same as TMDR_0 above | H'FFFF21<br>Bits 3 to 0 | 0, 0, 1, 1 |
| TMDR_2 | MD3<br>MD2<br>MD1<br>MD0 | Timer Mode Register_2 (Mode 3 to 0)<br>Same as TMDR_0 above | H'FFFF31<br>Bits 3 to 0 | 0, 0, 1, 1 |
| TIORH_0 | IOB3<br>IOB2<br>IOB1<br>IOB0 | Timer I/O Control Register H_0 (I/O Control B3 to B0)<br>Sets TGRB functions as follows:<br>When IOB3 to IOB0 = 0010, the initial output is 0 and 1 is output on compare-match. | H'FFFF12<br>Bits 7 to 4 | 0, 0, 1, 0 |
| | IOA3<br>IOA2<br>IOA1<br>IOA0 | Timer I/O Control Register H_0 (I/O Control A3 to A0)<br>Sets TGRA functions as follows:<br>When IOA3 to IOA0 = 0000, output is disabled. | H'FFFF12<br>Bits 3 to 0 | 0, 0, 0, 0 |
| TIORL_0 | IOD3<br>IOD2<br>IOD1<br>IOD0 | Timer I/O Control Register H_0 (I/O Control D3 to D0)<br>Sets TGRD functions as follows:<br>When IOD3 to IOD0 = 0000, output is disabled. | H'FFFF13<br>Bits 7 to 4 | 0, 0, 0, 0 |
| | IOC3<br>IOC2<br>IOC1<br>IOC0 | Timer I/O Control Register H_0 (I/O Control C3 to C0)<br>Sets TGRC functions as follows:<br>When IOC3 to IOC0 = 0000, output is disabled. | H'FFFF13<br>Bits 3 to 0 | 0, 0, 0, 0 |

| Register | | Function | Address | Setting |
|---|---|---|---|---|
| TIOR_1 | IOB3<br>IOB2<br>IOB1<br>IOB0 | Timer I/O Control Register_1 (I/O Control B3 to B0)<br>Sets TGRB functions as follows:<br>When IOB3 to IOB0 = 0010, the initial output is 0 and 1 is output on compare-match. | H'FFFF22<br>Bits 7 to 4 | 0, 0, 1, 0 |
| | IOA3<br>IOA2<br>IOA1<br>IOA0 | Timer I/O Control Register_1 (I/O Control A3 to A0)<br>Sets TGRA functions as follows:<br>When IOA3 to IOA0 = 0010, the initial output is 0 and 1 is output on compare-match. | H'FFFF22<br>Bits 3 to 0 | 0, 0, 1, 0 |
| TIOR_2 | IOB3<br>IOB2<br>IOB1<br>IOB0 | Timer I/O Control Register_2 (I/O Control B3 to B0)<br>Same as TIOR_1 above. | H'FFFF32<br>Bits 7 to 4 | 0, 0, 1, 0 |
| | IOA3<br>IOA2<br>IOA1<br>IOA0 | Timer I/O Control Register_2 (I/O Control A3 to A0)<br>Same as TIOR_1 above. | H'FFFF32<br>Bits 3 to 0 | 0, 0, 1, 0 |
| TCNT_0 | | Timer Counter<br>16-bit counter that can be read or written to | H'FFFF16 | H'0000 |
| TCNT_1 | | Timer Counter<br>16-bit counter that can be read or written to | H'FFFF20 | H'0000 |
| TCNT_2 | | Timer Counter<br>16-bit counter that can be read or written to | H'FFFF36 | H'0000 |
| TGRA_0 | | Timer General Register A_0<br>16-bit readable/writable register that is used for output compare or input capture | H'FFFF18 | H'00FF |
| TGRB_0 | | Timer General Register B_0<br>Same as above | H'FFFF1A | H'0055 |
| TGRA_1 | | Timer General Register A_1<br>Same as above | H'FFFF28 | H'00AA |
| TGRB_1 | | Timer General Register B_1<br>Same as above | H'FFFF2A | H'00CC |
| TGRA_2 | | Timer General Register A_2<br>Same as above | H'FFFF38 | H'00DD |
| TGRB_2 | | Timer General Register B_2<br>Same as above | H'FFFF3A | H'00EE |
| TSTR | CST2<br>CST1<br>CST0 | Timer Start Register (Counter Start 2 to 0)<br>When CSTn = 0, count operation of the corresponding TCNT is stopped.<br>When CSTn = 1, count operation of the corresponding TCNT is performed.<br>Note: Bits 7 to 3 are reserved. Only 0 should be written to these bits. | H'FFFEB0<br>Bits 2 to 0 | 1, 1, 1 |
| TSYR | SYNC2<br>SYNC1<br>SYNC0 | Timer Synchro Register (Timer Synchronization 2 to 0)<br>When SYNCn = 0, the corresponding TCNTn operates independently.<br>When SYNCn = 1, the corresponding TCNTn operates synchronously. | H'FFFEB1<br>Bits 2 to 0 | 1, 1, 1 |

## 5. Flowchart

1. Main routine



## Revision Record

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