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H8S/2200 Series

Using 16-Bit Timer Pulse Unit in Phase Counting Mode

Introduction

Phase counting mode of the 16-bit timer pulse unit is used to detect the phase difference between the signals input through the external clock input pins.

Target Device

H8S/2215

Contents

1. Overview

The phase counting function of the H8S/2215's TPU is used to detect phase differences between the signals from the external clock pins (channel 1: TCLKA and TCLKB, channel 2: TCLKC and TCLKD) and the H8 microcomputer's internal counter (TCNT) is incremented/decremented accordingly.

2. Configuration

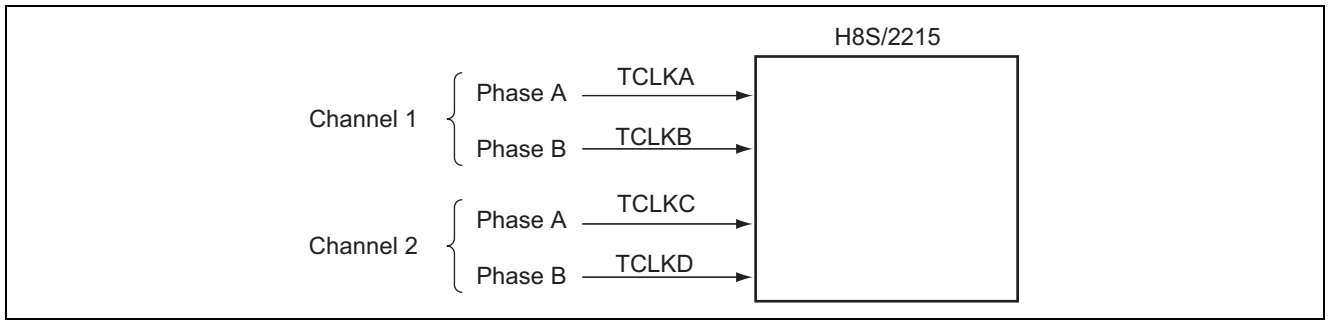


Figure 2.1 Example of Inputs for Phase Counting Mode

Table 2.1 Pin Configuration

Signal Name	Description
TCLKA	External clock phase-A for channel 1
TCLKB	External clock phase-B for channel 1
TCLKC	External clock phase-A for channel 2
TCLKD	External clock phase-B for channel 2

3. Sample Programs

3.1 Functions

1. Sets up the TPU in phase counting mode.
2. Starts/stops the TPU counter.
3. Reads the TPU status.
4. Reads the TPU counter value.
5. Sets a value into the TPU counter.

3.2 Program Incorporation

1. Incorporate sample program 3-A: #define definitions.
2. Incorporate sample program 3-B: prototype declarations.
3. Incorporate sample program 3-C: common subroutines.

3.3 Modifications to Sample Programs

Without modifications to the sample program, the system may not run. Modifications must be made according to your program and system environment.

1. The sample programs can be used without further changes if you use the I/O register structure definition file, which is available free of charge from the following Renesas web site:
   http://www.renesas.com/eng/products/mpumcu/tool/crosstool/iodef/index.html
   When you create structure definitions by yourself, modify the I/O register structures used in the sample program as appropriate.

3.4 Using the Sample Programs

Subroutines provided in the sample programs are described below.

1. Sets up the TPU in phase counting mode.

- Subroutine name: **int** com_tpu_count_mode **(int** ch_no , **int** count_mode)

Argument	Setting
ch_no	Specifies a TPU channel (TPU channel 0 does not support the phase counting function.) TPU_CH1 (1): TPU channel 1 is selected. TPU_CH2 (2): TPU channel 2 is selected.
count_mode	Specifies phase counting mode. TPU_PHASE_COUNT_RESET (0): Phase counting mode is canceled. TPU_PHASE_COUNT_1 (4): Phase counting mode 1 is specified. TPU_PHASE_COUNT_2 (5): Phase counting mode 2 is specified. TPU_PHASE_COUNT_3 (6): Phase counting mode 3 is specified. TPU_PHASE_COUNT_4 (7): Phase counting mode 4 is specified.

Return value	Description
NORMAL_END (0)	Normal termination
TPU_BUSY (-1)	Parameters cannot be set because TPU is counting.
TPU_PARM_ERR (-2)	A value other than 1 or 2 has been set for ch_no.

2. Starts/stops the TPU counter.

- Subroutine name: **void** com_tpu_control **(int** ch_no , **int** control)

Argument	Setting
ch_no	Specifies a TPU channel. Multiple channels can be specified at a time. TPU_CH0 (0): TPU channel 0 is selected. TPU_CH1 (1): TPU channel 1 is selected. TPU_CH2 (2): TPU channel 2 is selected. TPU_CH0_1 (3): TPU channels 0 and 1 are selected. TPU_CH0_2 (4): TPU channels 0 and 2 are selected. TPU_CH1_2 (5): TPU channels 1 and 2 are selected. TPU_CH0_1_2 (6): TPU channels 0, 1 and 2 are selected.
control	Starts/stops the TPU counter. TPU_STOP (0): TPU stops counting. TPU_START (1): TPU starts counting.

3. The TPU status is read.

- Subroutine name: **unsigned char** com_tpu_read_status **(int** ch_no)

Argument	Setting
ch_no	Specifies a TPU channel. TPU_CH0 (0): TPU channel 0 is selected. TPU_CH1 (1): TPU channel 1 is selected. TPU_CH2 (2): TPU channel 2 is selected.

Return value	Description
8-bit data	Contents of the timer status register (TSR) for the specified TPU channel

Bit	Name	Contents
7	TCFD	Count direction (Valid for TPU1 and TPU2) 0: TCNT is counting downward. 1: TCNT is counting upward.
6	—	(Reserved)
5	TCFU	Underflow flag (Valid for TPU1 and TPU2) 1: An underflow has occurred in phase counting mode.
4	TCFV	Overflow flag (Valid for TPU1 and TPU2) 1: An overflow has occurred in phase counting mode.
3	TFGD	Input capture/output compare flag D
2	TFGC	Input capture/output compare flag C
1	TFGB	Input capture/output compare flag B
0	TFGA	Input capture/output compare flag A

Note: For details, refer to description of the TPU register (TSR) in the H8S/2215 Hardware Manual.

4. Reads the TPU counter value.

- Subroutine name: **unsigned int** com_tpu_read_cnt_data **int** ch_no)

Argument	Setting
ch_no	Specifies a TPU channel. TPU_CH0 (0): TPU channel 0 is selected. TPU_CH1 (1): TPU channel 1 is selected. TPU_CH2 (2): TPU channel 2 is selected.

Return value	Description
16-bit data	Contents of the counter register (TCNT) for the specified TPU channel

5. Sets a value into the TPU counter.

- Subroutine name: **unsigned int** com_tpu_write_cnt_data (**int** ch_no , **unsigned int** count_data)

Argument	Setting
ch_no	Specifies a TPU channel. TPU_CH0 (0): TPU channel 0 is selected. TPU_CH1 (1): TPU channel 1 is selected. TPU_CH2 (2): TPU channel 2 is selected.
count_data	Counter setting value

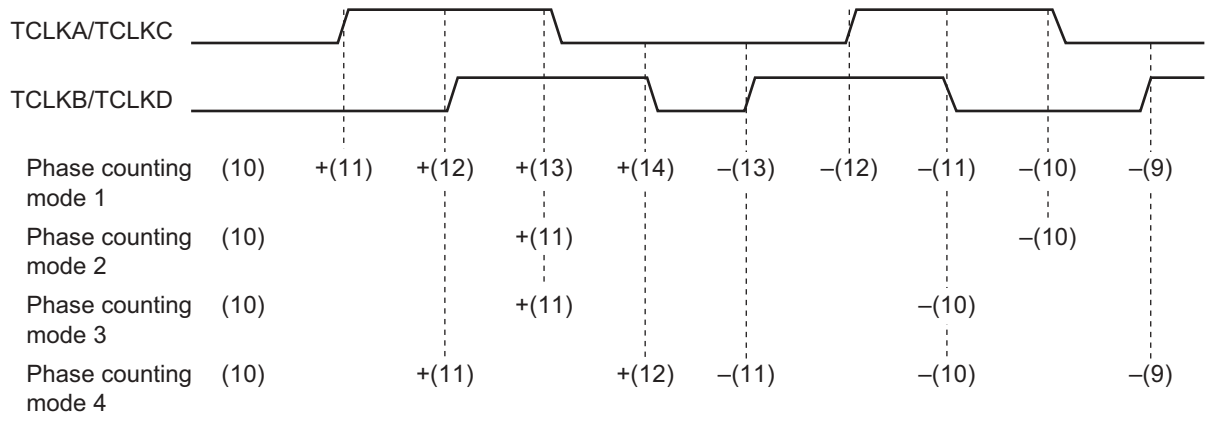
3.5 Description of Operation

3.5.1 Count Conditions in Phase Counting Mode

The phase counting function is only supported by TPU channels 1 and 2. Phase differences between two external clock inputs are detected and the counter (TCNT) is incremented or decremented. There are four phase counting modes, where different count conditions are applied.

External Clock Input		TCNT Count Direction			
Phase A	**Phase B**				
TCLKA (channel 1) **TCLKC (channel 2)**	**TCLKB (channel 1)** **TCLKD (channel 2)**	**Phase counting mode 1**	**Phase counting mode 2**	**Phase counting mode 3**	**Phase counting mode 4**
High	Rising	Up	—	—	Up
Low	Falling	Up	—	—	Up
Rising	Low	Up	—	—	—
Falling	High	Up	Up	Up	—
High	Falling	Down	—	Down	Down
Low	Rising	Down	—	—	Down
Rising	High	Down	—	—	—
Falling	Low	Down	Down	—	—

Example of Operation:



Note: Values in parentheses ( ) indicate counter (TCNT) values.

3.5.2 Coding Example

Setting up TPU channel 1 in phasing counting mode 2:

```
// Stop TPU1 counter
com_tpu_control(TPU_CH1,TPU_STOP);
// Initialize TCNT
com_tpu_write_cnt_data(TPU_CH1,0);
// Specify phase counting mode 2
com_tpu_count_mode(TPU_CH1,TPU_PHASE_COUNT_2);
// Start TPU1 count operation
com_tpu_control(TPU_CH1,TPU_START);

////////////////////////////////////////////////////////////////////////////////
// The phase difference between TCLKA and TCLKB is detected and counting starts.    //
////////////////////////////////////////////////////////////////////////////////

// Execute the loop until an underflow or an overflow occurs.
while((com_tpu_read_satus(TPU_CH1) && 0x30) == 0){
  // Processing when the counter exceeds 100.
  }
}
```

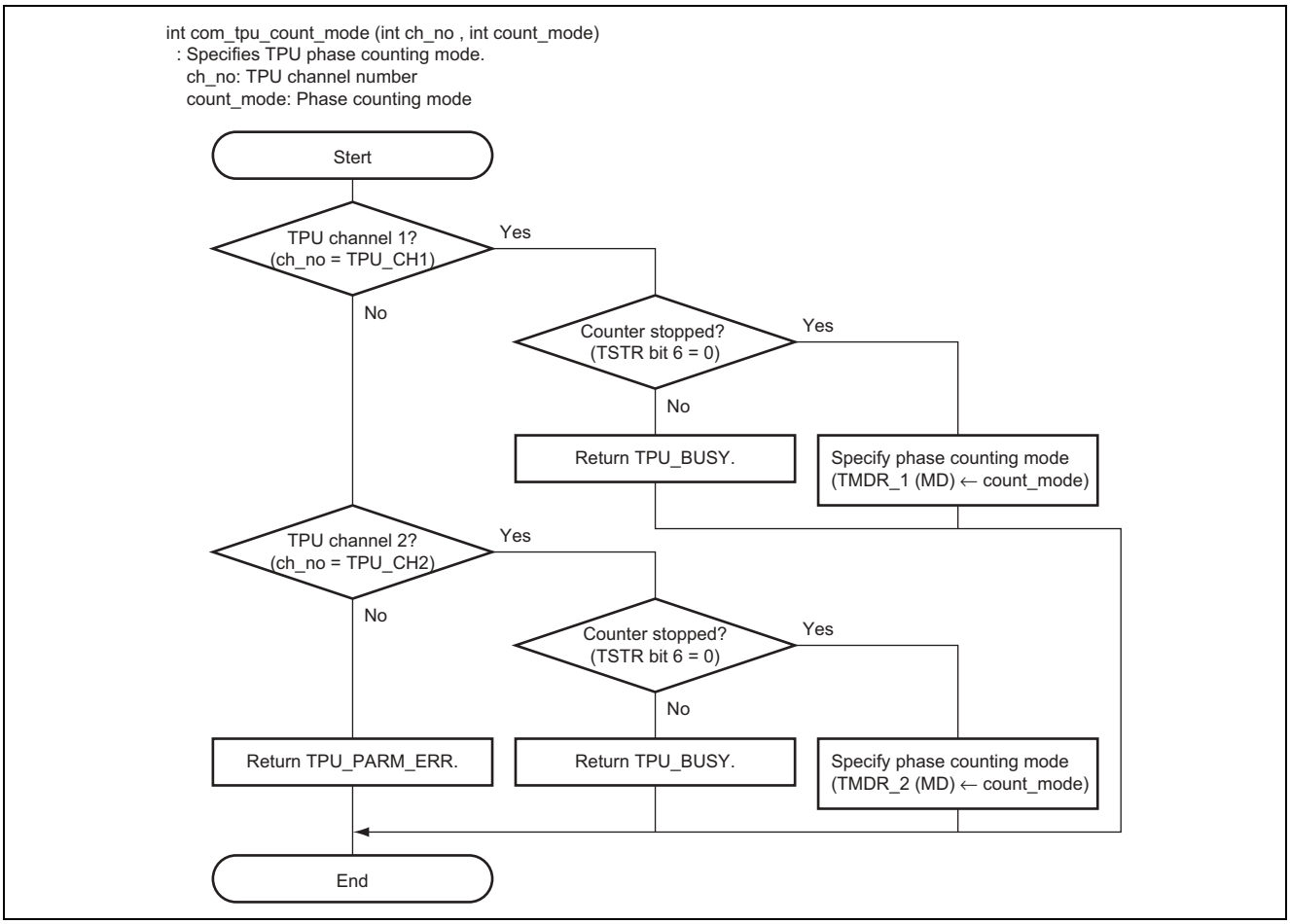
3.6 List of Registers Used

The internal registers of the H8 microcomputer used in the sample program are listed below. For detailed information, refer to the H8S/2215 Hardware Manual.

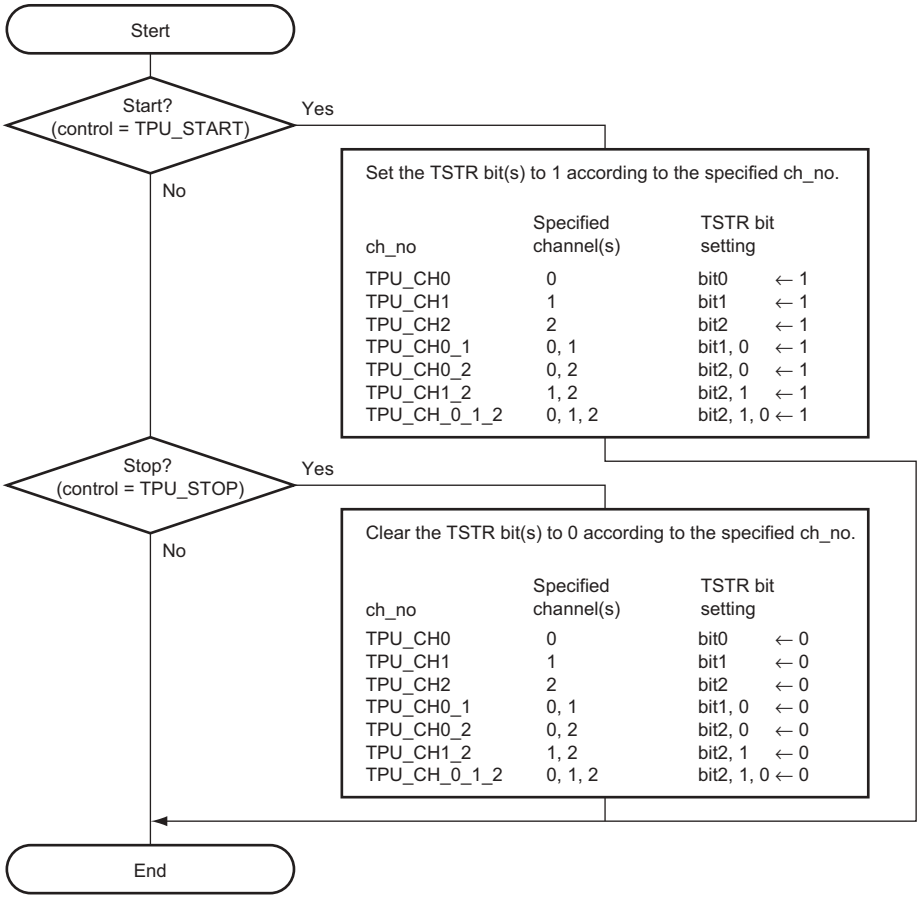
Name	Summary
Timer mode register (TMDR)	Specifies phase counting mode
Timer status register (TSR)	Indicates TCNT count direction Indicates underflow/overflow occurrence
Timer start register (TSTR)	Starts/stops TCNT operation
Timer counter (TCNT)	Timer counter

3.7 Flowchart

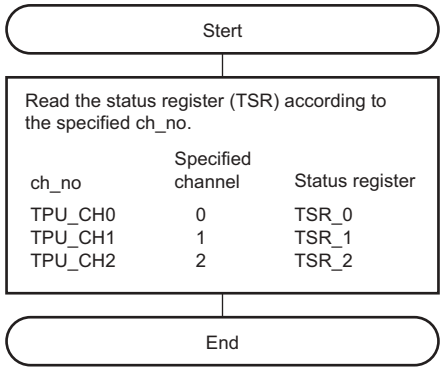
The sample program processing flow is shown below.



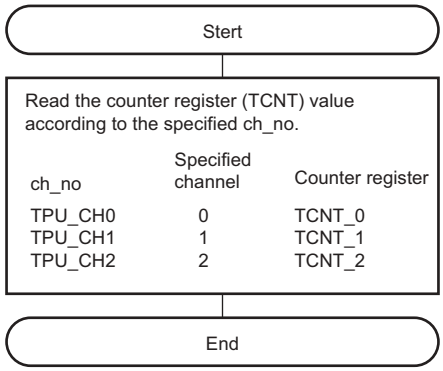
void com_tpu_control (int ch_no , int cntrol)
: Starts/stops the TPU
ch_no: TPU channel to be started or stopped (Multiple channel specification is allowed.)
control: Start/stop specification



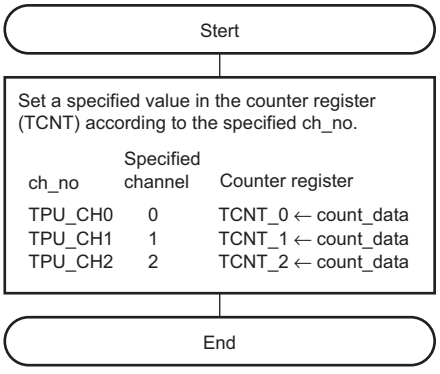
unsigned char com_tpu_read_status (int ch_no)
: Reads the TPU status register.
ch_no: TPU channel number



unsigned int com_tpu_read_cnt_data (int ch_no)
: Reads from the TPU counter register.
ch_no: TPU channel number



void com_tpu_write_cnt_data (int ch_no , unsigned char count_data)
: Sets a value to the TPU counter
ch_no: TPU channel number



4. Reference Document

- H8S/2215 Series Hardware Manual (published by Renesas Technology Corporation)

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Mar.16, 2004	—	First edition issued

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