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RENESAS

H8S/2200 Series

Serial Data Transmission in Asynchronous Mode

Introduction

Eight characters of 8-bit data are transmitted by the H8S/2215 to another H8S/2215 using the serial data transfer function in asynchronous mode.

Target Device

H8S/2215

Contents

1. Specifications

1. Eight characters (bytes) of data are transmitted using the serial data transfer function in asynchronous mode as shown in figure 1.
2. Transmit data communication format is specified for 8-bit data length, no parity and 1-bit stop bit.
3. The transmission bit rate is 38400 bps. Transmission ends when eight bytes of data have been transmitted.

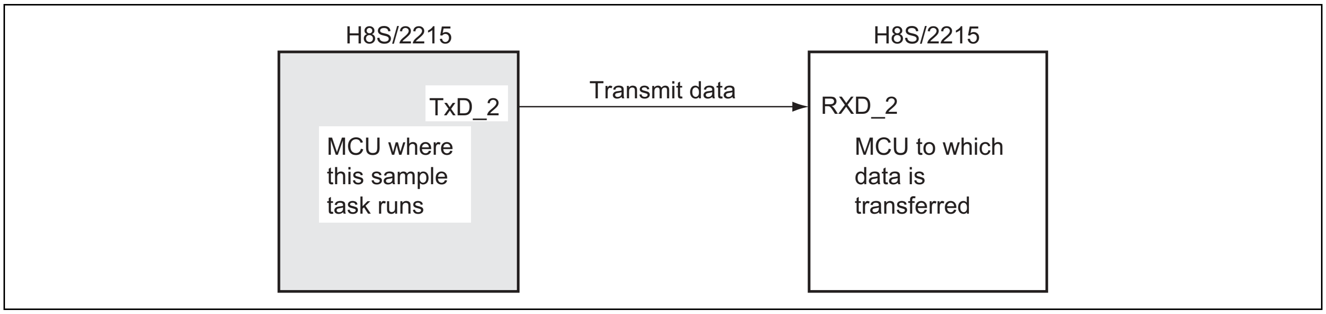


Figure 1 Serial Data Transmission in Asynchronous Mode

2. Description of Functions

1. Figure 2 shows a block diagram of the serial communication interface (SCI), and the following is the description for the block diagram:
   - The receive shift register (RSR) is a shift register that is used to receive serial data input from the RxD pin and convert it into parallel data. When one frame of data has been received, the data in RSR is automatically transferred to RDR. RSR cannot be directly accessed by the CPU.
   - The receive data register (RDR) is an 8-bit register that stores receive data. When one frame of data has been received, the received data in RSR is transferred to RDR, and then RSR is ready to receive the next data. RSR and RDR have a double-buffer structure, which enables continuous reception. Note that RDR should only be read once after RDRF in SSR is confirmed to be 1. RDR cannot be written to by the CPU. The initial value of RDR is H'00.
   - The transmit data register (TDR) is an 8-bit register that stores data for transmission. When TSR is detected to be empty, the data written to TDR is transferred to TSR and transmission starts. TSR and TDR have a double-buffer structure, which enables continuous transmission. If the next transmit data has already been written to TDR when transmission of one frame of data ends, it is transferred to TSR to continue transmission. TDR can always be read from or written to by the CPU, however, for reliable transmission, transmit data should only be written to TDR once after TDRE in SSR is confirmed to be 1. The initial value of TDR is H'FF.
   - The transmit shift register (TSR) is a shift register used to transmit serial data. Transmit data written to TDR is automatically transferred to TSR, and then sent to the TxD pin to perform serial data transmission. TSR cannot directly be accessed by the CPU.
   - The serial mode register (SMR) selects the communication format and internal baud rate generator's clock source.
   - The serial control register (SCR) controls transmission/reception operations and interrupts and selects a clock source for transmission/reception. Refer to the hardware manual for description of individual interrupt requests.
   - The serial status register (SSR) consists of SCI status flags and transmission/reception multiprocessor bits. TDRE, RDRF, ORER, PER and FER can be cleared but cannot be set by the CPU.
   - The bit rate register (BRR) is an 8-bit register that adjusts the bit rate. Since a baud rate generator is provided for each channel of SCI, different bit rates can be set for individual channels.

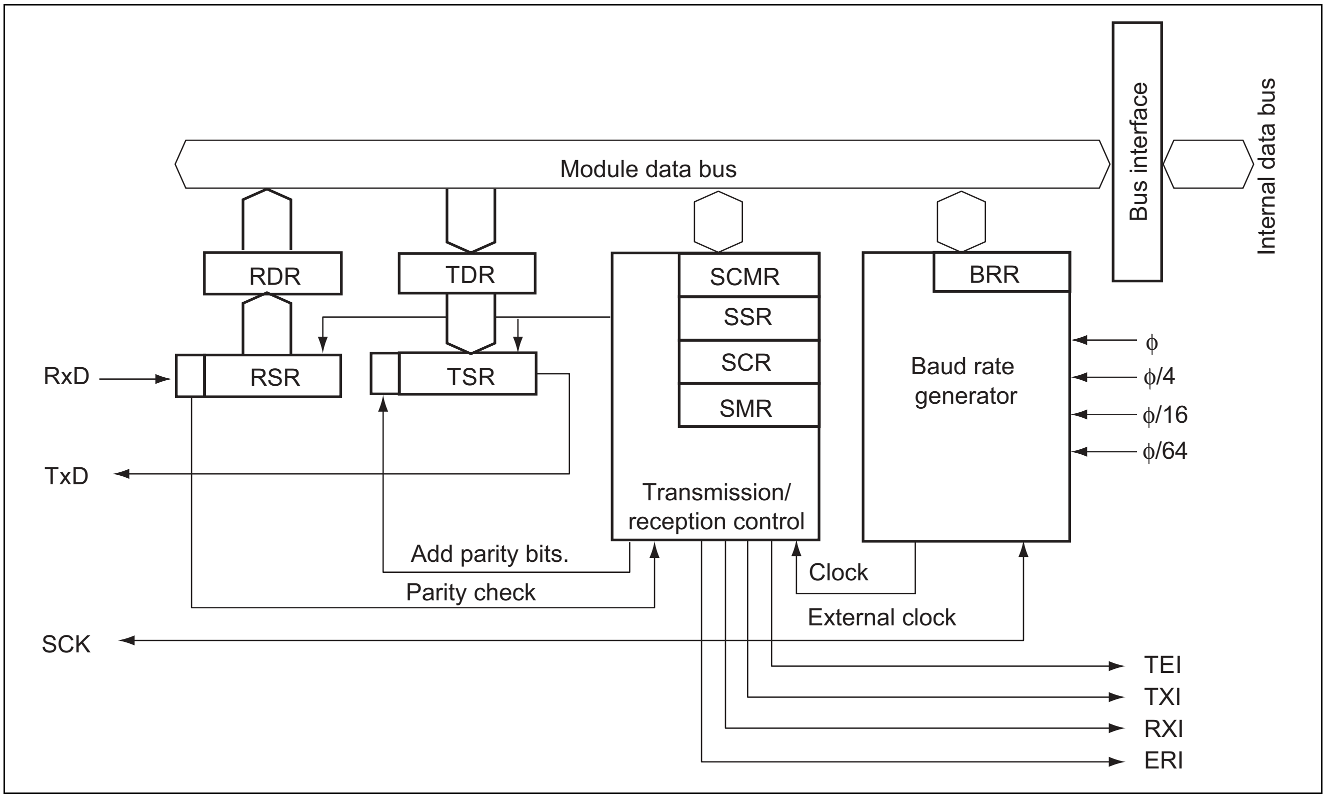


Figure 2 Block Diagram of Asynchronous Serial Data Transmission Function

2. Table 1 shows the assignment of functions used in this sample task.

Table 1 Assignment of Functions

Elements	Description
TSR	Register used to transmit serial data.
TDR	Register for storing transmit data.
RSR	Register used to receive serial data.
RDR	Register for storing received data.
SMR	Sets serial data communication format and clock source for the baud rate generator.
SSR	Status flags to indicate operation statuses of SCI.
BRR	Sets transmission/reception bit rate.
SCR	Enables transmission/reception and sets up TxD and RxD pins.
TxD	SCI transmit data output pin
RxD	SCI receive data input pin

3. Principles of Operation

Figure 3 illustrates asynchronous serial transmission operation of this sample task. A single frame for asynchronous serial communication consists of a low-level start bit, transmit/receive data, a parity bit and a high-level stop bit.

1. The SCI monitors the TDRE flag in SSR, and if the flag is 0, the SCI transfers the data in TDR to TSR.
2. After transferring data from TDR to TSR, the SCI sets the TDRE flag to 1 and starts transmission.
3. A frame is transmitted from the TxD pin from its start bit, and the SCI checks the TDRE flag at the timing of transmitting the stop bit. If TDRE = 0, the next data is transferred from TDR to TSR to repeat transmission.
4. If TDRE = 1, the TEND flag in SSR is set to 1. After the stop bit is sent, 1 is output to enter a mark state (high level).

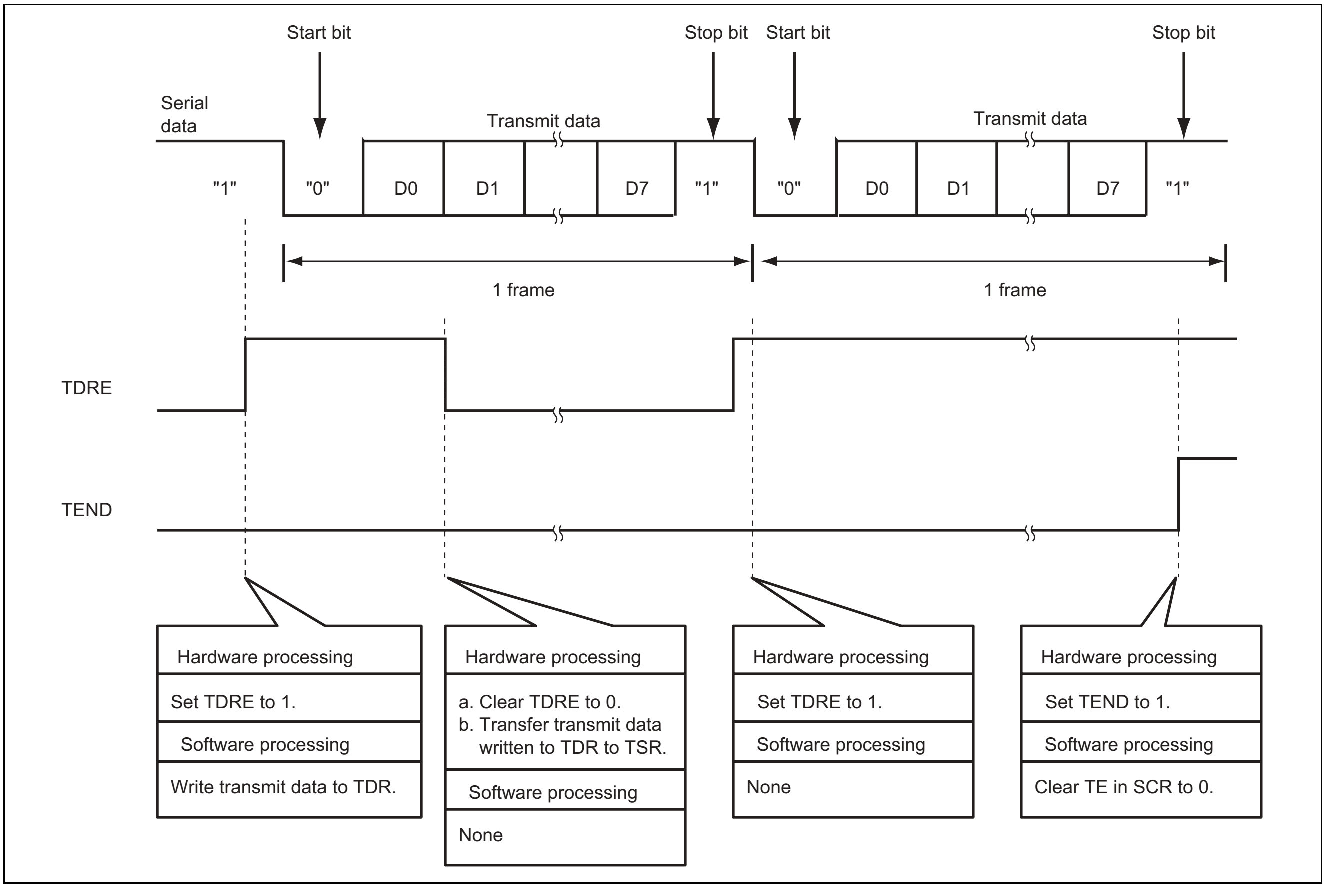


Figure 3 Operation of Serial Data Transmission in Asynchronous Mode

4. Description of Software

4.1 Module

Table 2 describes the module used in this sample task.

Table 2 Description of Modules

Module	Label	Function
Main routine	main	Sets the SCI up for asynchronous serial data transmission and ends after transmitting 8 bytes of data from TDR.

4.2 Arguments

Table 3 describes the arguments used in this sample task.

Table 3 Description of Arguments

Argument	Function	Used in	Data Length	Input/ Output
STD[0]to STD[7]	Data for asynchronous serial transmission	Main routine	1 byte	Input

4.3 Internal Registers

The SCI-related internal registers used in this sample task are described in table 4.

Table 4 Description of Internal Registers

Register		Function	Address	Setting
SMR_2	C/$\overline{A}$	Serial Mode Register_2 (Communication Mode) When C/$\overline{A}$ = 0, communication mode is set to asynchronous mode. When C/$\overline{A}$ = 1, communication mode is set to clocked synchronous mode.	H'FFFF88 Bit 7	0
	CHR	Serial Mode Register_2 (Character Length) When CHR = 0, data length is set to 8 bits in asynchronous mode. When CHR = 1, data length is set to 7 bits in asynchronous mode.	H'FFFF88 Bit 6	0
	PE	Serial Mode Register_2 (Parity Enable) When PE = 0, parity bit addition during transmission and parity check during reception are disabled in asynchronous mode. When PE = 1, parity bit addition during transmission and parity check during reception are enabled in asynchronous mode.	H'FFFF88 Bit 5	0
	O/$\overline{E}$	Serial Mode Register_2 (Parity Mode) When O/$\overline{E}$ = 0, even parity is selected. When O/$\overline{E}$ = 1, odd parity is selected.	H'FFFF88 Bit 4	0

Register		Function	Address	Setting
SMR_2	STOP	Serial Mode Register_2 (Stop Bit Length) When STOP = 0, the stop bit length is set to 1 bit in asynchronous mode. When STOP = 1, the stop bit length is set to 2 bits in asynchronous mode.	H'FFFF88 Bit 3	0
	MP	Serial Mode Register_2 (Multiprocessor Mode) When MP = 0, the multiprocessor communication function is disabled. When MP = 1, the multiprocessor communication function is enabled.	H'FFFF88 Bit 2	0
	CKS1 CKS0	Serial Mode Register_2 (Clock Select 1, 0) When CKS1 = 0 and CKS0 = 0, ϕ is selected as the clock source for the internal baud rate generator.	H'FFFF88 Bit 1 Bit 0	CKS1 = 0 CKS0 = 0
BRR_2		Bit Rate Register_2 When BRR = 12, the transmission bit rate is set to 38400 bps, which is set in relation to the baud rate generator's operating clock selected by CKS1 and CKS0 in SMR.	H'FFFF89	12
SCR_2	TE	Serial Control Register_2 (Transmit Enable) When TE = 0, transmission is disabled. When TE = 1, transmission is enabled.	H'FFFF8A Bit 5	0
	CKE1 CKE0	Serial Control Register_2 (Clock Enable 1, 0) When CKE1 = 0 and CKE0 = 0, an internal clock is selected as the clock source in asynchronous mode and SCK2 pin functions as an I/O port.	H'FFFF8A Bit 1 Bit 0	CKE1 = 0 CKE0 = 0
SSR_2	TDRE	Serial Status Register_2 (Transmit Data Register Empty) TDRE = 0 indicates that data has not been transferred from TDR to TSR and data cannot be written to TDR. TDRE = 1 indicates that data has been transferred from TDR to TSR and data can be written to TDR.	H'FFFF8C Bit 7	0
	TEND	Serial Status Register_2 (Transmit End) TEND = 0 indicates that transmission is in progress. TEND = 1 indicates that transmission has ended.	H'FFFF8C Bit 2	0
TDR_2		Transmit Data Register_2 8-bit register for storing transmit data.	H'FFFF8B	H'FF

- Bit rate register (BRR):
  BRR is an 8-bit register that sets the bit rate for transmission and reception in relation to the baud rate generator's operating clock selected by CKS1 and CKS0 in SMR. BRR can be read from or written to by the CPU at all times. Table 5 shows the principal bit rates and BRR settings in asynchronous mode with 16-MHz OSC.

Table 5 BRR Settings for Principal Bit Rates (Asynchronous Mode)

Bit Rate (bit/s)	1200	2400	4800	9600	19200	31250	38400
n	1	0	0	0	0	0	0
N	103	207	103	51	25	15	12
Error (%)	0.16	0.16	0.16	0.16	0.16	0.00	0.16

Notes: n: n = 0 when CKS1 and CKS0 = 0,0. n = 1 when CKS1 and CKS0 = 0,1.
N: BRR setting for the baud rate generator
For details, refer to the hardware manual.

4.4 ROM Usage

Table 6 describes the ROM usage in this sample task.

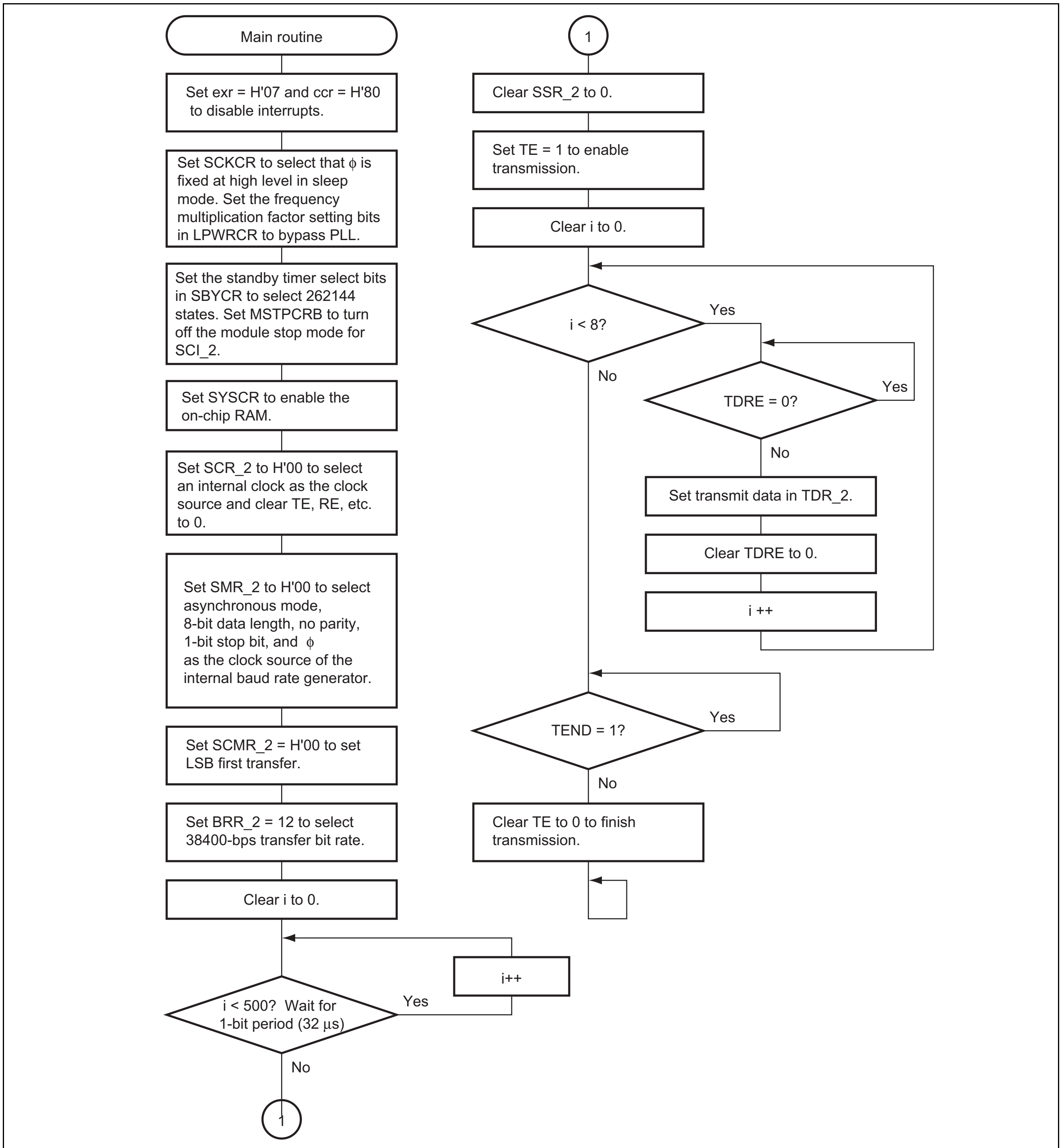
Table 6 Description of ROM

Label	Function	Address	Used in
STD[0]	Stores the first byte of data for asynchronous serial transmission.	H'00108C	Main routine
STD[1]	Stores the second byte of data for asynchronous serial transmission.	H'00108D	Main routine
STD[2]	Stores the third byte of data for asynchronous serial transmission.	H'00108E	Main routine
STD[3]	Stores the fourth byte of data for asynchronous serial transmission.	H'00108F	Main routine
STD[4]	Stores the fifth byte of data for asynchronous serial transmission.	H'001090	Main routine
STD[5]	Stores the sixth byte of data for asynchronous serial transmission.	H'001091	Main routine
STD[6]	Stores the seventh byte of data for asynchronous serial transmission.	H'001092	Main routine
STD[7]	Stores the eighth byte of data for asynchronous serial transmission.	H'001093	Main routine

Note: ROM addresses for STD[0] to STD[7] are allocated at the end of this program. They may not match the above addresses.

5. Flowchart

1. Main Routine



Revision Record

Rev.	Date	Description	
		Page	Summary
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