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April 1st, 2010
Renesas Electronics Corporation

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H8S/2200 Series

SCI Continuous Transmission and Reception

Introduction

Transmits and receives 48-byte data between the H8S/2215 and H8S/3687 in the clock synchronous mode. The DMAC is used.

Target Device

H8S/2215

Contents

1. Specifications

1. This sample task sets the SCI of the H8S/2215 in the clock synchronous mode and transmits and receives 48-byte data to and from the H8S/3687 continuously.
2. This sample task uses the DMAC to transfer data from memory to TDR and from RDR to memory without the intervention of the CPU.
3. The transmitting side becomes the clock master.

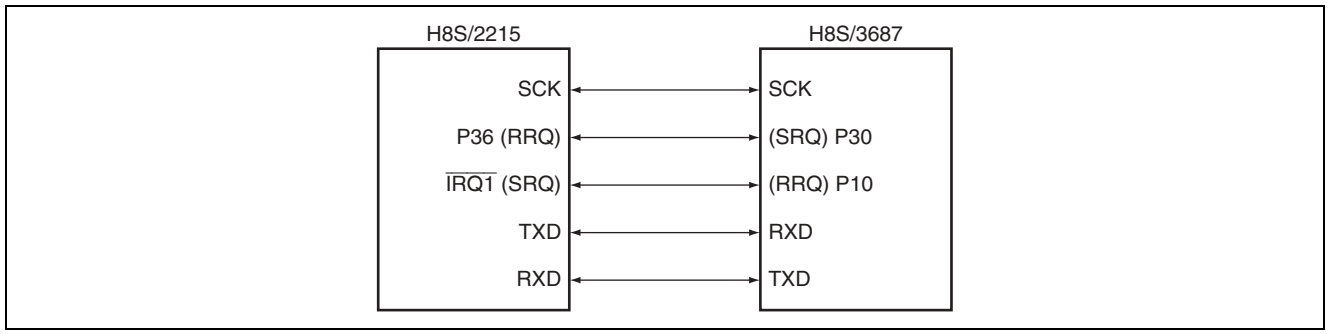


Figure 1 Block Diagram of the Clock Synchronous Mode SCI by the H8S/2215

2. Description of Functions

1. The H8S/2215 internal functions to be used by this sample task are shown in figure 2. This sample task performs high-speed serial communication, using the DMAC0A, DMAC0B and SCI1 as shown in figure 2.

   [Data Buffer]

   Buffer RAM for storing data to be transmitted and received.

   [DMAC0A]

   Operates in the sequential mode. Starts up by an SCI transmission completion interrupt and transfers the contents in the transmit data buffer to SCI.

   [DMAC0B]

   Operates in the sequential mode. Starts up by an SCI reception completion interrupt and transfers receive data to the reception data buffer.

   [SCI1]

   Transmits and receives serial data.

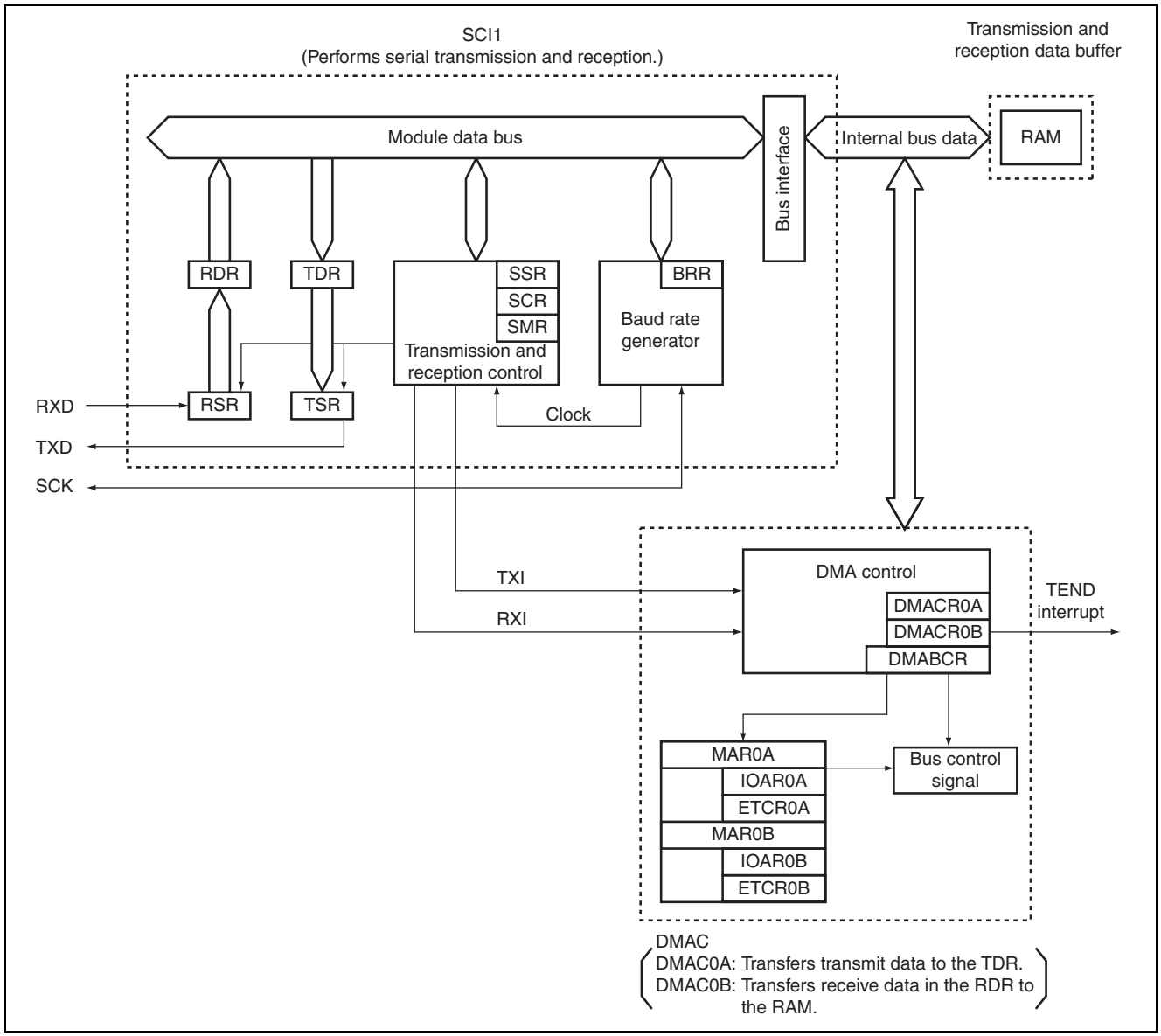


Figure 2 Block Diagram of Continuous Transmission and Reception

2. Function allocation of this sample task is shown in table 1. This sample task allocates the H8S/2215 functions as shown in table 1 to transfer transmit data and receive data without the intervention of the CPU.

Table 1 Assignment of Functions

Elements		Description
Interrupt controller	ISCRL	Selects interrupt generation at detection of a falling edge of IRQ1 input.
	IER	Enables an IRQ1 interrupt.
	ISR	Indicates the state of an IRQ1 interrupt request.
SCI1	SCK1	Transmits a transfer clock. During reception, receives a transfer clock.
	RXD1	Receive data input pin
	TXD1	Transmit data output pin
	SMR1	Sets the SCI in the clock synchronous mode mode.
	SCR1	Sets transmission and reception.
	SSR1	Indicates the states of reception and transmission.
	RDR1	Stores received data.
	TDR1	Sets data to be transmitted.
	BRR1	Sets the transfer rate.
PORT 3	P3DDR	Sets I/O of port 3.
	P3DR	Transmits RRQ.
DMAC	DMABCR	Controls operation of each channel.
	DMACR0A	Controls DMAC0A operation.
	MAR0A	Sets the transfer source address (data buffer).
	IOAR0A	Sets the transfer destination address (TDR).
	ETCR0A	Sets the transfer count.
	DMACR0B	Controls DMAC0B operation.
	MAR0B	Sets the transfer destination address (data buffer).
	IOAR0B	Sets the transfer source address (RDR).
	ETCR0B	Sets the transfer count.

3. Principles of Operation

1. Data Transmission

The principles of operations used during data transmission is shown in figure 3. This sample task controls the I/O port and the clock synchronous mode SCI at the timing shown in figure 3 to make an interface.

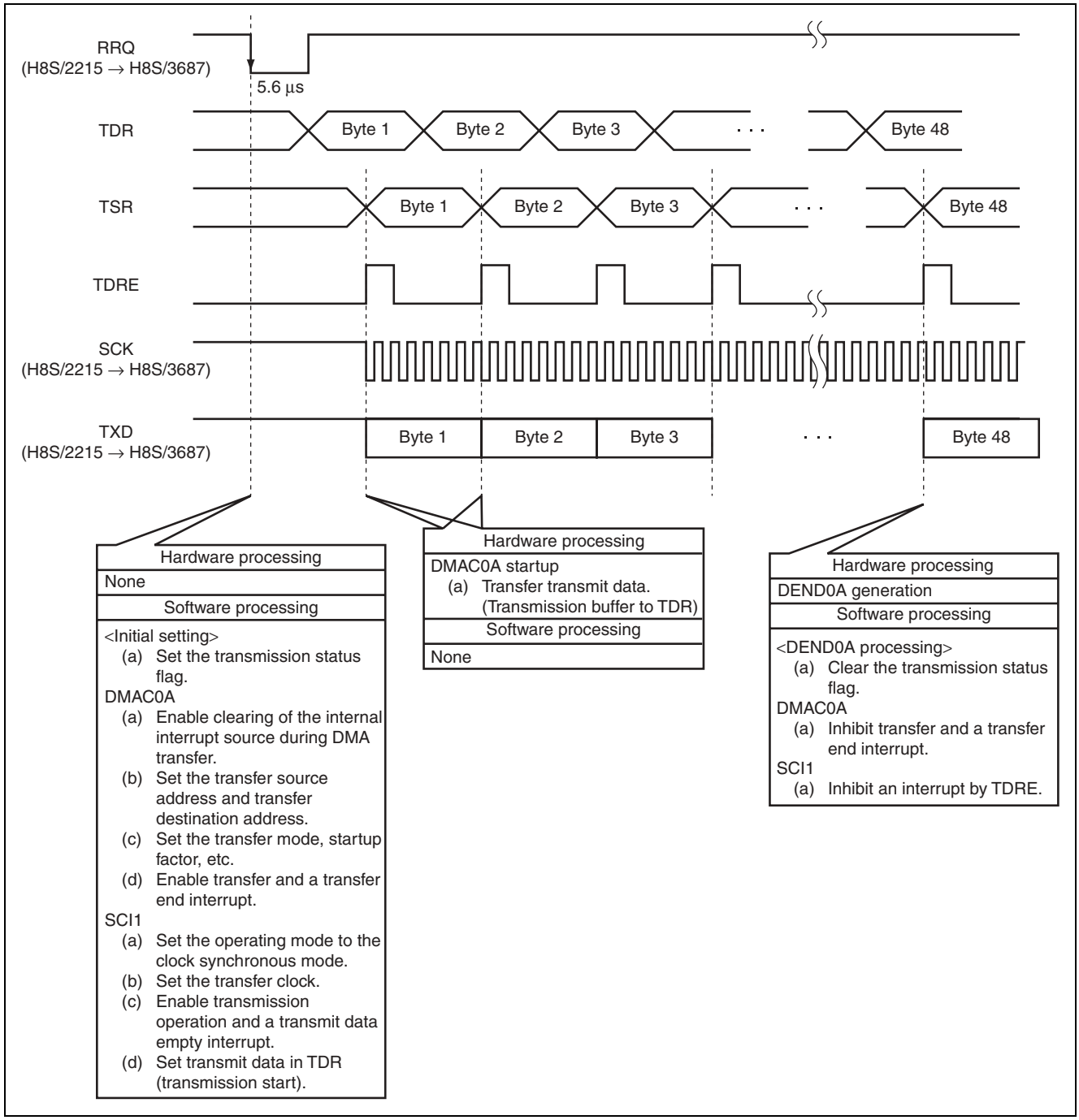


Figure 3 Principles of Operations Used of Data Transmission

2. Data Reception

The principles of operations used during data reception are shown in figure 4. This sample task controls the I/O port and the clock synchronous mode SCI as shown in figure 4 to make an interface.

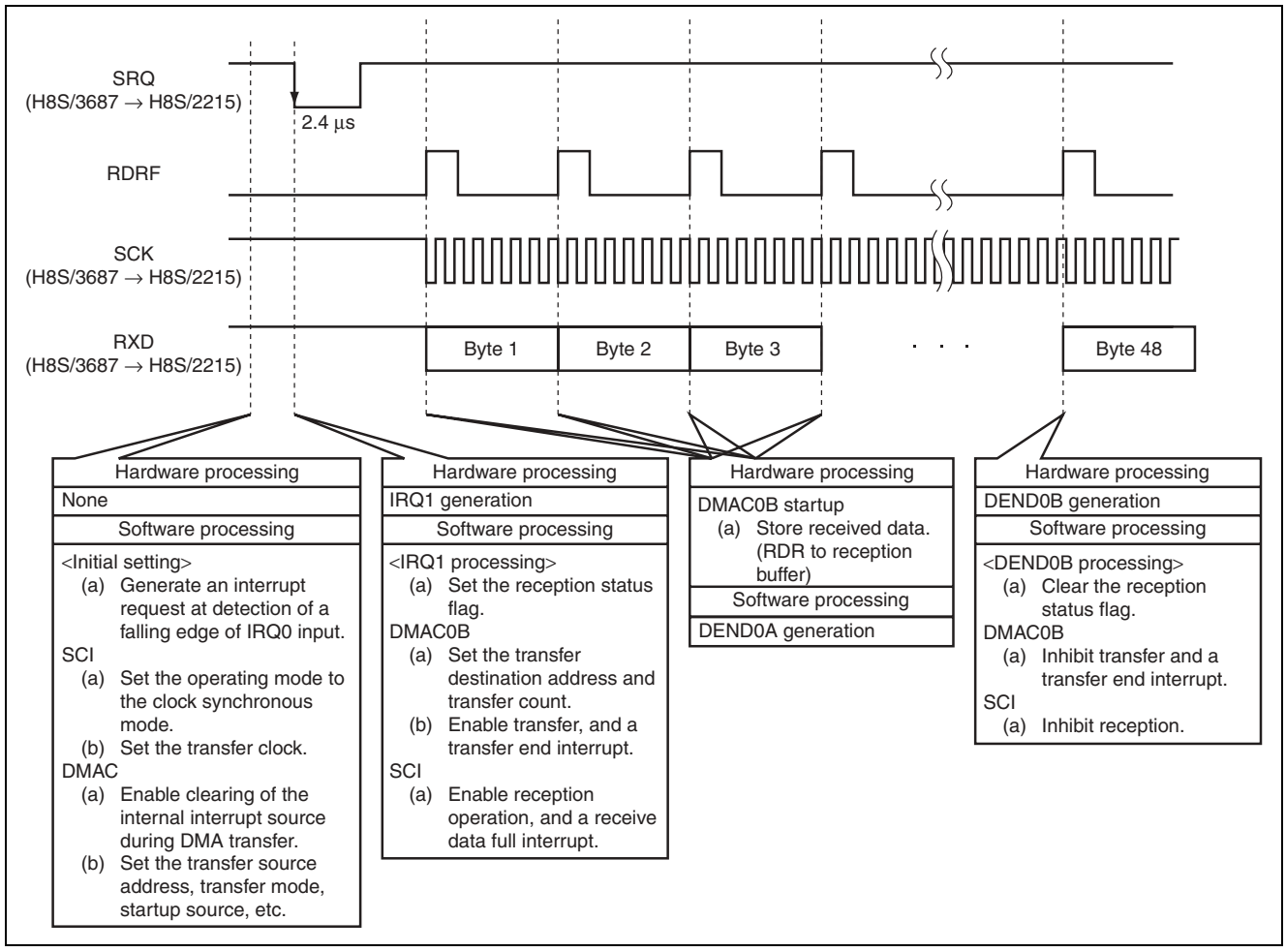


Figure 4 Principles of Operations Used of Data Reception

4. Description of Software

1. Description of Modules

Module Name	Label Name	Function
Main routine	hiscimn	Performs initial setting of the I/O port, SCI, and DMAC.
Data transmission	txstart	Enables the DMAC to transfer data and starts SCI transmission operation.
Data reception	rxstart	Starts up by an IRQ1 interrupt, enables DMAC transfer, and starts reception operation of the SCI.
Transmission completion	txend	Starts up by a DMAC0A transfer end interrupt, clears stat_tx and inhibits transmission processing.
Reception completion	rxend	Starts up by a DMAC0B transfer end interrupt, clears stat_rx and inhibits reception processing.

2. Description of Arguments

Register Name	Function	Data Length	Used in	I/O
stat_tx	Flag indicating transmission in progress	unsigned char	Data transmission Data reception	Output Input
stat_rx	Flag indicating reception in progress	unsigned char	Data transmission Data reception	Input Output

3. Internal Registers Used

Implemented Function	Register Name	Function
SCI1	SMR1	Sets the SCI as follows: • Sets the SCI operating mode to the clock synchronous mode mode. • Sets the clock source of the baud generator to ϕ.
	SCR1	Sets the SCI as following during transmission and reception respectively: Transmission: Enables a transmit data empty interrupt. Enables transmission. Sets the SCK pin to output a synchronizing clock. Reception: Enables a receive data full interrupt. Enables reception. Sets the SCK pin to input a synchronizing clock.
	SSR1	Transmission: Clears TDRE to start transmission. Reception: Clears RDRF to start reception.
	RDR1	Stores received data.
	TDR1	Sets data to be transmitted.
	BRR1	Sets the transfer rate.
DMAC	DMABCR	Sets the DMAC0A and DMAC0B as follows: • Sets transfer mode to short-address mode. • Enables an internal interrupt source to be cleared during DMA transfer. • Enables data transfer and a transfer end interrupt.
	DMACR0A	Sets the DMAC0A as follows: • Sets the data size to the byte size. • Sets increment of MAR. • Sets data transfer in the sequential mode. • Sets the data transfer direction (ch0A: MAR to IOAR) • Sets an SCI transmission completion interrupt as the startup source.
	MAR0A	Sets the transmission buffer address.
	IOAR0A	Sets the TDR address.
	ETCR0A	Sets the transfer count.
	DMACR0B	Sets the DMAC0B as follows: • Sets the data size to the byte size. • Sets increment of MAR. • Sets data transfer in the sequential mode. • Sets the data transfer direction (ch0B: IOAR to MAR) • Sets an SCI reception completion interrupt as the startup source.
	MAR0B	Sets the reception buffer address.
	IOAR0B	Sets the RDR address.
	ETCR0B	Sets the transfer count.
I/O	P3DDR	Sets I/O of port 3.
	P3DR	Transmits RRQ.

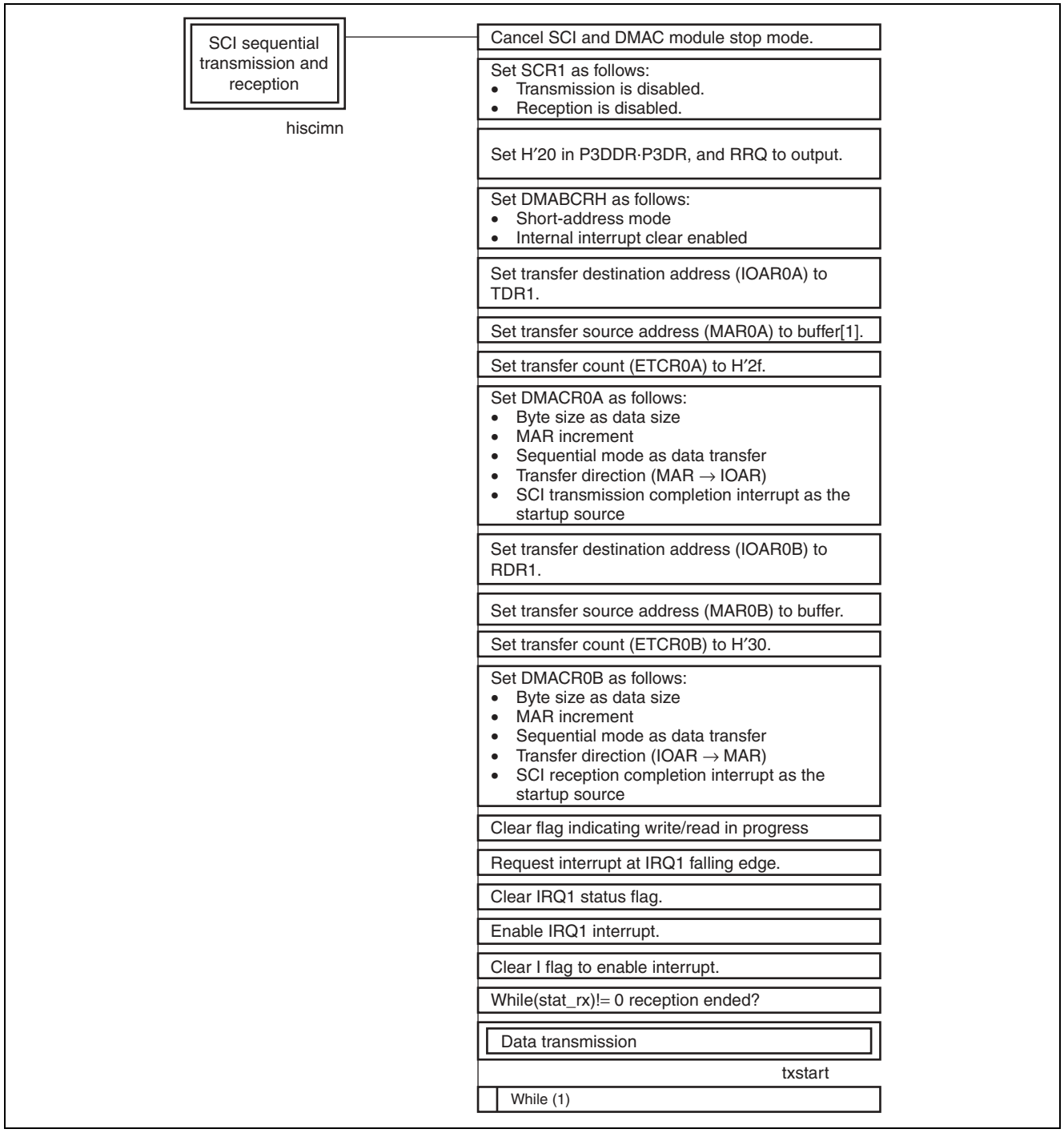
Implemented Function	Register Name	Function
Interrupt controller	IER	Enables an IRQ1 interrupt.
	ISCR	Sets an interrupt request to be generated at detection of a falling edge of IRQ1.
	ISR	Indicates the IRQ1 input state.
MSTPCR		Cancels the SCI and DMAC module stop mode.

4. RAM Usage
   Table below describes RAM usage in this sample task.

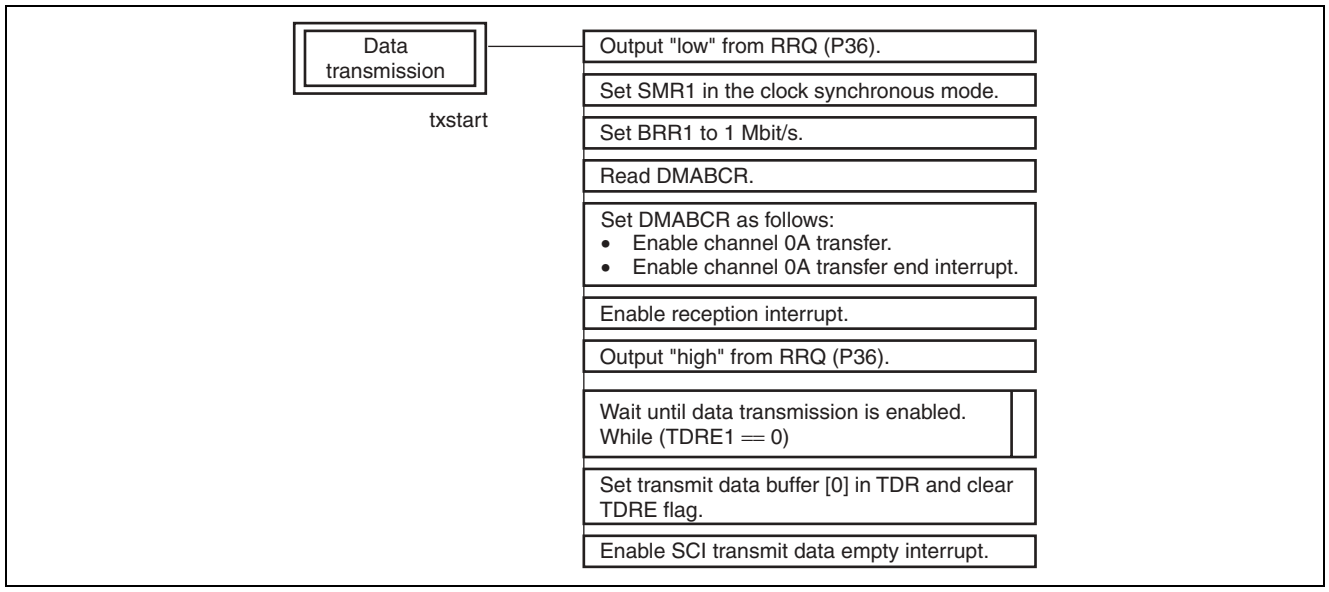
Register Name	Function	Data Length	Used in
buffer	Stores transmit and received data.	48 bytes	Data transmission

5. PAD

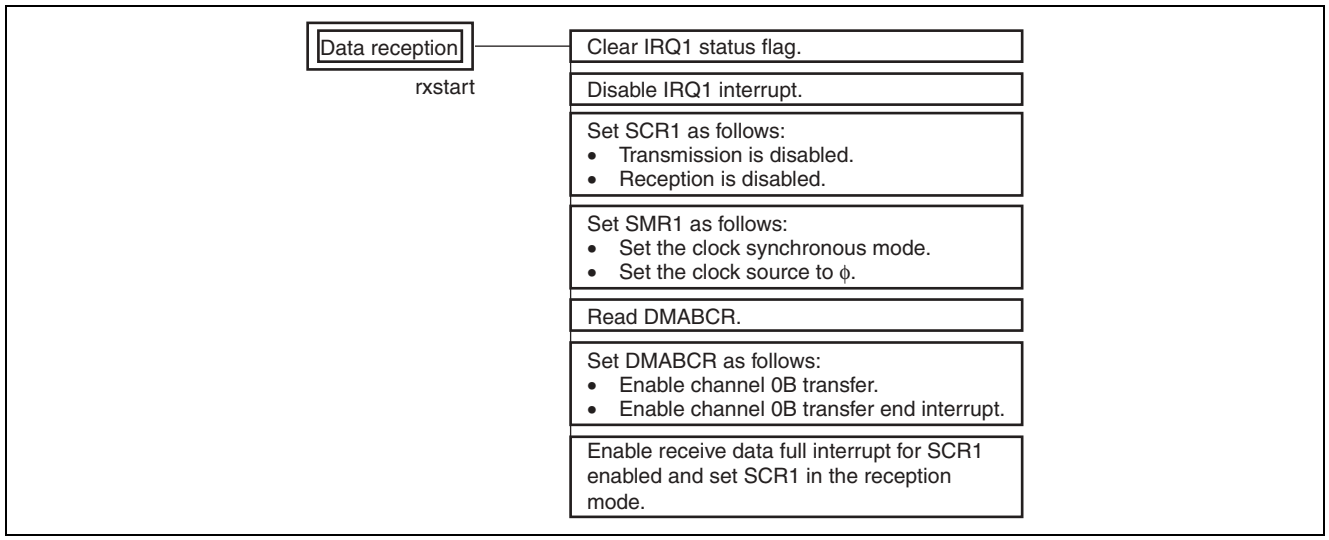
1. Main Routine



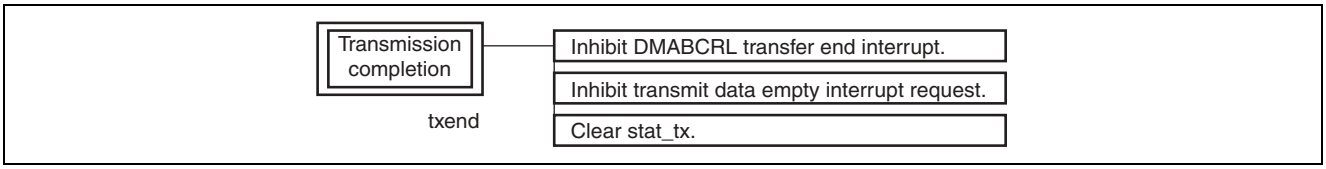
2. Data Transmission



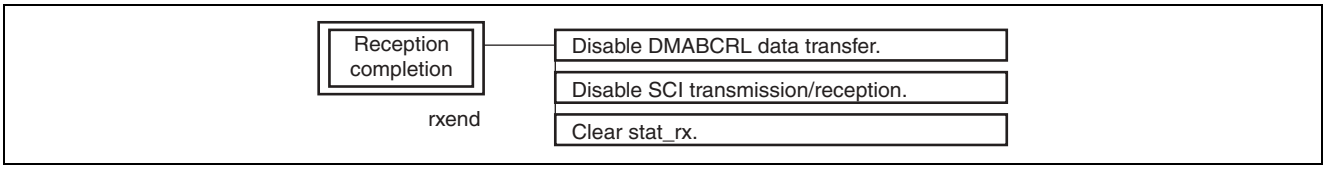
3. Data Reception
An interruption occurs when IRQ1 sets the LOW level, and performs the following.



4. Transmission Completion
   An interruption occurs when the data transmission of DMAC channel 0A completes, and performs the following.



5. Reception Completion
   An interruption occurs when the data reception of DMAC channel 0B completes, and performs the following.



Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Mar.16.04	—	First edition issued

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