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H8S / 2200 Series

Pulse-Train Output

Introduction

Pulses with duty ratio of 50% is output using the 16-bit counter based on the cyclic data set in the RAM

Target Device

H8S / 2215

Contents

1. Specifications.....	2
2. Description of Module Usage.....	3
3. Principles of Operation.....	4
4. Software Description.....	5
5. PAD.....	6

1. Specifications

- (1) Outputs a pulse train with a 50% duty cycle as shown in figure 1. The period is set by cycle data in RAM.
- (2) When the microcomputer is operating at 20 MHz, the cycle of the pulse for output can be set as desired to values between 100 ns and 3.27 ms.

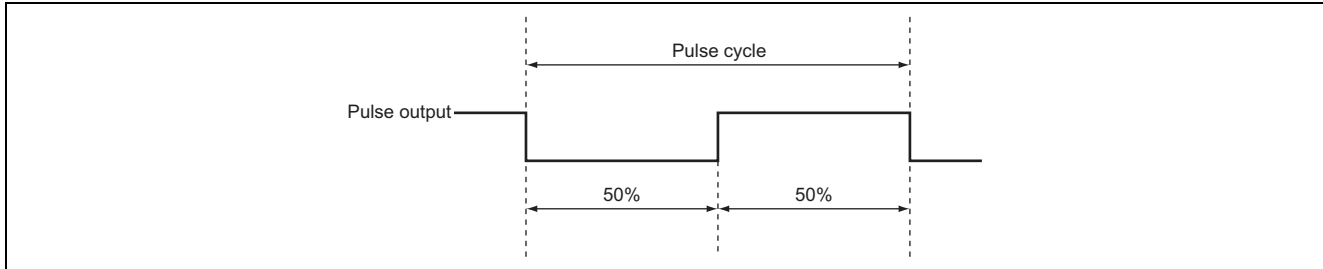


Figure 1 Example of Pulse Output

2. Description of Module Usage

(1) TPU0 is used to output a pulse with duty cycle of 50%.

(a) A block diagram of TPU0, the timer used in this application, is given in figure 2.

The following functions of the TPU0 are used:

- Automatic output of a pulse by hardware with no software intervention (output compare)
- Clearing of the counter (counter clear) on a compare-match
- Inversion of the output for every occurrence of a compare match (toggled output)

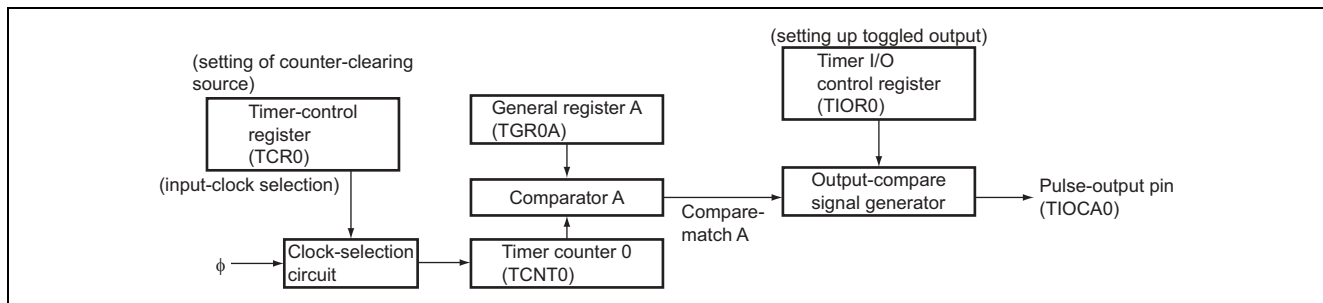


Figure 2 Configuration for Pulse-Train Output

(2) Usage features in this sample task is described in table 1. Pulse-train output is achieved by using functional elements as described in the table.

Table 1 Function Assignments

Element	Description
TCR0	Selects the clock and counter-clearing sources for input to TCNT0
TIOCA0	Outputs the pulse train
TIOR0	Sets the pulse output
TGR0A	Sets the 1/2-cycle period for the pulse train

3. Principles of Operation

Task operation is depicted in figure 3. The pulses are output through a combination of hardware and software processing by the H8S / 2215.

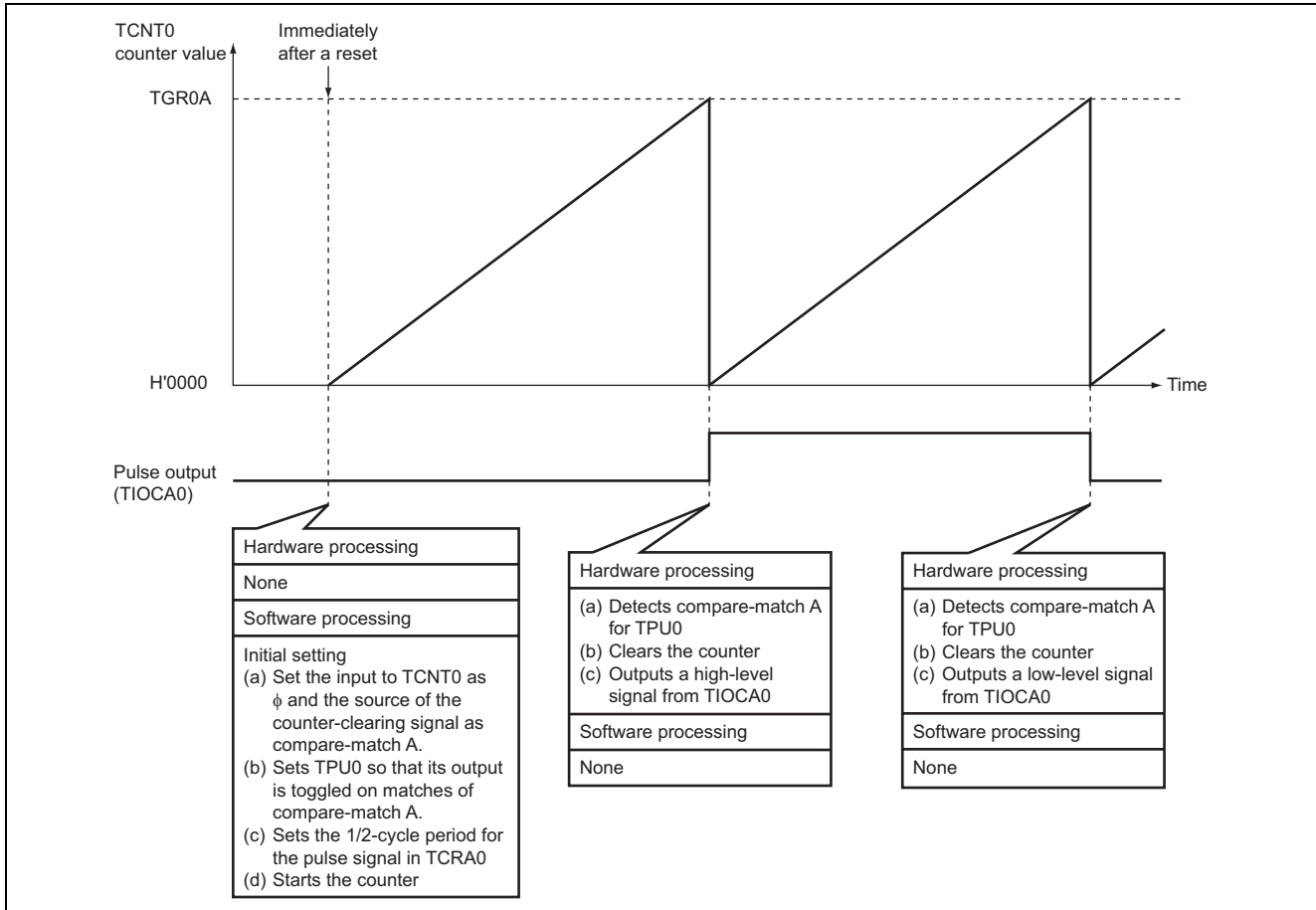


Figure 3 Principle of Pulse-Output Operation

4. Software Description

(1) Function

Function	Label	Description
Main routine	poutmn	Makes initial settings of TPU and RAM, and outputs a pulse

(2) Arguments

Label	Description	Data Length	Used in	I/O
pul_cyc	Sets the timer value which is equivalent to the pulse cycle. The pulse cycle is obtained by the following expression: Pulse cycle (ns) = Timer value x ϕ period (50 ns in operation at 20 MHz)	Unsigned short	Main routine	Input

(3) Internal Registers

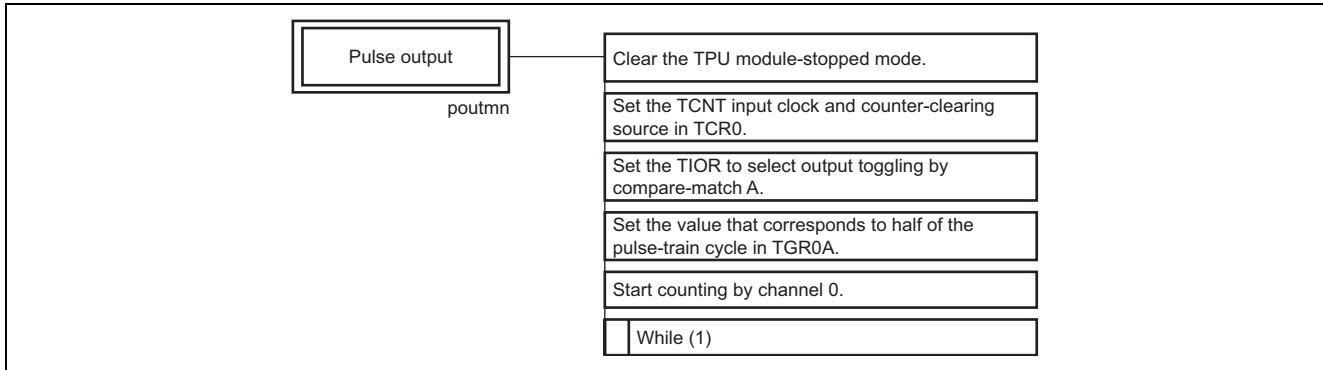
Register	Description	Used in
TSTR	Enables and disables the timer counter	Main routine
TCR0	Selects the clock for input to TCNT and the source of the counter-clearing signal	Main routine
TIOR0	Configures output-pulse behavior in response to compare-match A	Main routine
TGR0A	Sets the 1/2-cycle period for the output pulse	Main routine
MSTPCR	Clears the TPU module-stopped mode	Main routine

(4) RAM Usage

Internal RAM other than that for argument-storage is not used

5. PAD

(1) Main routine



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16 '04	—	First edition issued

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