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Renesas Electronics Corporation

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H8S/2200 Series

One-Shot Pulse Output

Introduction

Outputs a one-shot pulse, synchronizing with a falling edge of an external signal. The delay time from the falling edge and pulse width can be varied.

Target Device

H8S/2215

Contents

1. Specifications

1. As shown in figure 1, this function outputs a one-shot pulse, synchronizing with the falling edge of the external signal.
2. The delay time from the falling edge of the external signal and pulse width can be changed within the following ranges:

   1µs ≤ delay time < reference pulse cycle – pulse width

   50ns ≤ pulse width < reference pulse cycle – delay time
3. The reference pulse frequency can be entered from 62.5Hz.

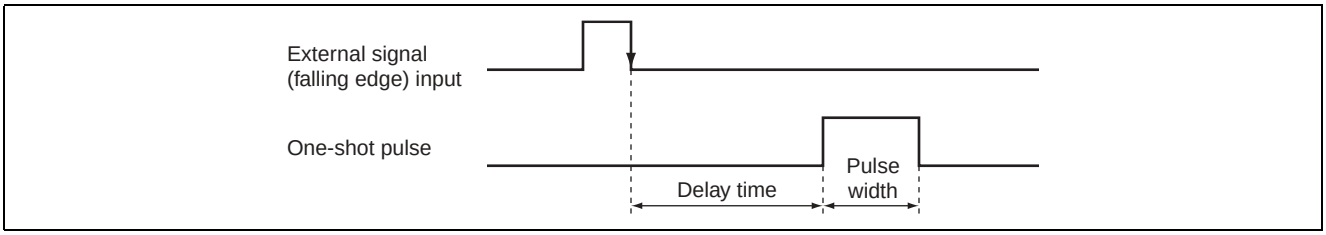


Figure 1 One-Shot Pulse Output

2. Description of Functions

1. This sample task outputs a one-shot pulse by using DMAC0A, DMAC0B, and TPU0.
   A. The block diagram of internal functions used in this sample task is shown in figure 2.
      In this sample task, a one-shot pulse is output by using the following TPU and DMAC functions:

   [TPU]
   - Function that transfers the buffer register contents to a general register at occurrence of compare match. (Buffer operation)
   - Function that can set an output/input capture register for each register.
   - Function that can clear a counter by input capture.

   [DMAC]
   - Function that starts up DMAC at occurrence of TPU input capture.

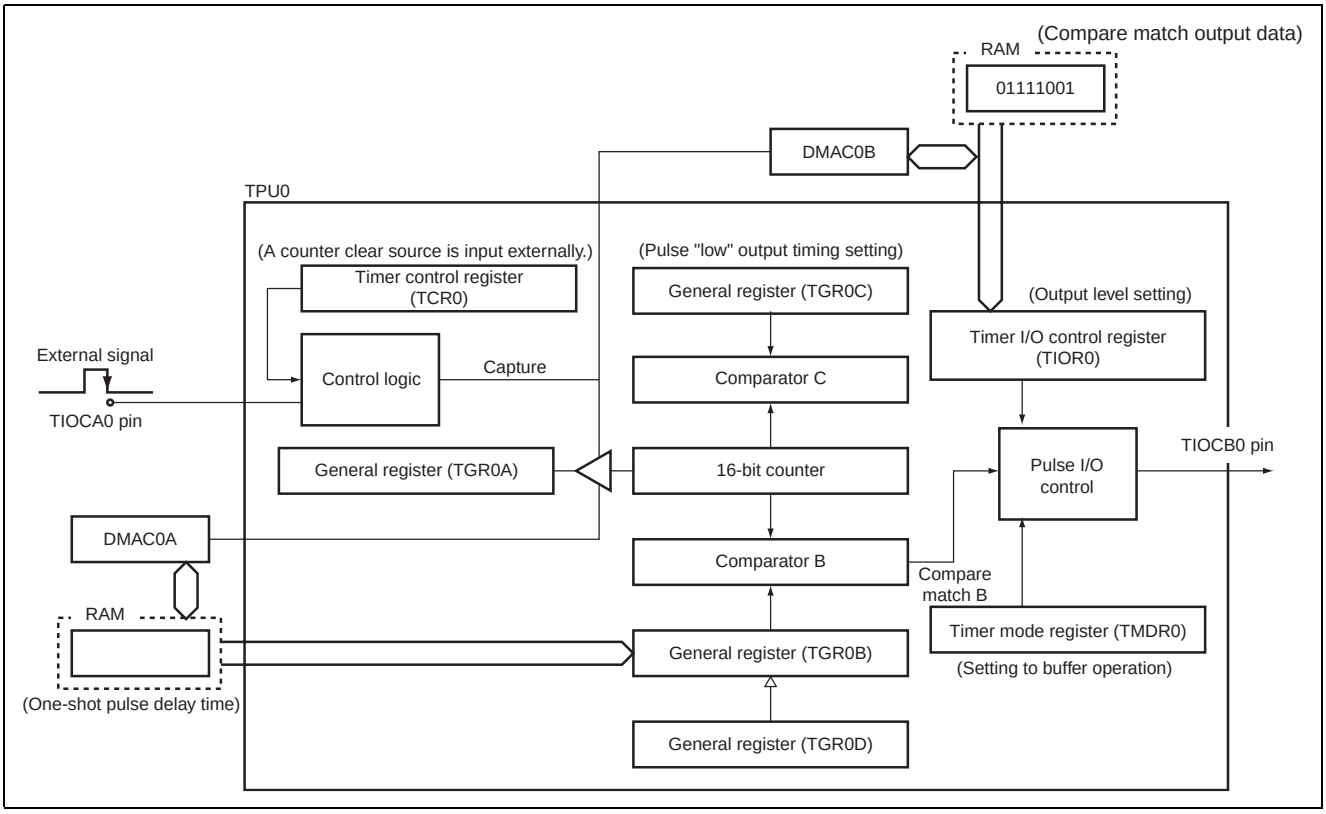


Figure 2 Block Diagram of One-Shot Pulse Output

2. Function allocation of this sample task is shown in table 1. This sample task allocates H8S/2215 functions as shown in table 1 to output a one-shot pulse.

Table 1 Assignment of Functions

Elements		Description
TPU0	TCR0	Sets a counter clear source.
	TIER0	Enables an interrupt by TGI0C.
	TIOR0	Sets TGR0A as the capture register and TGR0B and TGR0C as compare match registers.
	TMDR0	Sets buffer operation.
	TGR0B	Sets a one-shot pulse delay time.
	TGR0C	Sets an output prohibit timing value of one-shot pulse.
	TGR0D	Sets a reset timing value of one-shot pulse.
	TIOCA0	Inputs the external signal.
	TIOCB0	Outputs a one-shot pulse.
DMAC	DMABCRH, L	Controls operations of each DMAC channel.
	DMACR0A, B	Sets the transfer size, mode, and startup source of each channel.
	MAR0A, B	Sets a transfer source address.
	IORA0A, B	Sets a transfer destination address.
	ETCR0A, B	Sets a transfer count.

3. Principles of Operation

The principles of operations used are shown in figure 3. As shown in figure 3, a one-shot pulse is output by H8S/2215 hardware and software processing.

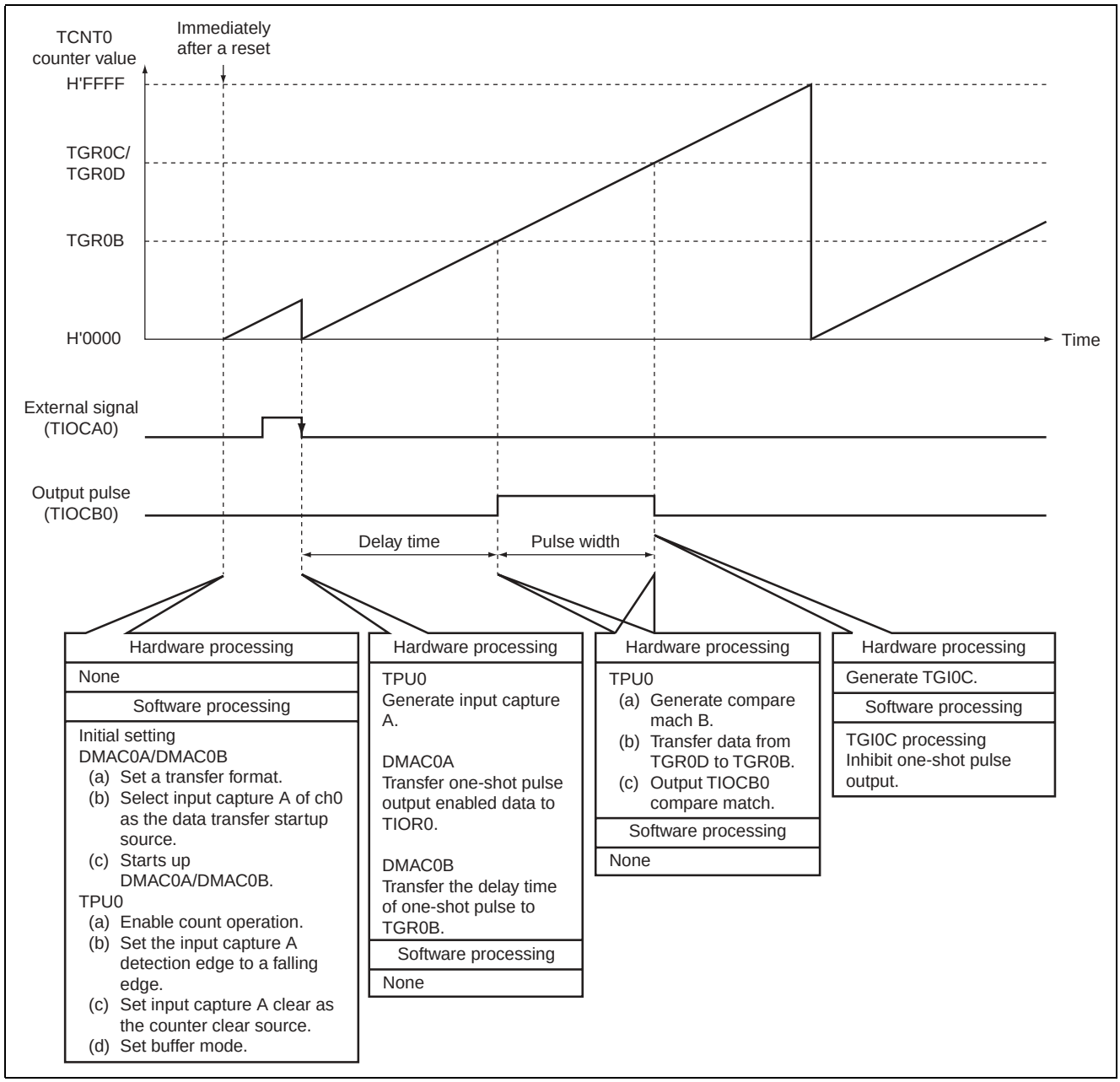


Figure 3 Principles of Operations Used of One-Shot Pulse Output

4. Description of Software

1. Description of Modules

Module Name	Label Name	Function
Main routine	ONEMN	Sets the delay time and pulse width in TGR0B and TGR0D, and a one-shot pulse reset value to TGR0C to output a one-shot pulse.
Pulse output inhibition	POUTDLE	Inhibits pulse output.

2. Description of Arguments

Label Name	Function	Data Length	Used in	I/O
set_dly	Sets a timer value that governs the delay time of one-shot pulse. The delay time is obtained by the following expression: Delay time (ns) = timer value × ϕ cycle (62.5 ns during 16-MHz operation)	unsigned short	Main routine	Input
one_rst	Sets a timer value that governs the reset timing of one-shot pulse. The reset timing is obtained by the following expression: Pulse reset timing (ns) = timer value × ϕ cycle (62.5 ns during 16-MHz operation)	unsigned short	Main routine	Input
io_cntr	Sets one-shot pulse output enabled data. (A falling edge is set as the input capture A detection edge and compare match B is toggled during output.)	unsigned char	Main routine	Output

3. Description of Internal Registers Used

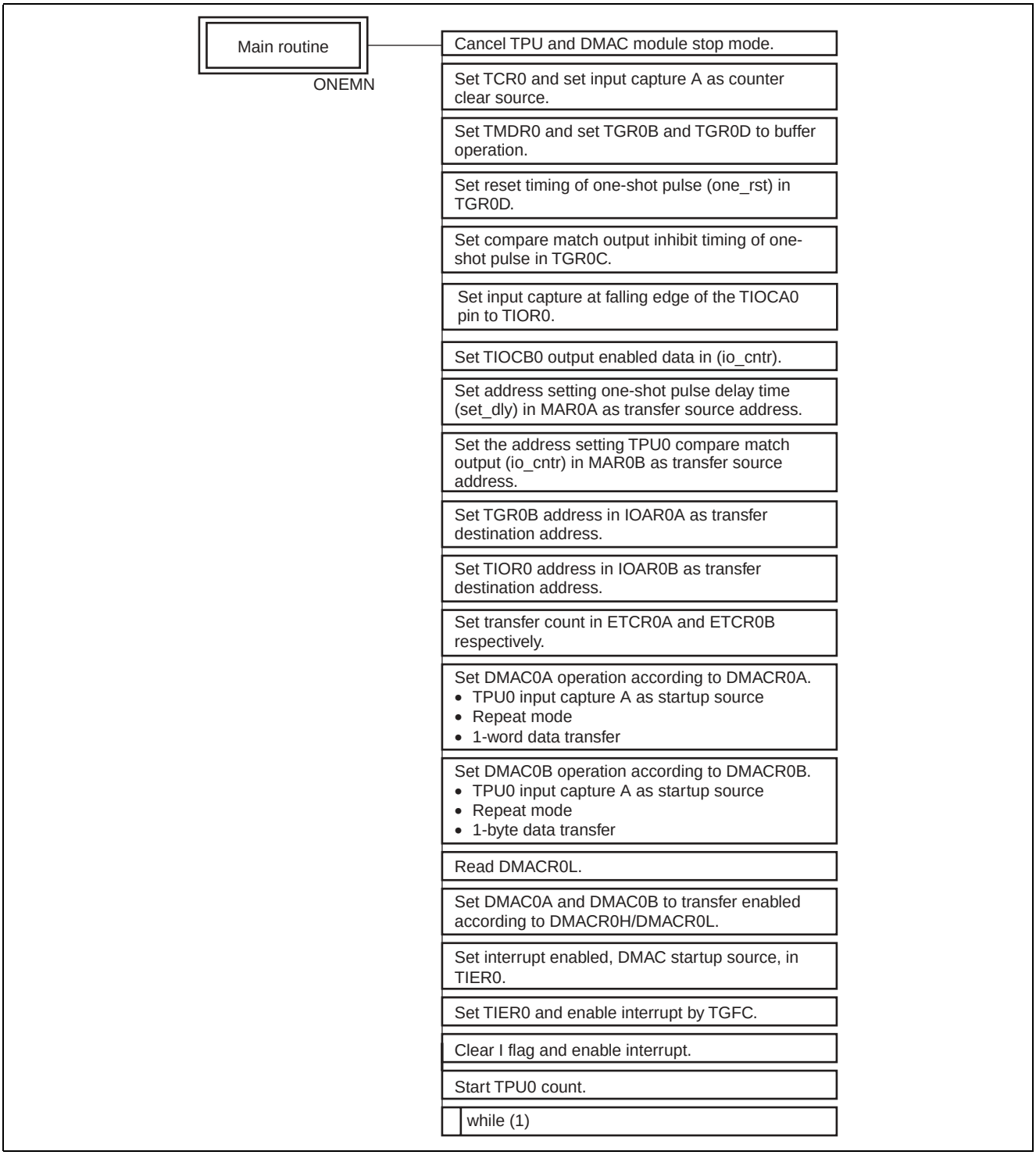
Register Name		Function	Used in
TPU0	TSTR	Selects operation/stop of the timer counter.	Main routine
	TMDR	Sets TGR0B and TGR0D to buffer operation.	
	TCR0	Sets a clock to be input to TCNT and a counter clear source.	
	TIOR0	Detects a falling edge of an input pulse.	
		Sets a level to be output from TIOCB0 at occurrence of compare match B.	Pulse output inhibition
	TIER0	Enables an interrupt by TGI0C.	Main routine/ pulse output inhibition
	TSR0	Indicates occurrence of compare match by TGR0B.	Main routine
	TGR0B	Sets the delay time of one-shot pulse.	
	TGR0C	Sets a pulse output inhibit timing value of one-shot pulse.	
	TGR0D	Sets a reset timing value of one-shot pulse.	
DMAC	DMABCR0 DMACR0 A / B	Sets the operation of each DMAC channel.	
	MAR0 A / B	Sets the address of data to be transferred to each register.	
	IOAR0 A / B	Sets the transfer destination register address of each channel.	
	ETCR0 A / B	Sets the transfer count of each channel.	
MSTPCR		Cancels the TPU and DMAC module stop mode.	

4. RAM Usage

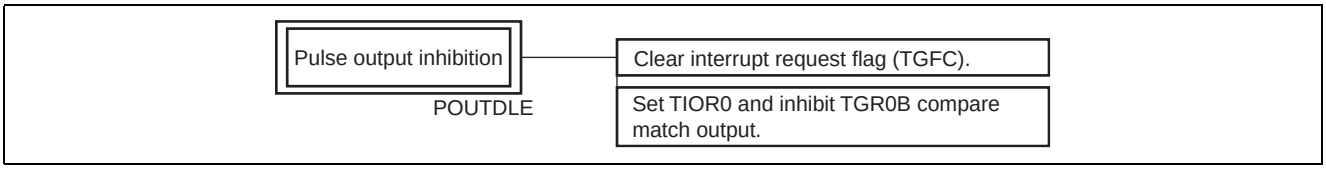
This sample task uses only arguments.

5. PAD

1. Main Routine



2. Pulse Output Inhibition



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16.04	—	First edition issued

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