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Renesas Electronics Corporation

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H8S / 2200 Series

Long-Cycle Pulse Output

Introduction

A pulse with variable cycle period in the range from 6.55 ms to 214.7 s is output using the 32-bit counter. The duty rate is variable from 0 to 100%.

Target Device

H8S / 2239

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1. Specifications

- (1) Performs 32-bit counting and outputs a long-cycle pulse with a variable duty cycle (see figure 1).
- (2) The duty rate can be set to any value from 0 to 100%, with a resolution of 1/65535.
- (3) In operation at 20 MHz, the pulse period can be set to any value between 6.55 ms and 214.7 s, in 3.27-ms units.

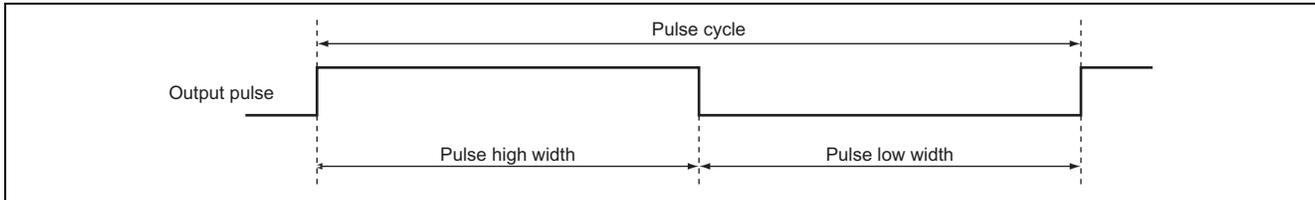


Figure 1 Example of Long-Cycle Pulse Output

2. Description of Module Usage

(1) Two 16-bit counters, TPU1 and TPU2, are connected to operate as a 32-bit counter. The long-cycle pulse thus produced is output from TPU1.

The following features are used.

- Connection of two 16-bit counters to operate as a single 32-bit counter (cascade-connected operation)
- Automatic output of a pulse by hardware with no software intervention (output-compare)
- Generation of PWM output by TGRA_1 and TGRB_1 operating as a pair (PWM mode 1)

Figure 2 is a block diagram of the TPU elements used.

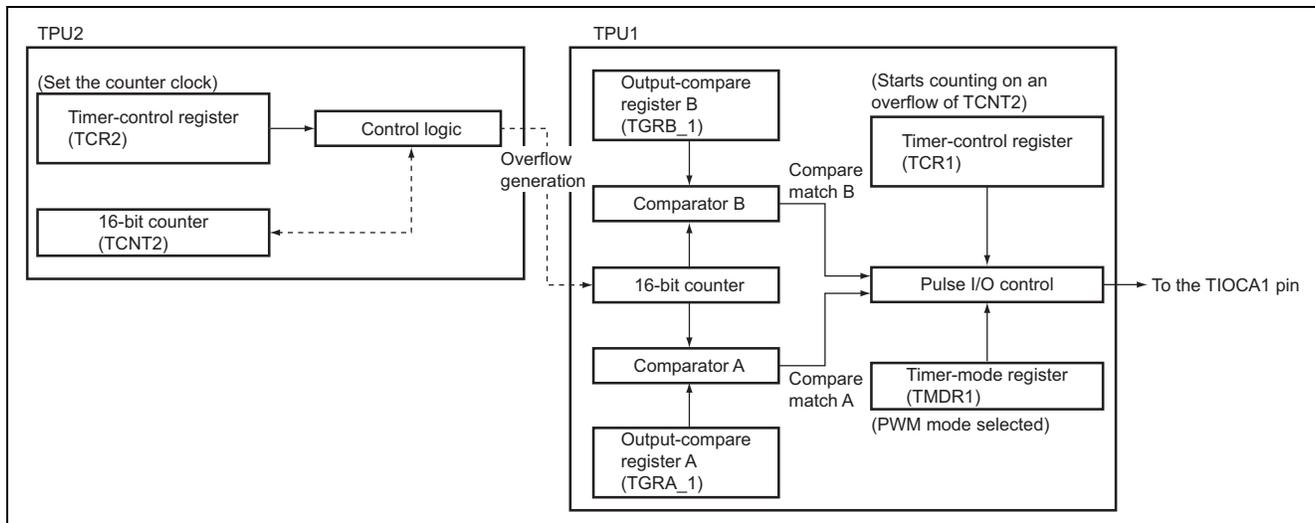


Figure 2 Block Diagram of Long-Cycle Pulse Output

(2) Usage of H8S/2239 modules in this sample task is described in table 1. A 32-bit timer-counter is configured by using the functions as described in this table.

Table 1 Assignment of Functions

Element	Description
TPU1	Selects PWM mode 1
TCR1	Sets the clock for input to TCNT1 and the counter-clearing source
TCNT1	16 higher-order bits of the 32-bit counter
TGRA_1	Sets the low width of the pulse
TGRB_1	Sets the high width of the pulse
TIOCA1	Outputs the pulse
TCR2	Selects the clock for input to TCNT2
TCNT2	16 lower-order bits of the 32-bit counter

3. Principles of Operation

Task operation is as shown in figure 3. As the figure shows, long-cycle pulses are output through a combination of hardware and software processing.

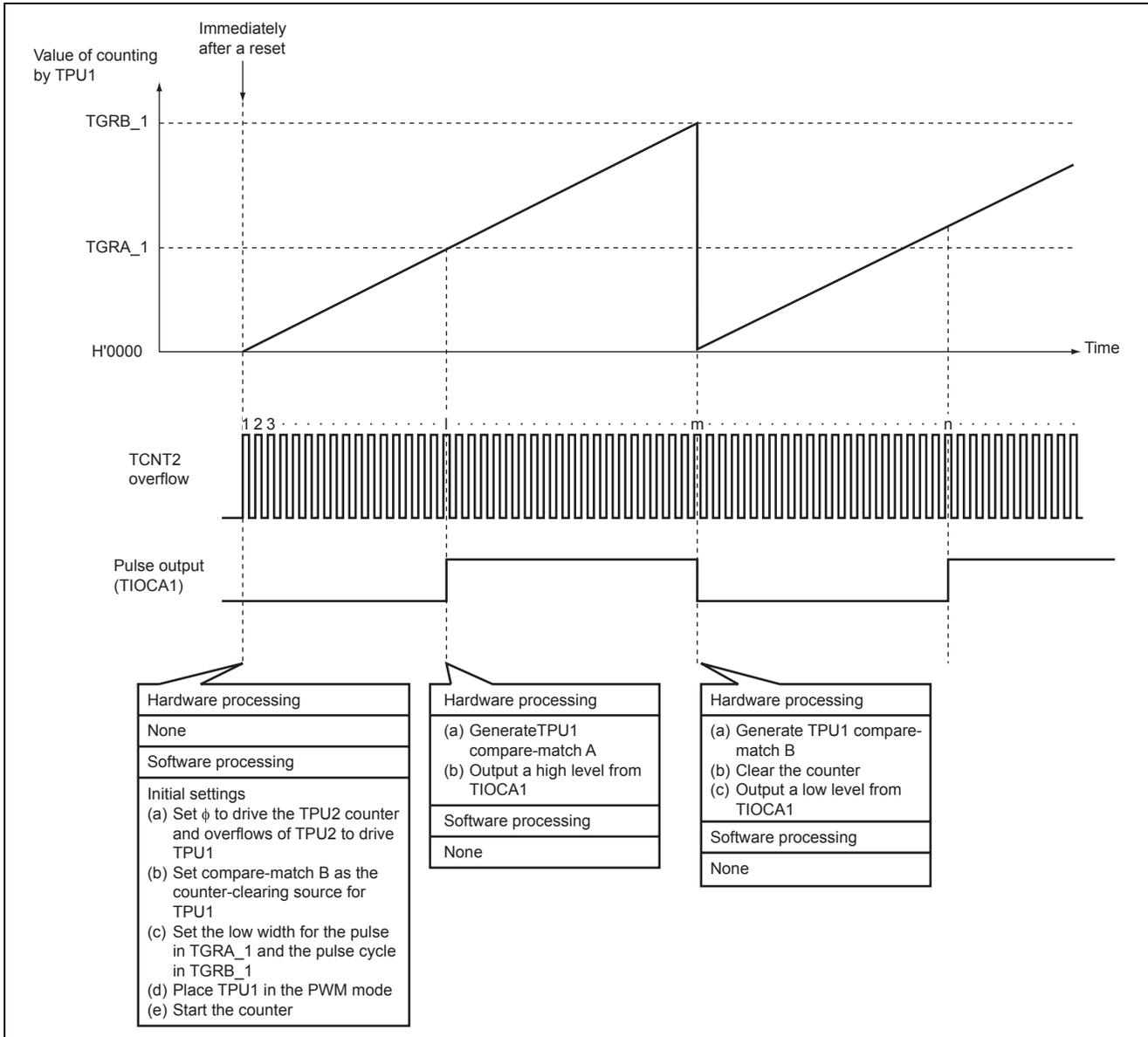


Figure 3 Output of the Long-Cycle Pulse

4. Software Description

(1) Function

Function	Label	Description
Main routine	LPULMN	Outputs a long-cycle pulse by using the counters of TPU1 and TPU2 in 32-bit counter operation

(2) Arguments

Label	Description	Data Type	Used in	I/O
lpul_wid	Sets the timer value that governs the low width of the output pulse. The low width of the pulse is obtained by the following expression: Low width (ms) = timer value x external clock (= 3.27 ms in 20-MHz operation)	unsigned short	Main routine	Input
lpul_cyc	Sets the timer value that governs the period of the output pulse. The period is obtained by the following expression: Period (ms) = timer value x external clock (TCNT2 overflow output) (= 3.27 ms in 20-MHz operation)	unsigned short	Main routine	Input

(3) Internal Registers

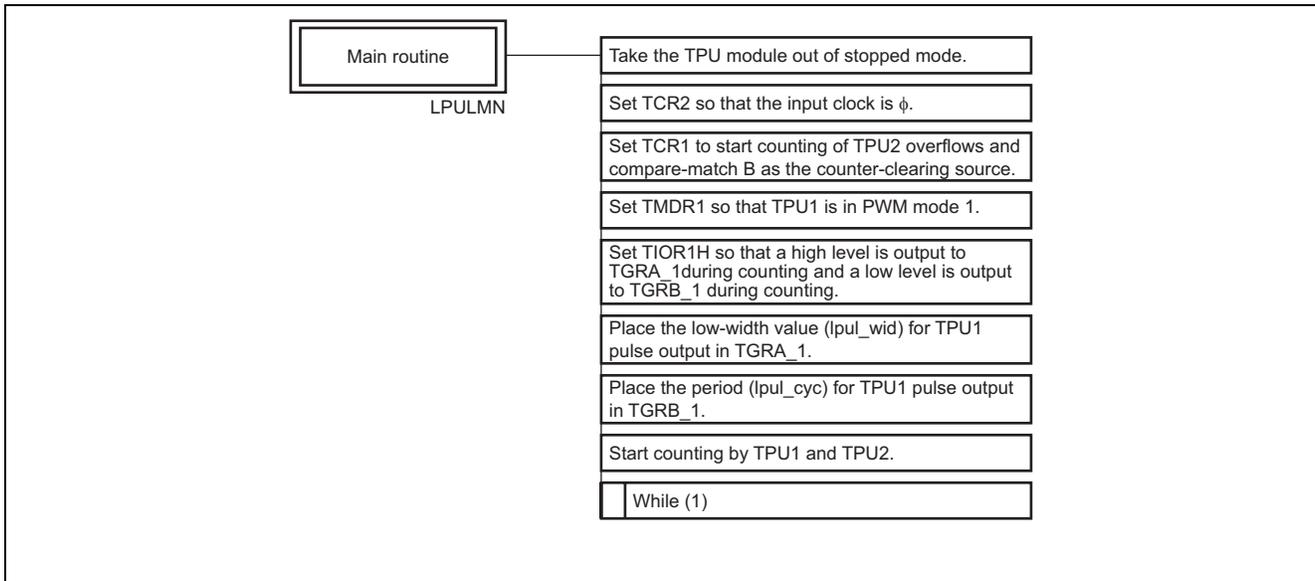
Register	Description	Used in
TSTR	Starts and stops the timer counter	Main routine
TMDR1	Selects PWM mode 1	Main routine
TCR1	Sets the clock for input to TCNT1 and the source for counter-clearing	Main routine
TCNT1	Counts the overflow of TCNT2 and operates as the 32-bit counter	Main routine
TGRA_1	Sets the low width of the pulse	Main routine
TGRB_1	Sets the high width of the pulse	Main routine
TIOCA1	Outputs the pulse	Main routine
TCR2	Selects the clock for input to TCNT2	Main routine
TCNT2	16-bit free-running counter	Main routine

(4) RAM Usage

No RAM is used other than that for argument storage.

5. PAD

(1) Main routine



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16.04	—	First edition issued

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