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April 1st, 2010
Renesas Electronics Corporation

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Introduction
A pulse with variable cycle period in the range from 6.55 ms to 214.7 s is output using the 32-bit counter. The duty rate is variable from 0 to 100%.

Target Device
H8S / 2239

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1. Specifications

(1) Performs 32-bit counting and outputs a long-cycle pulse with a variable duty cycle (see figure 1).
(2) The duty rate can be set to any value from 0 to 100%, with a resolution of 1/65535.
(3) In operation at 20 MHz, the pulse period can be set to any value between 6.55 ms and 214.7 s, in 3.27-ms units.

![Diagram of Long-Cycle Pulse Output](image)

Figure 1 Example of Long-Cycle Pulse Output
2. Description of Module Usage

(1) Two 16-bit counters, TPU1 and TPU2, are connected to operate as a 32-bit counter. The long-cycle pulse thus produced is output from TPU1.

The following features are used.

- Connection of two 16-bit counters to operate as a single 32-bit counter (cascade-connected operation)
- Automatic output of a pulse by hardware with no software intervention (output-compare)
- Generation of PWM output by TGRA_1 and TGRB_1 operating as a pair (PWM mode 1)

Figure 2 is a block diagram of the TPU elements used.

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(2) Usage of H8S/2239 modules in this sample task is described in table 1. A 32-bit timer–counter is configured by using the functions as described in this table.

Table 1  Assignment of Functions

<table>
<thead>
<tr>
<th>Element</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPU1</td>
<td>Selects PWM mode 1</td>
</tr>
<tr>
<td>TCR1</td>
<td>Sets the clock for input to TCNT1 and the counter-clearing source</td>
</tr>
<tr>
<td>TCNT1</td>
<td>16 higher-order bits of the 32-bit counter</td>
</tr>
<tr>
<td>TGRA_1</td>
<td>Sets the low width of the pulse</td>
</tr>
<tr>
<td>TGRB_1</td>
<td>Sets the high width of the pulse</td>
</tr>
<tr>
<td>TIOCA1</td>
<td>Outputs the pulse</td>
</tr>
<tr>
<td>TCR2</td>
<td>Selects the clock for input to TCNT2</td>
</tr>
<tr>
<td>TCNT2</td>
<td>16 lower-order bits of the 32-bit counter</td>
</tr>
</tbody>
</table>
3. Principles of Operation

Task operation is as shown in figure 3. As the figure shows, long-cycle pulses are output through a combination of hardware and software processing.

![Figure 3: Output of the Long-Cycle Pulse](image)

**Figure 3: Output of the Long-Cycle Pulse**
4. Software Description

(1) Function

<table>
<thead>
<tr>
<th>Function</th>
<th>Label</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>LPULMN</td>
<td>Outputs a long-cycle pulse by using the counters of TPU1 and TPU2 in 32-bit counter operation</td>
</tr>
</tbody>
</table>

(2) Arguments

<table>
<thead>
<tr>
<th>Label</th>
<th>Description</th>
<th>Data Type</th>
<th>Used in</th>
<th>I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>lpul_wid</td>
<td>Sets the timer value that governs the low width of the output pulse. The low width of the pulse is obtained by the following expression: Low width (ms) = timer value x external clock (= 3.27 ms in 20-MHz operation)</td>
<td>unsigned short</td>
<td>Main routine</td>
<td>Input</td>
</tr>
<tr>
<td>lpul_cyc</td>
<td>Sets the timer value that governs the period of the output pulse. The period is obtained by the following expression: Period (ms) = timer value x external clock (TCNT2 overflow output) (= 3.27 ms in 20-MHz operation)</td>
<td>unsigned short</td>
<td>Main routine</td>
<td>Input</td>
</tr>
</tbody>
</table>

(3) Internal Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSTR</td>
<td>Starts and stops the timer counter</td>
<td>Main routine</td>
</tr>
<tr>
<td>TMDR1</td>
<td>Selects PWM mode 1</td>
<td>Main routine</td>
</tr>
<tr>
<td>TCR1</td>
<td>Sets the clock for input to TCNT1 and the source for counter-clearing</td>
<td>Main routine</td>
</tr>
<tr>
<td>TCNT1</td>
<td>Counts the overflow of TCNT2 and operates as the 32-bit counter</td>
<td>Main routine</td>
</tr>
<tr>
<td>TGRA_1</td>
<td>Sets the low width of the pulse</td>
<td>Main routine</td>
</tr>
<tr>
<td>TGRB_1</td>
<td>Sets the high width of the pulse</td>
<td>Main routine</td>
</tr>
<tr>
<td>TIOCA1</td>
<td>Outputs the pulse</td>
<td>Main routine</td>
</tr>
<tr>
<td>TCR2</td>
<td>Selects the clock for input to TCNT2</td>
<td>Main routine</td>
</tr>
<tr>
<td>TCNT2</td>
<td>16-bit free-running counter</td>
<td>Main routine</td>
</tr>
</tbody>
</table>

(4) RAM Usage

No RAM is used other than that for argument storage.
5. PAD

(1) Main routine

- Take the TPU module out of stopped mode.
- Set TCR2 so that the input clock is φ.
- Set TCR1 so that TPU2 overflows and compare-match B as the counter-clearing source.
- Set TMDR1 so that TPU1 is in PWM mode 1.
- Set TDIR1H so that a high level is output to TGRA_1 during counting and a low level is output to TGRB_1 during counting.
- Place the low-width value (lpul_wid) for TPU1 pulse output in TGRA_1.
- Place the period (lpul_cyc) for TPU1 pulse output in TGRB_1.
- Start counting by TPU1 and TPU2.
- While (1)
## Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
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<td>1.00</td>
<td>Mar.16.04</td>
<td>—</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>
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