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April 1st, 2010
Renesas Electronics Corporation

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H8S/2200 Series

Interval Timer

Introduction

This application demonstrates the operation of H8S/2215's timer function in interval timer mode.

Target Device

H8S/2215

Contents

1. Specifications

1. Interval timer interrupts are generated at constant intervals using the interval timer function.
2. The timer counter (TCNT) overflow period is set to 32 µs. When TCNT overflows, execution shifts to a timer interrupt processing routine, in which the value of 'counter', an 8-bit counter in RAM, is incremented.

2. Description of Functions

1. Figure 1 shows a block diagram of the interval timer, and the following is the description for the block diagram (this block diagram is the same as that of the watchdog timer):
   — The timer counter (TCNT) is an 8-bit up counter that can be read from or written to. TCNT is initialized to H'00 when the TME bit in the timer control/status register (TCSR) is 0.
   — The timer control/status register (TCSR) selects a clock input to TCNT, sets timer mode, etc.
   — The reset control/status register (RSTCSR) controls internal reset signal generation and selects the type of the internal reset signal. RSTCSR is initialized to H'1F by a reset signal from the $\overline{\text{RES}}$ pin. It is not initialized by an internal reset signal generated upon a WDT overflow.

To use the 8-bit timer in interval timer mode, set the WT/$\overline{\text{IT}}$ bit to 0 and TME bit to 1 in TCSR. In interval timer mode, the interval timer interrupt (WOVI) is generated every time TCNT overflows, and interrupt processing can be executed at regular time intervals.

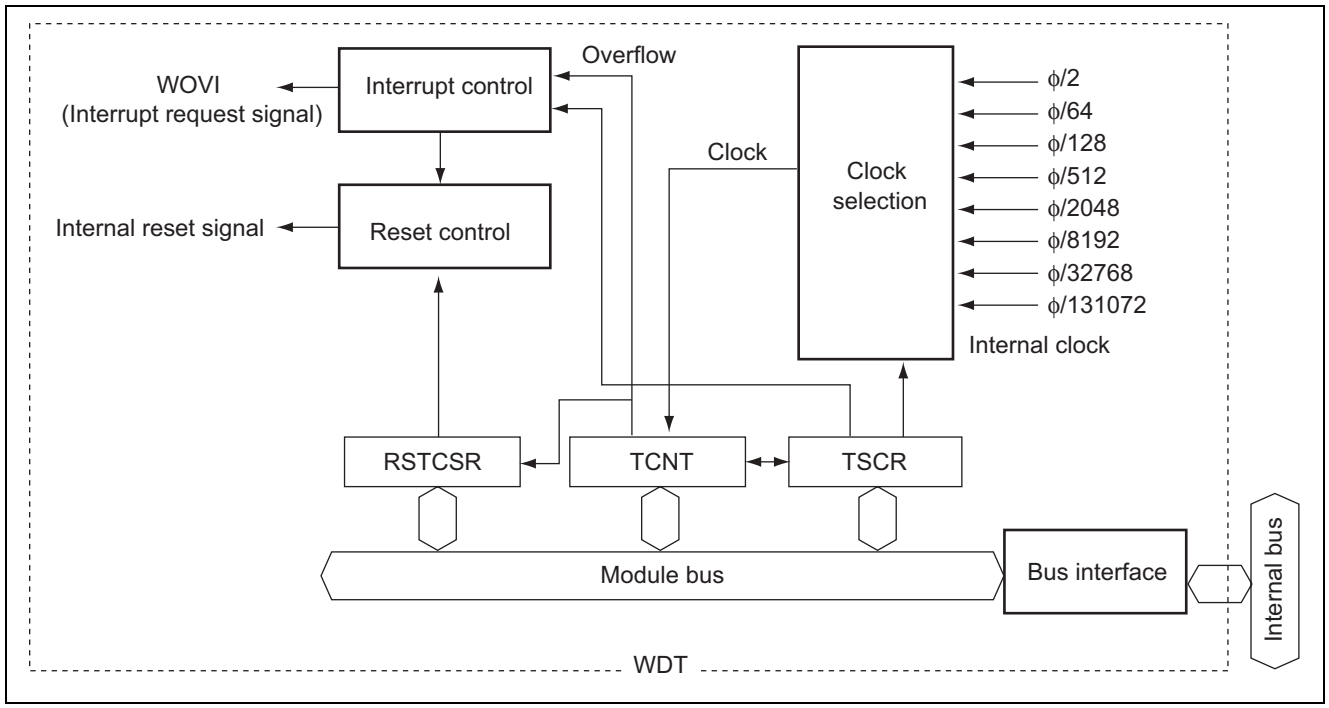


Figure 1 Block Diagram of Interval Timer

2. Table 1 shows the assignment of functions used in this sample task.

Table 1 Assignment of Functions

Elements	Description
TCNT	8-bit up counter
TCSR	Register that selects clock input to TCNT and timer mode
RSTCSR	Register that controls the internal reset signal generated upon TCNT overflow

3. Principles of Operation

Figure 2 illustrates the operation of this sample task. The 8-bit counter in RAM is incremented using the interval timer function through the hardware and software processing shown in the figure.

1. System clock (ϕ)/2 is used as the input clock for TCNT (ϕ = 16 MHz).
2. TCNT overflow period is set to 32 µs (= (1/(16 MHz/2)) × 256). When an overflow occurs, execution shifts to the timer interrupt processing routine, intval, in which 'counter' is incremented.
3. When the 'counter' value reaches H'FF, it is reset to H'00 and starts counting up again.

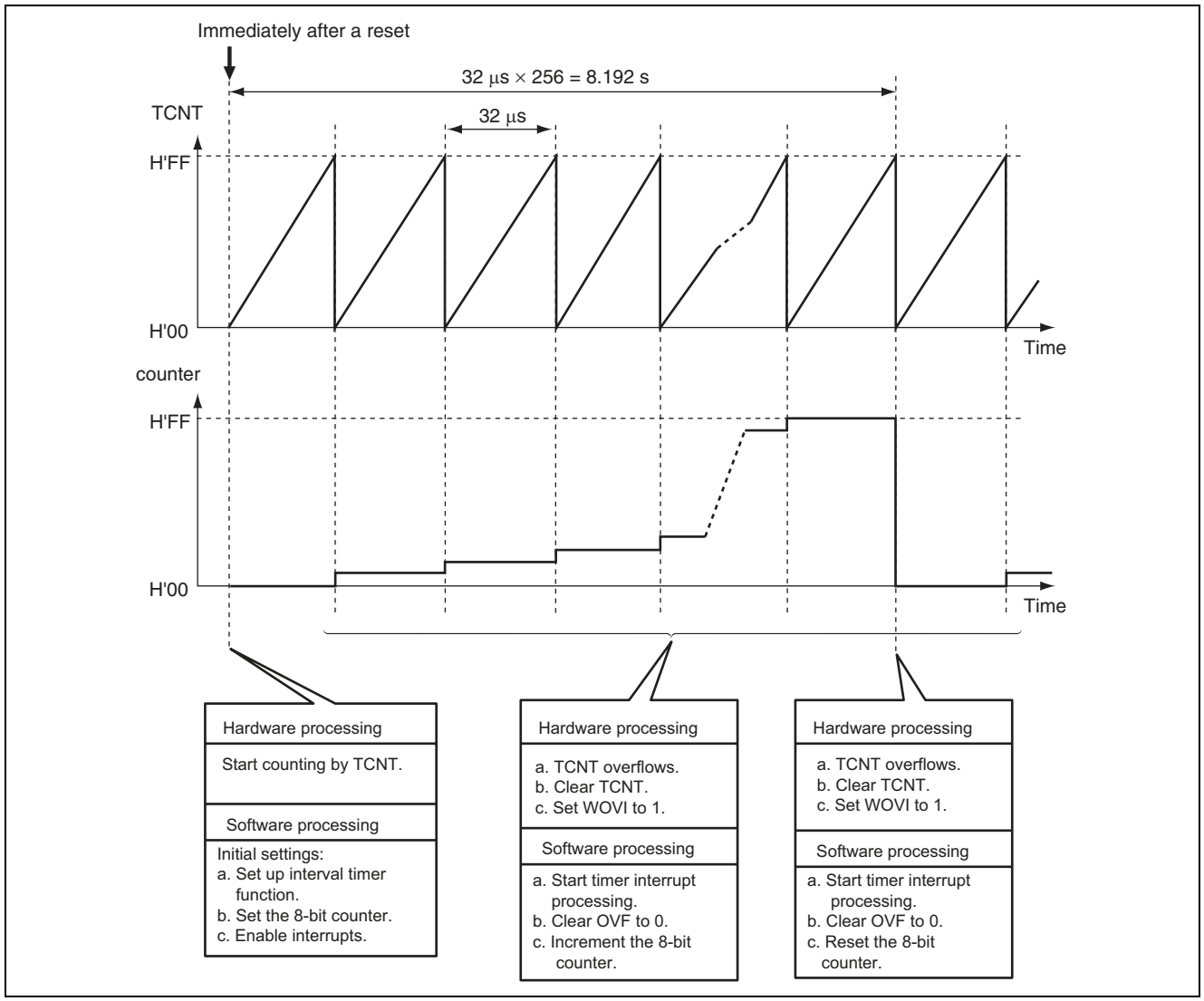


Figure 2 Operation of 8-Bit Counter Incrementation Using Interval Timer Function

4. Description of Software

4.1 Module

Table 2 describes the modules used in this sample task.

Table 2 Description of Modules

Module	Label	Function
Main routine	main	Makes settings for interval timer function, sets the 8-bit counter, and enables interrupts.
Count-up	intval	Timer interrupt processing routine that increments or initializes the 8-bit 'counter' in RAM.

4.2 Arguments

This sample task does not use arguments.

4.3 Internal Registers

The internal registers used in this sample task are described in table 3.

Table 3 Description of Internal Registers

Register		Function	Address	Setting
TCNT		Timer Counter Readable/writable 8-bit up counter	For writing: H'FFFF74 For reading: H'FFFF75	H'00 when TME in TCSR is 0
TCSR	OVF	Timer Control/Status Register (Overflow Flag) Only "0" can be written for flag clearing. When OVF = 0, no overflow occurs on TCNT. When OVF = 1, an overflow occurs on TCNT.	H'FFFF74 Bit 7	0
	WT/$\overline{IT}$	Timer Control/Status Register (Timer Mode Select) When WT/$\overline{IT}$ = 0, interval mode is selected. When WT/$\overline{IT}$ = 1, watchdog timer mode is selected.	H'FFFF74 Bit 6	0
	TME	Timer Control/Status Register (Timer Enable) When TME = 0, counting by TCNT is stopped. When TME = 1, counting by TCNT is started.	H'FFFF74 Bit 5	0
	—	Timer Control/Status Register (Reserved) These bits are always read as 1 and cannot be modified.	H'FFFF74 Bit 4 Bit 3	1, 1
	CKS2 to CKS0	Timer Control/Status Register (Clock Select 2 to 0) Eight values from 000 to 111 can be set for CKS2 to CKS0. In this sample task, these bits are set to 000 to cause an overflow at the cycle of ϕ/2 (32 μs). (ϕ = 16 MHz)	H'FFFF74 Bit 2 to bit 0	CKS2 = 0 CKS1 = 0 CKS0 = 0

Register		Function	Address	Setting
RSTCSR	WOVF	Reset Control/Status Register (Watchdog Timer Overflow Flag) WOVF = 0 indicates that TCNT has not overflowed (or TCNT is cleared). WOVF = 1 indicates that TCNT has overflowed (H'FF to H'00).	For writing: H'FFFF76 For reading: H'FFFF77 Bit 7	0
	RSTE	Reset Control/Status Register (Reset Enable) When RSTE = 0, internal reset is not induced but only TCNT and TCSR are reset when TCNT has overflowed. When RSTE = 1, internal reset is induced when TCNT has overflowed.	For writing: H'FFFF76 For reading: H'FFFF77 Bit 6	0
	RSTS	Reset Control/Status Register (Reset Select) When RSTS = 0, a power-on reset is selected. When RSTS = 1, a manual reset is selected.	Same addresses as above. Bit 5	0
	—	Reset Control/Status Register (Reserved) These bits are always read as 1 and cannot be modified.	Same addresses as above. Bit 4 to bit 0	1,1,1,1,1

4.4 RAM Usage

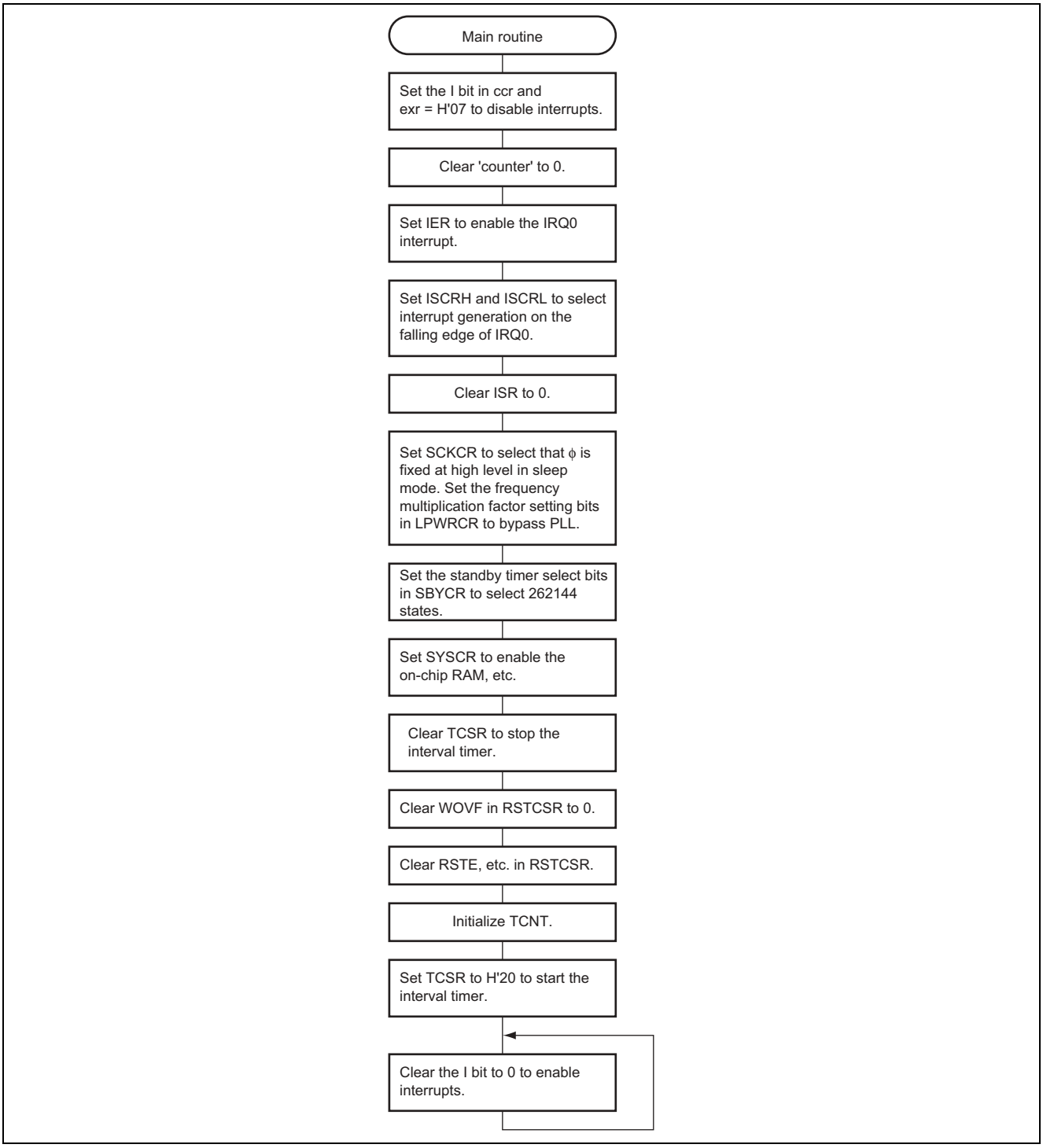
Table 4 describes the RAM usage in this sample task.

Table 4 Description of RAM

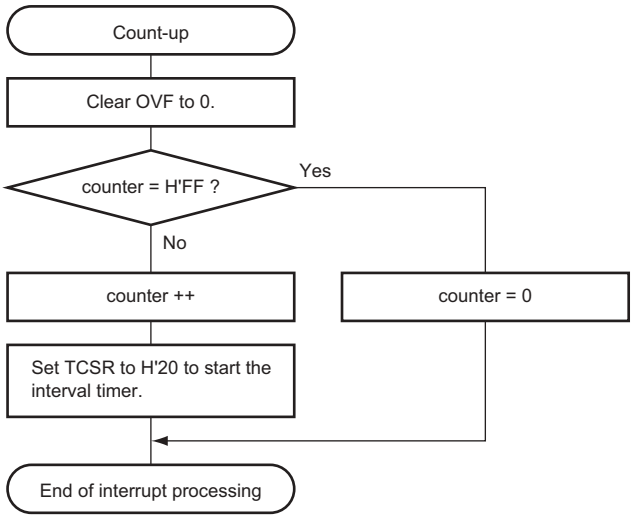
Label	Function	Address	Used in
counter	8-bit counter	H'FFB000	Main routine, Count-up

5. Flowchart

1. Main routine



2. Timer interrupt processing routine



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16, 2004	—	First edition issued

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