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H8S/2200 Series

DMA Transfer by External Request (DREQ)

Introduction

Transfers data on one internal RAM to another internal RAM with a DMAC, using the external request pin as the activation source.

Target Device

H8S/2239

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2. Configuration 2
3. Description of Functions 3
4. Principles of Operation 4
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1. Overview

The H8S/2239 transfers data on one internal RAM to another internal RAM with a DMAC. In this transfer, the H8S/2239 uses the external request pin (DREQ0 or DREQ1) as the activation source.

2. Configuration

Figure 1 shows the configuration of the confirmed operation of this application note.

List of Components Used

No.	Component	Specifications
1	HSB8S2239F H8S/2239 CPU board (HOKUTO DENSHI CO., LTD.)	Board power supply input: 3.3 VDC Operating frequency: Main 16 MHz MCU operating mode: 7 (Single chip mode)

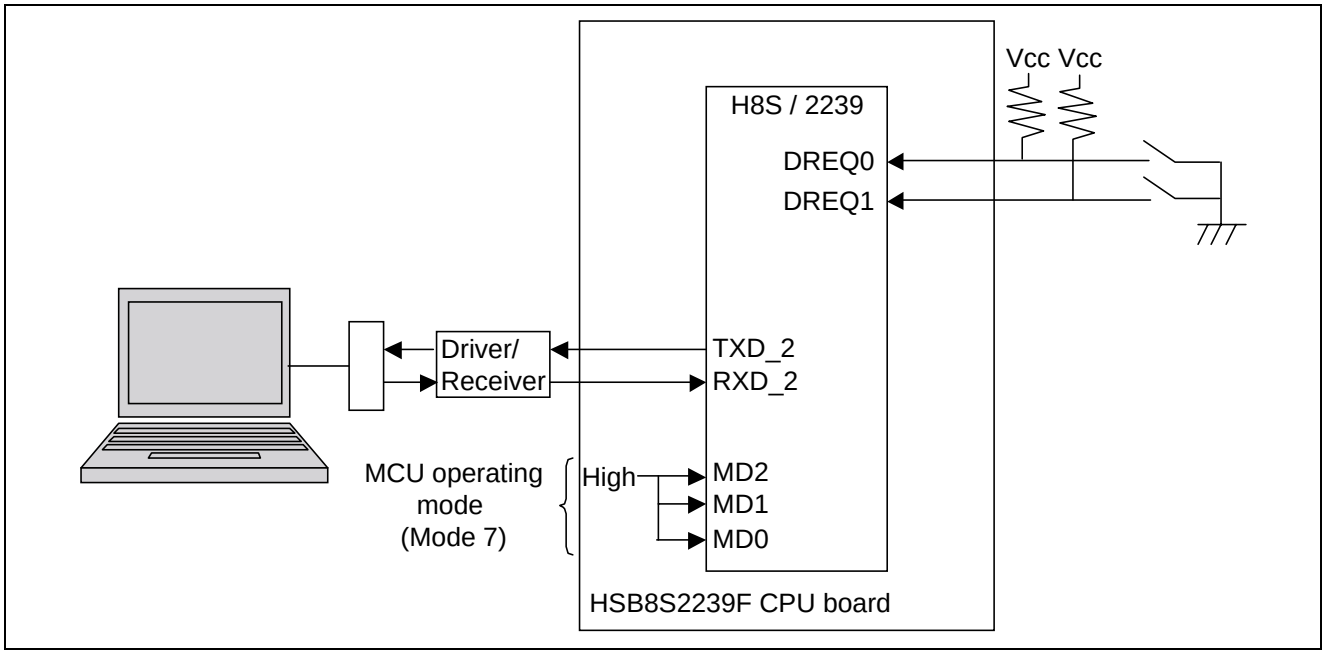


Figure 1 Confirmed Configuration

3. Description of Functions

The DMAC is started by inputting a command from the terminal software connected to the RS-232C interface. The H8S/2239 provides the read/write function for debugging internal memory.

1. Communication specifications
   The terminal software is connected according to the specifications below.

Communication method	Asynchronous
Bit rate	38400 bps
Data size	8 bits
Parity	None
Stop bit	1 bit
Terminating code	Line feed

2. Supported functions

No.	Function	Specifications
1	Performs DMA transfer to transfer data at 0xFFFFC0 - 0xFFFFCF to 0xFFFFD0 - 0xFFFFDF on an internal RAM chip. In this transfer, use DREQ0 or DREQ1 as the external request. The edge sense or level sense can be selected to use the DREQ.	Format: dmΔ(dreq_no)Δ(factor) dreq_no: 0 = Uses the DREQ0 external pin as the DMAC activation source. 1 = Uses the DREQ1 external pin as the DMAC activation source. factor: 2 = Edge sense (DMA is activated on the falling edge of DREQ. In this case, data is transferred each time a DREQ falling edge is detected.) 3 = Level sense (DMA is activated at the low level sense of DREQ. In this case, data is continuously transferred while DREQ is low.)
2	Data of 64 bytes is read from a specified memory address for display.	Format: mrΔaddress (Specify a 4-byte value in address.)
3	Data of 4 bytes is written at a specified memory address.	Format: mwΔaddressΔdata (Specify a 4-byte value in address and data.)

4. Principles of Operation

4.1 Initialization Processing

Before exercising DMAC control, start up the microcomputer and perform operations such as internal register initialization.

1. Control for low power consumption, clock oscillator initialization

Register name ←Set value	Bit	Name	Value	Contents
LPWCR ←0x03	7	DTON	0	Direct transfer on flag
	6	LSON	0	Low-speed on flag
	5	NESEL	0	Noise elimination sampling frequency (use of ϕ/32)
	4	SUBSTP	0	Subclock oscillator operation
	3	RFCUT	0	Uses internal feedback resistance control.
	2	----	0	
	1:0	STC[1:0]	11	Bypasses PLL.
MSTPCRA ←0x0C	7	MSTPA7	0	Operates the DMAC module.
	6	MSTPA6	0	Operates DTC module.
	5	MSTPA5	0	Operates the TPU module.
	4	MSTPA4	0	Operates the TMR_0,1 module.
	3:2	MSTPA[3:2]	11	(Reserved)
	1	MSTPA1	0	Operates the AD module.
	0	MSTPA0	0	Operates the TMR_2,3 module.
MSTPCRB ←0x1F	7	MSTPB7	0	Operates the SCI0 module.
	6	MSTPB7	0	Operates the SCI1 module.
	5	MSTPB7	0	Operates the SCI2 module.
	4:0	MSTPB[4:0]	1111	(Reserved)
MSTPCRC ←0x4F	7	MSTPC7	0	Operates the SCI3 module.
	6	MSTPC6	1	(Reserved)
	5	MSTPC5	0	Operates the DA module.
	4	MSTPC4	0	PC break controller operation
	3:0	MSTPC[3:0]	11111	(Reserved)

2. I/O port initialization
   Set the input/output pins of port 7 as indicated below. Set all other pins to the output mode.

Port	Register name ←Set value	Bit	Name	Value	Contents
7	P7DDR ←0xFC	7:2	P7[7:2]DDR	all"1"	Output (Not used)
		1	P71DDR	0	Input (DREQ1)
		0	P70DDR	0	Input (DREQ0)

3. TPU0 timer initialization
   Make settings so that a timer interrupt is generated at intervals of 100 ms for timer monitoring.

Register name ←Set value	Bit	Name	Value	Contents
TCR_0 ←0x23	7:5	CCLR[2:0]	001	Counter clear on TGRA compare match
	4:3	CKEG[1:0]	00	Count on rising edge
	2:0	TPSC[2:0]	011	Count with ϕ/64
TMDR_0 ←0x00	7:6	----	00	
	5	BFB	0	Normal TGRB operation
	4	BFA	0	Normal TGRA operation
	3	----	00	
	2:0	MD[2:0]	000	Normal operation
TIORH_0 ←0x00	7:4	IOB[3:0]	0000	TBRB output compare (Not used)
	3:0	IOA[3:0]	0000	TBRA output compare
TIORL_0 ←0x00	7:4	IOD[3:0]	0000	TBRD output compare (Not used)
	3:0	IOC[3:0]	0000	TBRC output compare (Not used)
TIER_0 ←0x00	7	TTGE	0	Disables AD conversion start request. (Not used)
	6	----	0	
	5	TCIEU	0	Disables underflow interrupt. (Not used)
	4	TCIEV	0	Disables overflow interrupt. (Not used)
	3	TGIED	0	Disables TGRD interrupt. (Not used)
	2	TGIEC	0	Disables TGRC interrupt. (Not used)
	1	TGIEB	0	Disables TGRB interrupt. (Not used)
	0	TGIEA	0	Enables TGRA interrupt.
TGRA_0 ←25000	15:0	TGRA_0	25000	TBRA output compare value (To be set to generate an interrupt at intervals of 100 ms)
TCNT_0 ←0x0000	15:0	TCNT_0	0x0000	Counter clear
TSTR ←0x01	7:0	TSTR	0x01	TCNT_0 counter start

4. Serial interface (SCI_2) initialization
   Make settings to connect the terminal software for starting DTC.

Register name ←Set value	Bit	Name	Value	Contents
SCR_2 ←0x00	7	TIE	0	Disables transmit interrupt.
	6	RIE	0	Disables receive interrupt.
	5	TE	0	Disables transmit operation.
	4	RE	0	Disables receive operation.
	3	MPIE	0	Disables multi-processor interrupt.
	2	TEIE	0	Disables transmit end interrupt.
	1:0	CKE[1:0]	00	Asynchronous, internal clock used
	7	TIE	0	Disables transmit interrupt.
SMR_2 ←0x00	7	C/A	0	Asynchronous mode
	6	CHR	0	8-bit length
	5	PE	0	Makes no parity check.
	4	O/E	0	Even parity (Not used)
	3	STOP	0	One stop bit
	2	MP	0	Disables the multi-processor communication function.
	1:0	CKS[1:0]	00	Clock source = ϕ
SCMR_2 ←0x00	7:4	----	0000	
	3	DIR	0	LSB first
	2	INV	0	No data inversion
	1-0	----	00	
BRR ←9	7:0	BRR	12	Sets the transmission speed to 38400 bps.

— Wait at least one stop bit time period. (38400 bps: About 30 µs)
— Receive processing is enabled.

Register name (Address←Set value)	Bit	Name	Value	Contents
SCR_2 ←0x50	7	TIE	0	Disables transmit interrupt.
	6	RIE	1	Enables receive interrupt.
	5	TE	0	Disables transmit operation.
	4	RE	1	Enables receive operation.
	3	MPIE	0	Disables multi-processor interrupt.
	2	TEIE	0	Disables transmit end interrupt
	1:0	CKE[1:0]	00	Asynchronous, internal clock used

4.2 DMAC Control

1. Overview

Activate the DMAC by entering the following command from the terminal software connected to SCI:

Format: dmΔ(dreq_no)Δ(factor)

dreq_no : 0 = Uses the DREQ0 external pin as the DMAC activation source.
1 = Uses the DREQ1 external pin as the DMAC activation source.

factor : 2 = Edge sense
(DMA is activated on the falling edge of DREQ. In this case, data is transferred each time a DREQ falling edge is detected.)
3 = Level sense
(DMA is activated upon the detection of DREQ at low level. In this case, data is continuously transferred while DREQ is low.)

The DMAC performs DMA transfer to transfer data at 0xFFFFC0 - 0xFFFFCF to 0xFFFFD0 - 0xFFFFDF on an internal RAM chip. In this transfer, the DMAC uses DREQ0 or DREQ1 as the external request pin. In this application note, the DMAC is set so that it resets the receive interrupt source. This reset disables normal receive interrupts during DMA transfer (depending on the setting of DMABCRH(DTA)). When data transfer ends, a DMAC end interrupt occurs to end DMA transfer processing.

The DMAC of the H8S/2215 has four channels (0A, 0B, 1A, and 1B) and run in the operating modes shown below. In this application note, however, the DMAC uses channel 0 when DREQ0 is the activation source and channel 1 when DREQ1 is the activation source. It uses these channels in the normal mode of the full address mode. If the addresses of both the transfer source and transfer destination are incremented as in this application note, you must use the full address mode.

For more information about the specifications of each operating mode, see the "H8S/2215 Series Hardware Manual."

Transfer mode		Transfer source	Remarks
Full address mode	Normal mode (1) Auto-request • A transfer request is internally retained. • The specified count from 1 to 65536 is continuously transferred. • Burst/cycle steal transfer can be selected.	• Auto-request	• One or two A and B channels can be operated in combination.
	(2) External request • A single transfer request can transfer 1 byte or 1 word. • The number of transfers is 1 to 65536.	• External request	
	Block transfer mode • A single transfer request can transfer the specified 1 block size. • The transfer count is 1 to 65536. • The source or destination can be specified in the block area. • The block size is 1 to 256 bytes or words.	• Compare match/input capture A interrupt of the TPU channels 0 to 5 • SCI send data empty interrupt • SCI receive data full interrupt • A/D converter conversion end interrupt • External request	

2. DMAC setting

Before starting the DMAC, set each register using the procedures shown below.

This application program enables this setting to be made using one subroutine (set_dma_req_dreq) at a time. For details, see Chapter 5, "Description of Sample Program."

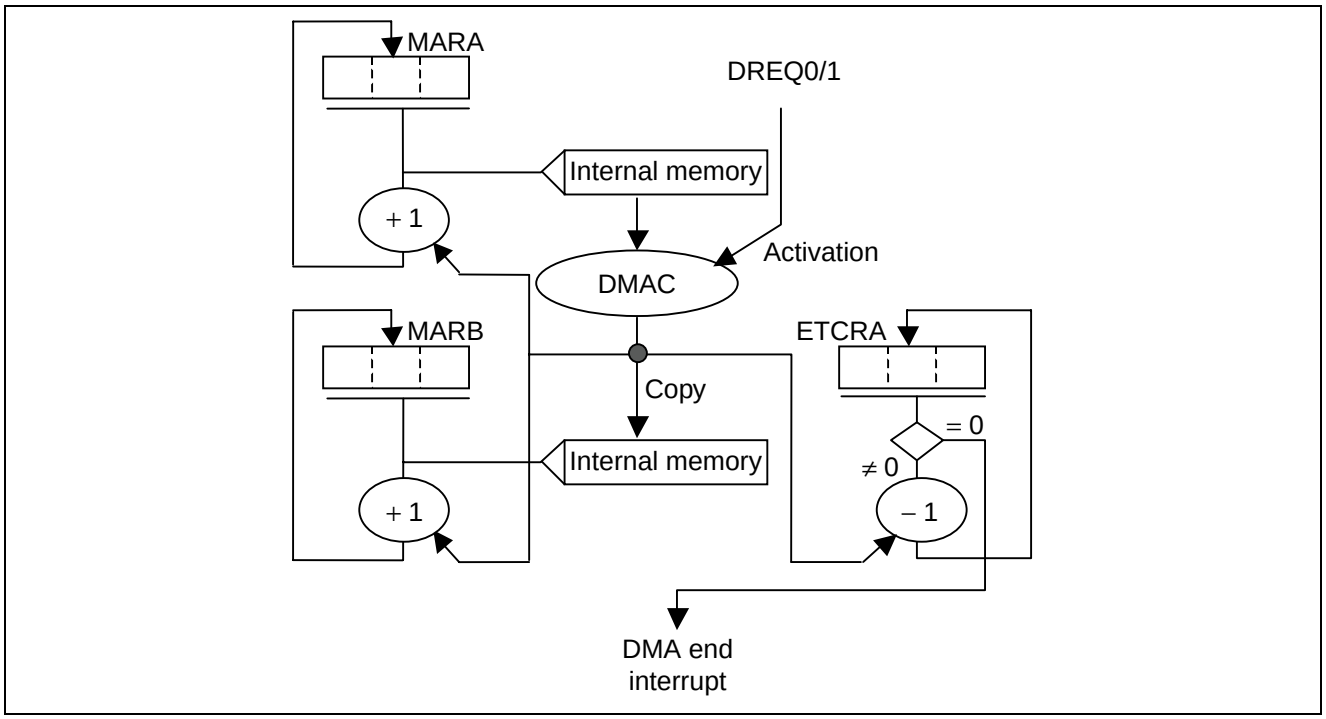
If the activation source is DREQ0, 0 is added to the end of the character string(enclosed in parentheses) of the set register name. If the activation source is DREQ1, 1 is added to the end of the character string.

For example, if the activation source is DREQ0, DMBCRH(FAE) becomes DMBCRH(FAE0). If the activation source is DREQ1, DMBCRH(FAE) becomes DMBCRH(FAE1).

No	Setting	Register to be set
1	Set the operating mode to the full address mode.	DMABCRH(FAE) ← 0
2	Set the internal interrupt source so that it is reset by the DMAC during DMA transfer. (In activation by an external request, this bit is not used.)	DMABCRH(DTA) ← 1
3	Set the starting address (0xFFFFC0) of the transfer source in MARA.	MARA ← 0xFFFFC0
4	Set the starting address (0xFFFFD0) of the transfer destination in MARB.	MARA ← 0xFFFFD0
5	Set the number of transfers in ETCRA.	ETCRA ← 16
6	Set 1 byte as the unit of DMA transfer.	DMCRA(DTSZ) ← 0
	Set DMCRA so that MARA is incremented by 1 every DMA transfer.	DMCRA(SAID) ← 0 DMCRA(SAIDE) ← 1
	Set the normal mode.	DMCRA(BLKDIR) ← 0 DMCRA(BLKE) ← 0
	Set the DMCRA so that MARB is incremented by 1 every DMA transfer.	DMCRA(DAID) ← 0 DMCRA(DAIDE) ← 1
	Set DMCRA so that DMA can be activated by DREQ.	When the DREQ uses edge sense: DMCRA(DTF[3:0]) ← 2 When the DREQ use level sense: DMCRA(DTF[3:0]) ← 3
7	Set DMA data transfer to "enable." (Actual transfer processing is triggered by the DREQ signal.)	DMABCRH(DTME) ← 1 DMABCRH(DTE) ← 1
8	Set DMABCRH so that a DMA end interrupt occurs when DMA transfer ends. (DTIEA is used to set a transfer end interrupt and DTIEB to set a transfer suspension interrupt. In this application note, the transfer suspension interrupt is not used.)	DMABCRH(DTIEA) ← 1 DMABCRH(DTIEB) ← 0

3. DMAC activation
   Making the above settings performs DMA transfer where the DREQ pin serves as the activation source.
   There are two ways DREQ pin is used: edge sense and level sense. When the edge sense is selected, the DMAC transfers one-byte data or one-word data each time change of the DREQ pin from a high level to a low level is detected. When the DREQ pin is kept at a high level when the level sense is selected, the DMAC enters the transfer request wait state. The DMAC continuously transfers data when the DREQ pin is kept at a low level.

4. DMAC operation
   The DMAC performs DMA transfer the number of transfers set in the ETCRA register. At the end of DMA transfer, a DMAC end interrupt occurs to end processing. The processing flow of this operation is shown below.
   A. The DMAC copies the contents at the transfer source address (0xFFFFC0) indicated by the MARA register to the transfer destination address (0xFFFFD0) indicated by the MARB register.
   B. The DMAC increments the transfer destination address indicated by the MARA register and transfer source address indicated by the MARB register by one and decrements the number of transfers indicated by the ETCRA register by one.
   C. Steps A. and B. are repeated till ERCTA becomes 0.
   D. When ERCTA becomes 0, a DMA end interrupt occurs and the DMAC resets DMABCRH(DTE) to 0.
   E. Software sets DMABCRH(DTIEA) to 0 to end DMAC processing during DMA end interrupt processing.



5. Description of Sample Program

5.1 File Configuration

A sample program is provided as a project of HEW (High-performance Embedded Workshop). When h8s.hws is executed, HEW starts up to enable source program referencing and updating. If you do not have HEW, directly reference the following source files on an editor:

No.	File name	Application
1	resetprg.c	Executed starting at reset vector address 0 when the microcomputer is reset
2	intprg.c	Executed when an interrupt source other than a reset is generated.
3	dbsct.c	Processing for setting the start and end addresses of a section used by the _INITSCT function of resetprg.c in the section initialization table. For details of the processing, refer to sections 9 and 10 of the "H8S and H8/300 Series C/C++ Compiler, Assembler, Optimizing Linkage Editor User's Manual."
4	h8s2239.c	Main routine of this application note
5	com.c	Main common and interrupt processing routine of this application note
6	2239S.H	Structure definition file of the internal registers of the H8S/2239 This file is available from the following URL [*2] but it does not contain DMAC-related definitions. For this reason, this file is partly modified and used. For modification locations, see "Source Codes." (The structure definition for the DMAC was cited from the H8S/2215 use.)
7	cwtbl.h	Variable and constant definitions are made for this application note.
8	prototypeh	A prototype declaration is made for this application note.
9	stacksct.h	A stack size definition is made.

[*1] http://www.renesas.com
[*2] http://www.renesas.com

5.2 Linkage

The linkage address of each section is indicated below.

In a HEW project file, a section can be referenced or set with Category : section in the Link/Librarq tab of the -Standard Toolchain option.

Section	Start address
PResetPRG	0x000400
PIntPRG	
P	0x000800
C	
C$DSEC	
C$BSEC	
D	
B	0xFFB000
R	
S	0xFFEDB0

5.3 Subroutine Specifications

In this application note, you can set and start DMA parameters using only one subroutine. Using this function lets you use DMA easily.

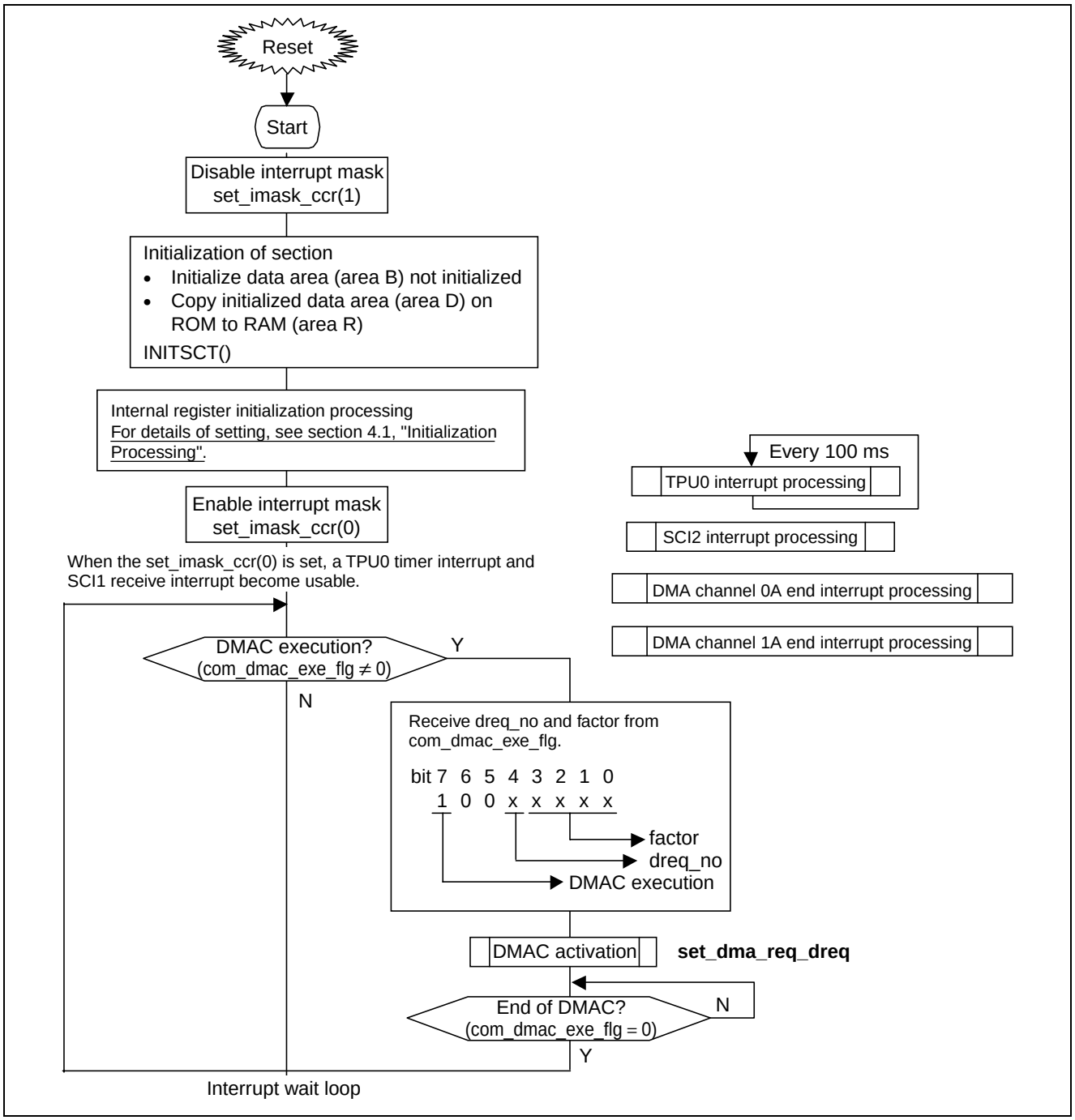
1. The following subroutine performs DMA transfer to transfer data at 0xFFFFC0 - 0xFFFFCF to 0xFFFFD0 - 0xFFFFDF on an internal RAM chip. In this DMA transfer, the DREQ0 or DREQ1 external request serves as the activation source.

```
Subroutine name: void set_dma_req_dreq
                   ( unsigned long dreq_no , unsigned long factor)
```

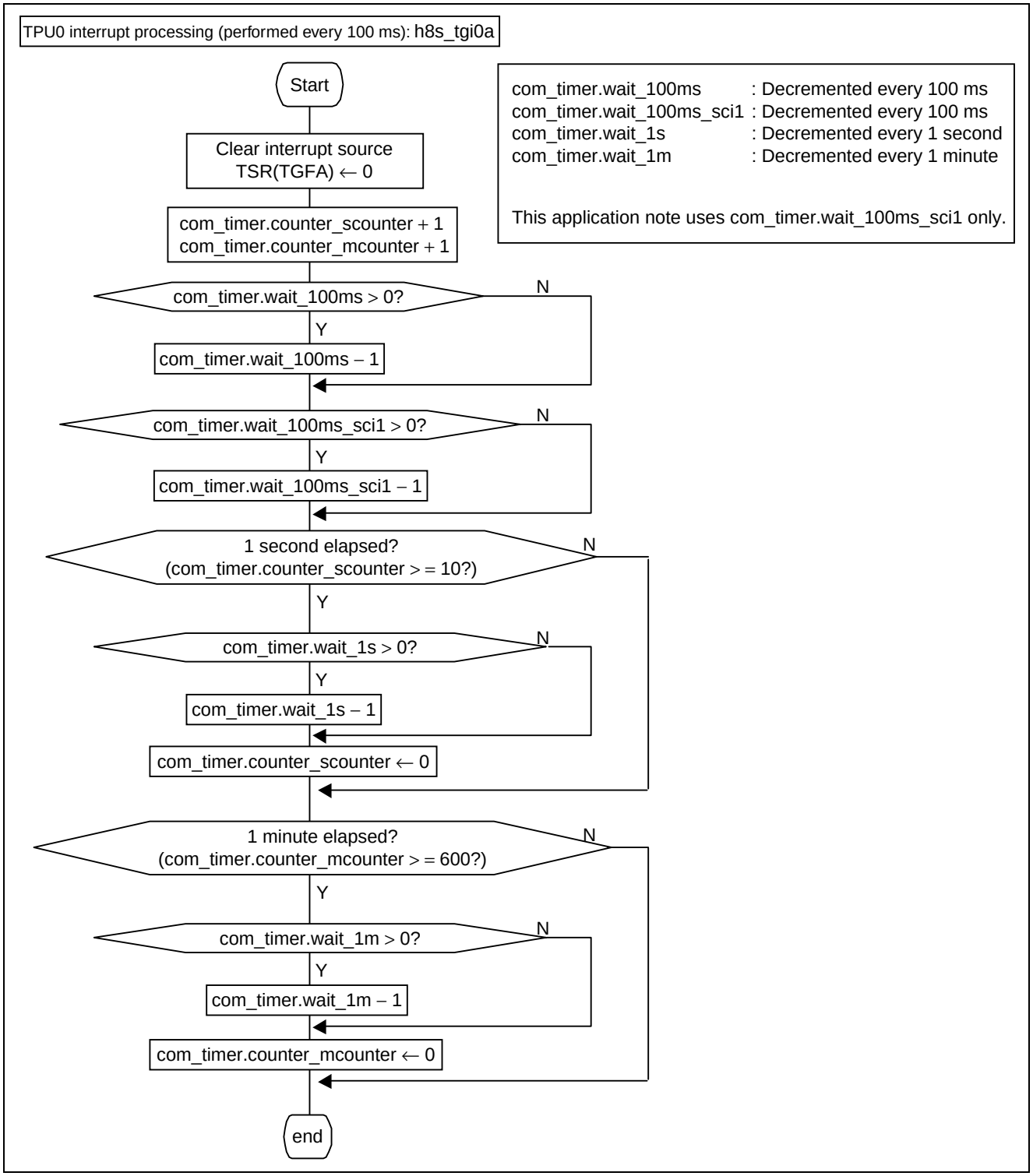
Parameter	Setting
dreq_no	Specifies DREQ0 or DREQ1 as the activation source. **DREQ_0** (0) : Selects DREQ0. **DREQ_1** (1) : Selects DREQ1
factor	Specifies a DMAC activation method using DREQ. **DREQ_EDGE** (2) : Activates the DMAC on the falling edge of DREQ. **DREQ_LOW_LEVEL** (3) : Activates the DMAC when change of the DREQ pin to a low level is detected.

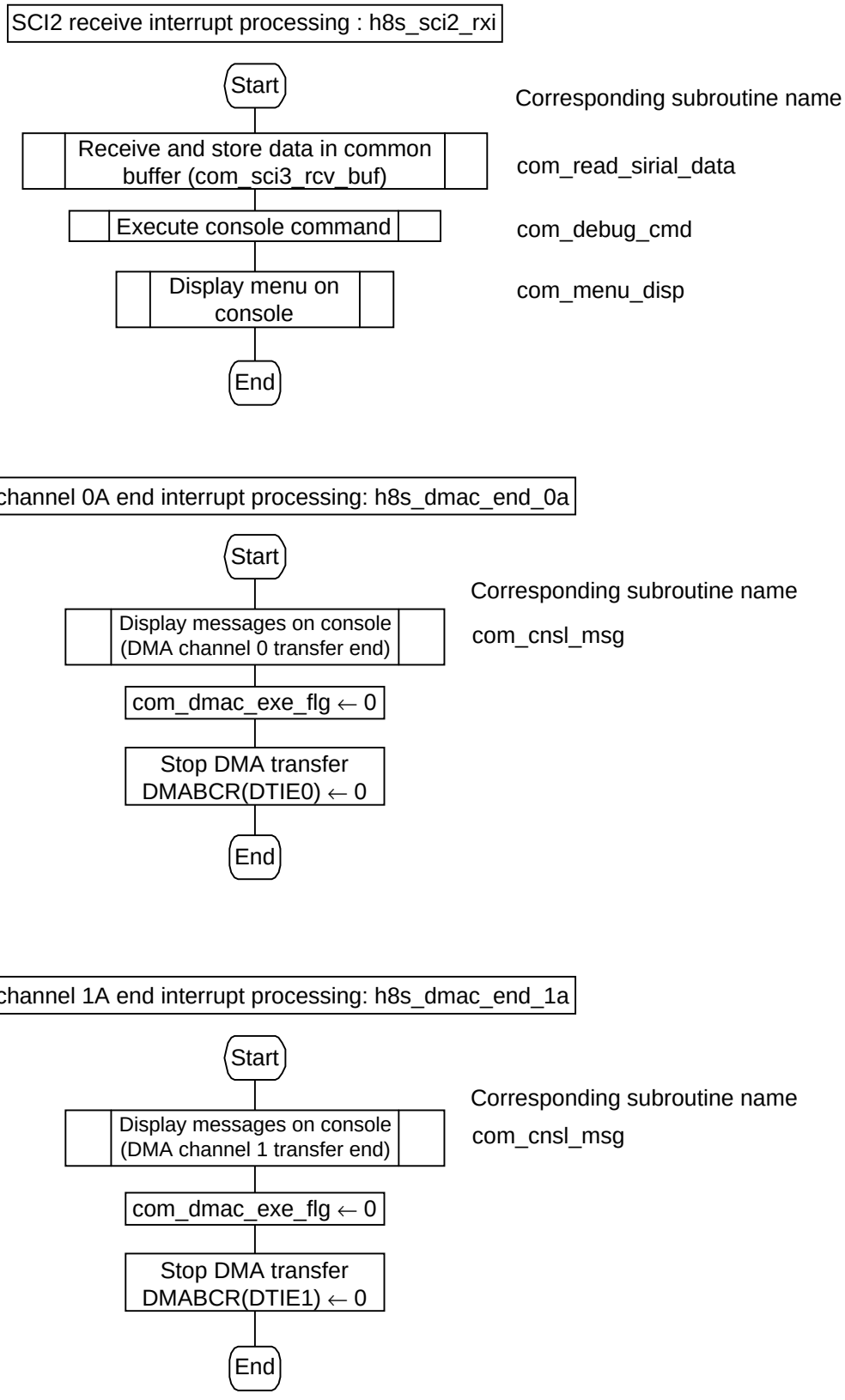
6. Flowchart

6.1 Overall Flow



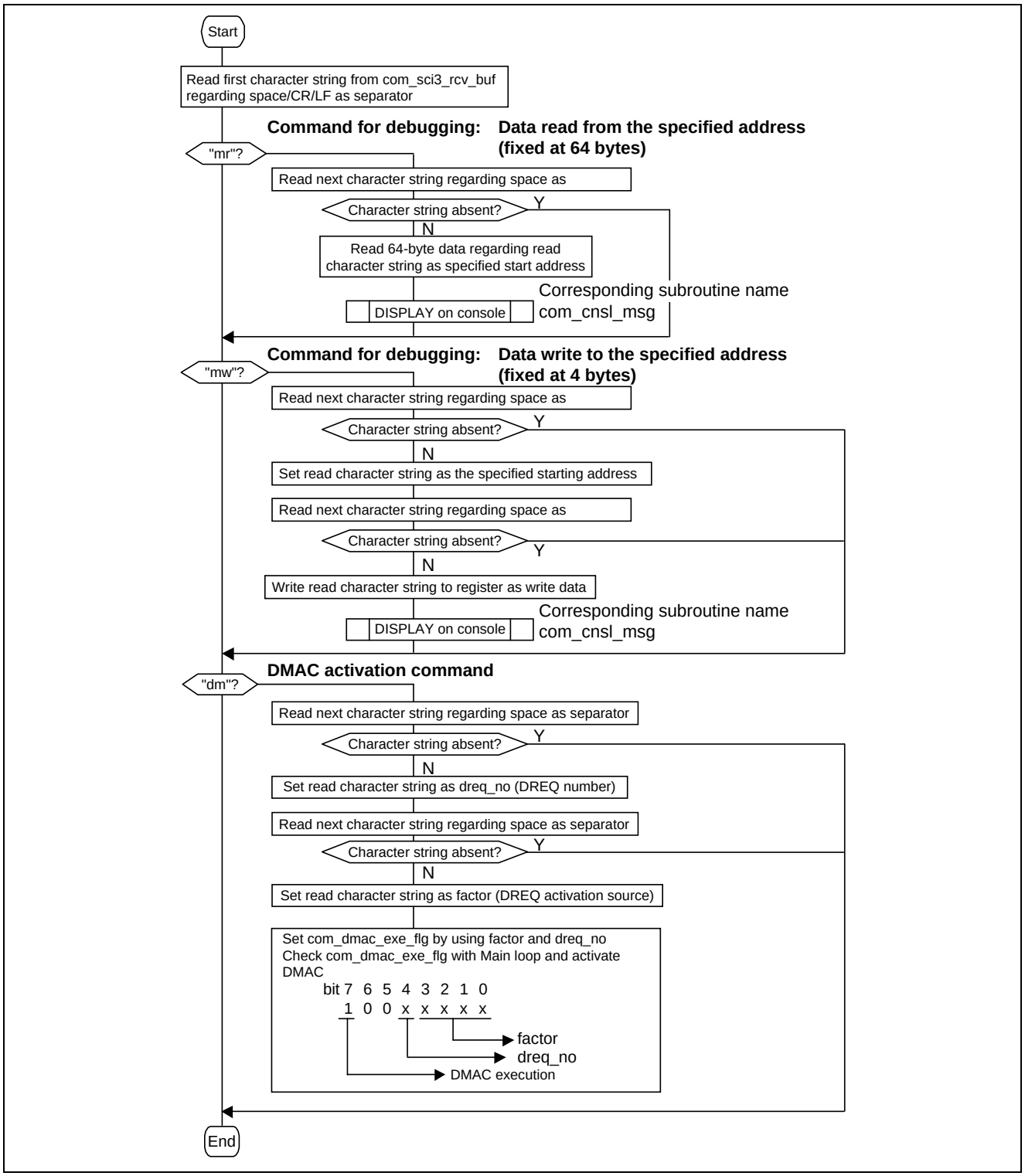
6.2 Interrupt Processing



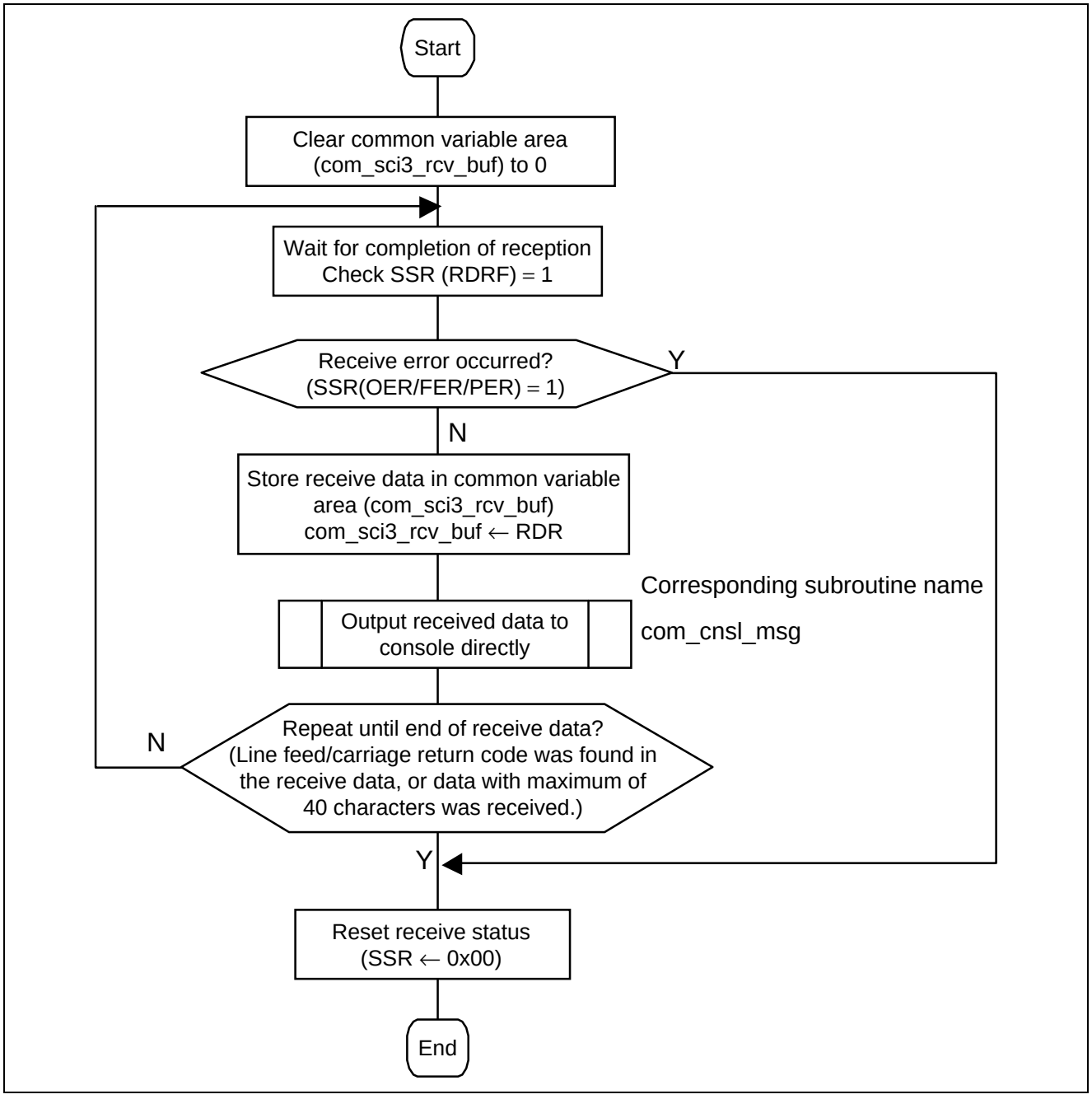

SCI2 receive interrupt processing : h8s_sci2_rxi
Start
Receive and store data in common buffer (com_sci3_rcv_buf)
Execute console command
Display menu on console
End
Corresponding subroutine name
com_read_sirial_data
com_debug_cmd
com_menu_disp
DMA channel 0A end interrupt processing: h8s_dmac_end_0a
Start
Display messages on console (DMA channel 0 transfer end)
com_dmac_exe_flg ← 0
Stop DMA transfer DMABCR(DTIE0) ← 0
End
Corresponding subroutine name
com_cnsl_msg
DMA channel 1A end interrupt processing: h8s_dmac_end_1a
Start
Display messages on console (DMA channel 1 transfer end)
com_dmac_exe_flg ← 0
Stop DMA transfer DMABCR(DTIE1) ← 0
End
Corresponding subroutine name
com_cnsl_msg

6.3 Detailed Processing

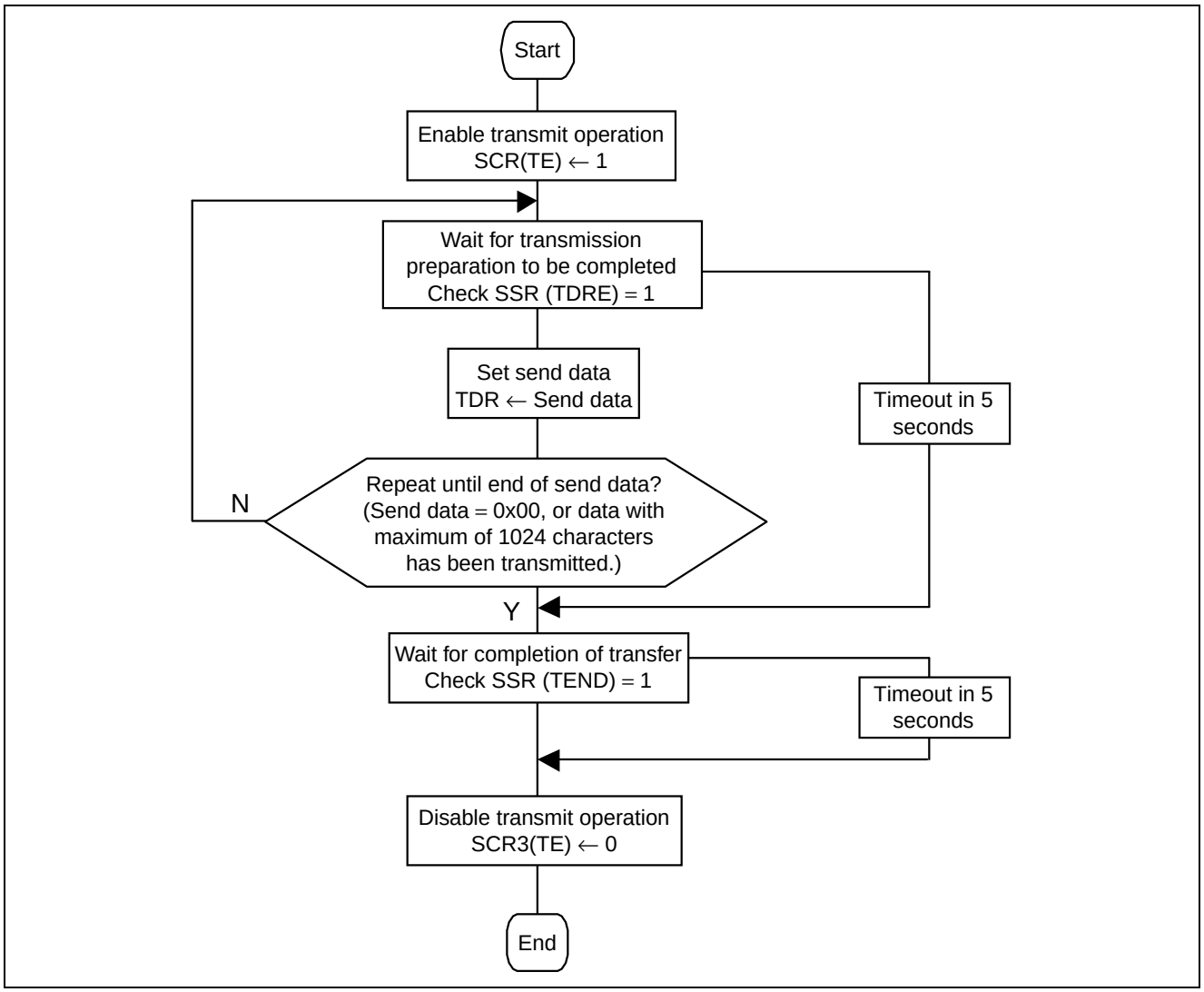
```
com_debug_cmd
: Console command analysis and execution
```



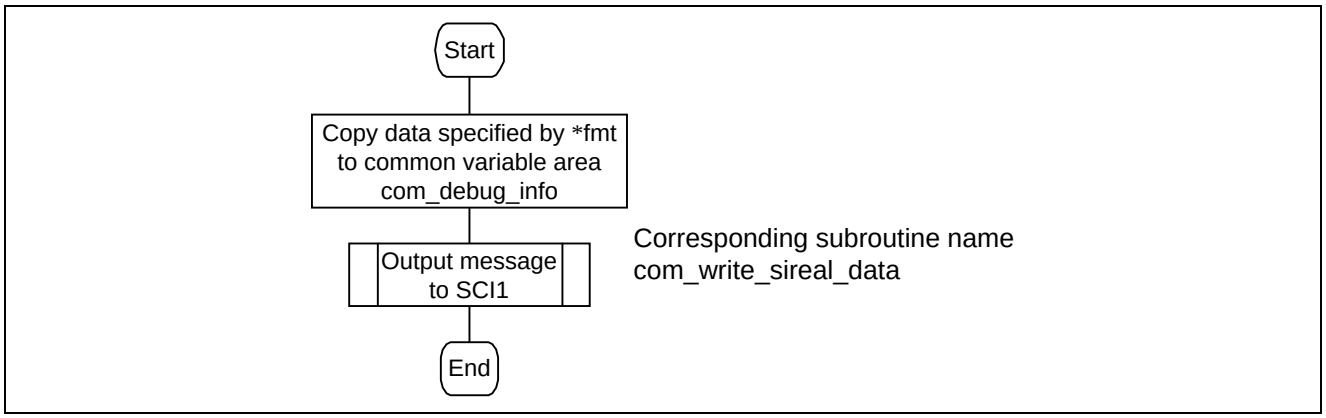
```
com_read_sirial_data
: Reception of a message from the SCI interface
   Receive data not longer than 40 characters is received
   in the common variable area (com_sci3_rcv_buf).
```



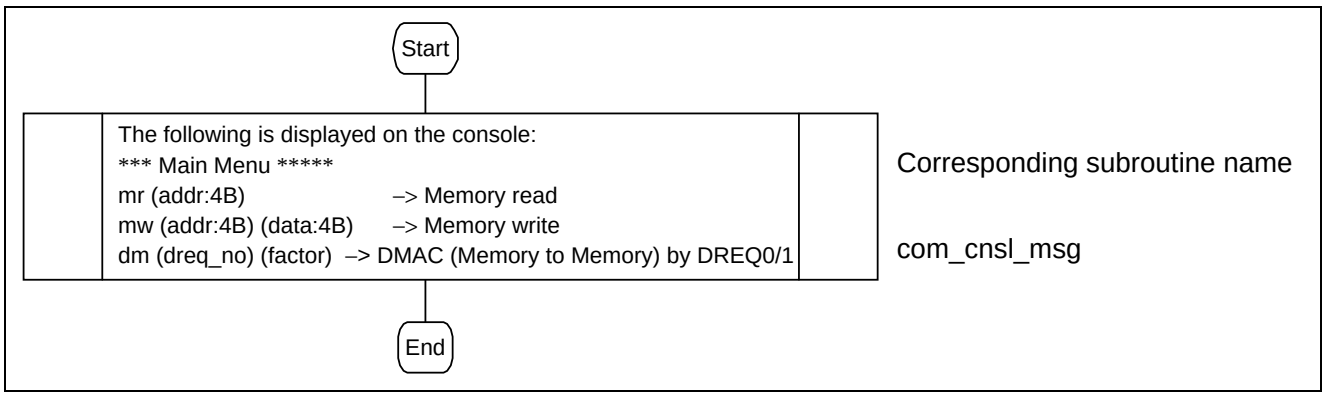
```
com_write_sireal_data ( char *p )
: Transmission of a message to the SCI interface
   *p : Address where message data is stored
```



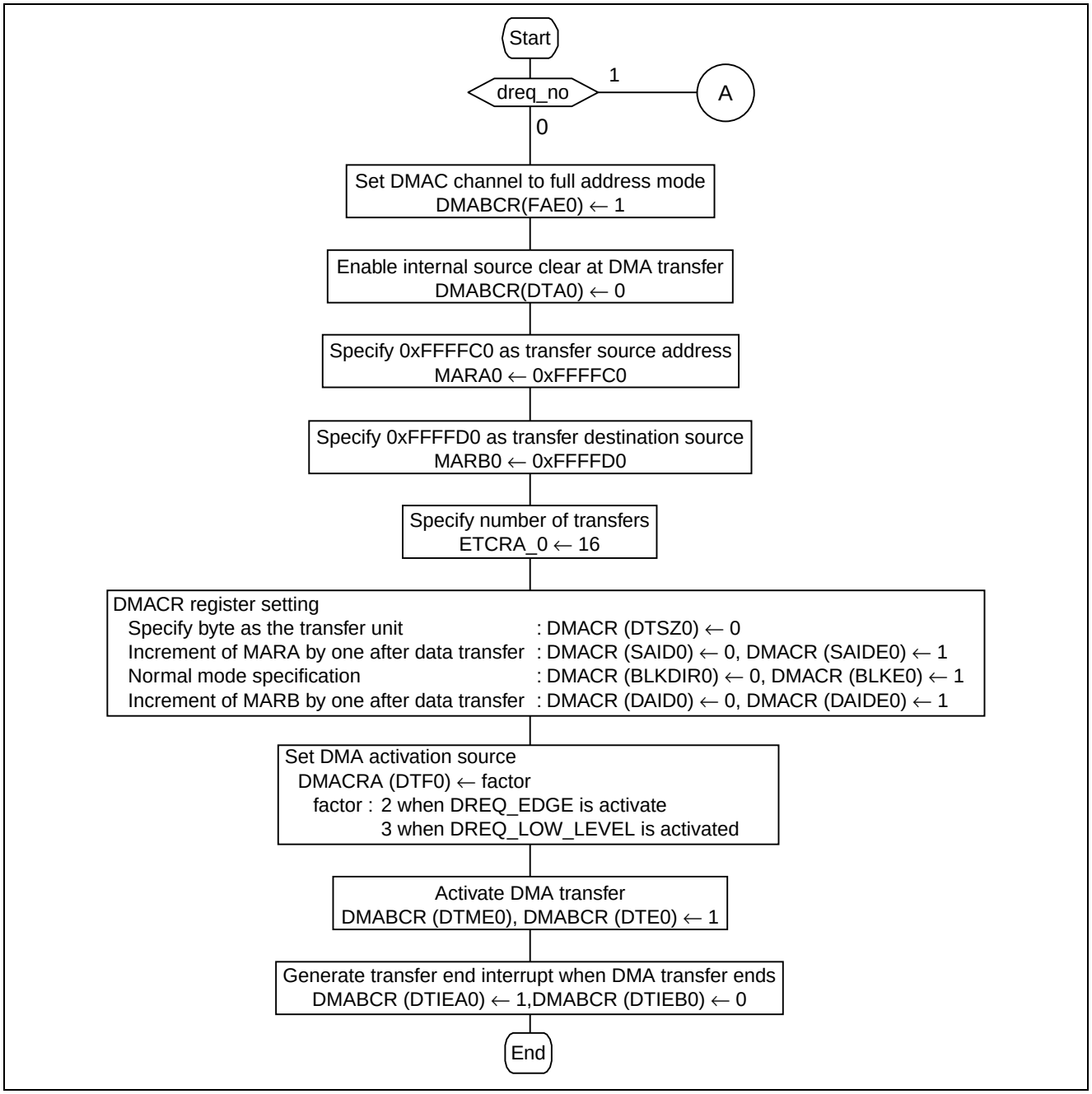
```
com_cnsl_msg(char *fmt, ...)
: Transmission of a message to the console
   *fmt : Address where variable-length message data is stored
```

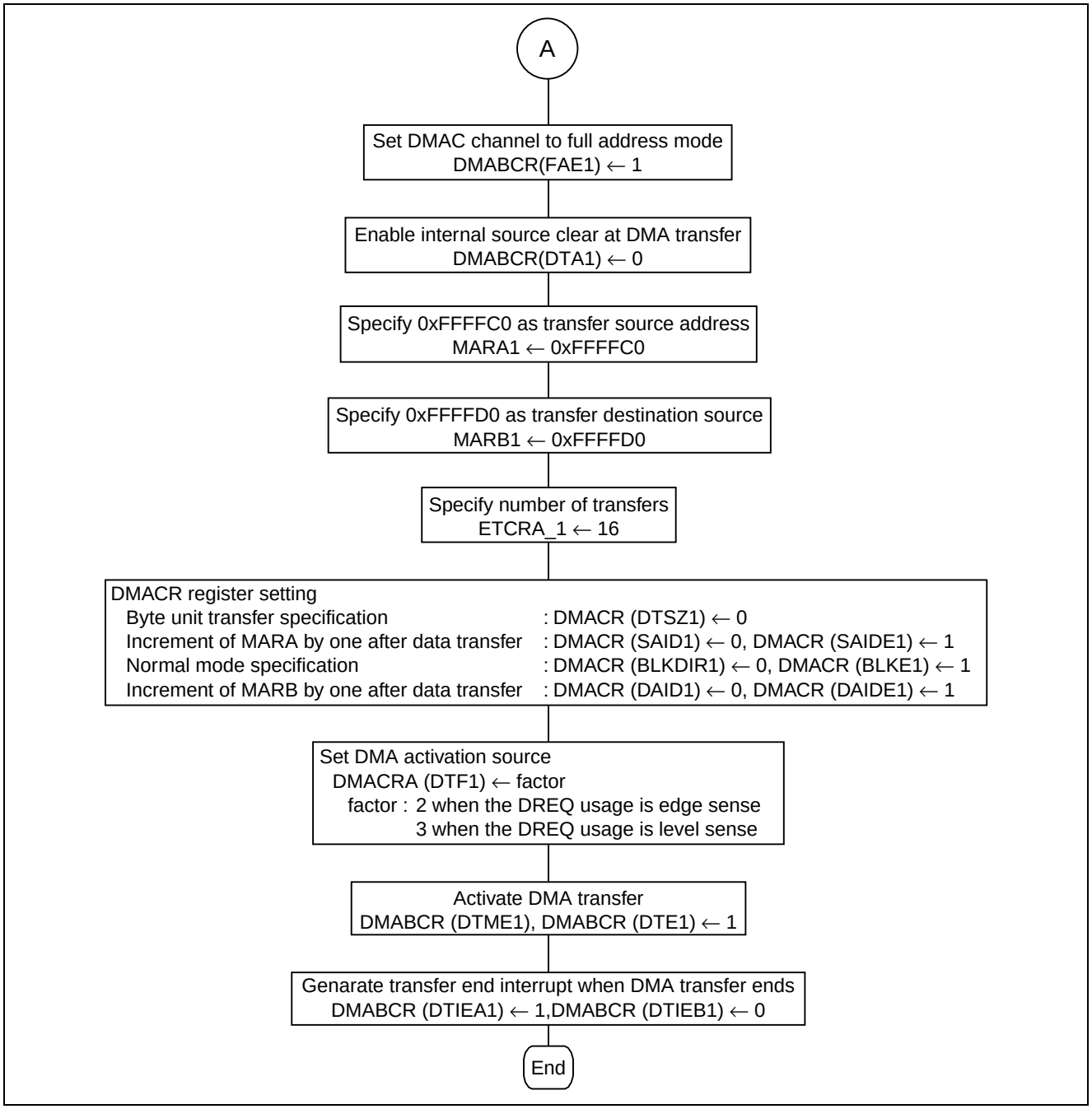



```
com_menu_disp
: Display of the operation menu on the console
```



```
void set_dma_req_dreq ( unsigned char dreq_no , unsigned char factor)
 : Performs DMA transfer using DREQ0 or DREQ1 as the activation source.
   Copies data at 0xFFFFC0 to 0xFFFFCF to 0xFFFFD0 to 0xFFFFDF on an internal
   RAM chip.
     dreq_no
      DREQ_0 (0)    : Uses DREQ0 as the activation source.
      DREQ_1 (1)    : Uses DREQ1 as the activation source.
     factor
      DREQ_EDGE      (2) : Activates the DMAC at the falling edge of DREQ.
      DREQ_LOW_LEVEL (3) : Activates the DMAC when a low-level DREQ is
                           detected.
```




A
Set DMAC channel to full address mode
DMABCR(FAE1) ← 1
Enable internal source clear at DMA transfer
DMABCR(DTA1) ← 0
Specify 0xFFFFC0 as transfer source address
MARA1 ← 0xFFFFC0
Specify 0xFFFFD0 as transfer destination source
MARB1 ← 0xFFFFD0
Specify number of transfers
ETCRA_1 ← 16
DMACR register setting
Byte unit transfer specification : DMACR (DTSZ1) ← 0
Increment of MARA by one after data transfer : DMACR (SAID1) ← 0, DMACR (SAIDE1) ← 1
Normal mode specification : DMACR (BLKDIR1) ← 0, DMACR (BLKE1) ← 1
Increment of MARB by one after data transfer : DMACR (DAID1) ← 0, DMACR (DAIDE1) ← 1
Set DMA activation source
DMACRA (DTF1) ← factor
factor : 2 when the DREQ usage is edge sense
3 when the DREQ usage is level sense
Activate DMA transfer
DMABCR (DTME1), DMABCR (DTE1) ← 1
Genarate transfer end interrupt when DMA transfer ends
DMABCR (DTIEA1) ← 1,DMABCR (DTIEB1) ← 0
End

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Mar.16.04	—	First edition issued

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