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Renesas Electronics Corporation

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# H8S/2200 Series

## Block Transfer

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### Introduction

Outputs data set in ROM to I/O ports and outputs pulse each time a falling edge of an external signal is detected.

### Target Device

H8S/2215

### Contents

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### 1. Specifications

As shown in figure 1, this sample task transfers 30-byte (6 bytes  $\times$  5 blocks) data set in ROM to I/O ports and outputs pulse each time a falling edge of the external signal IRQ1 is detected.

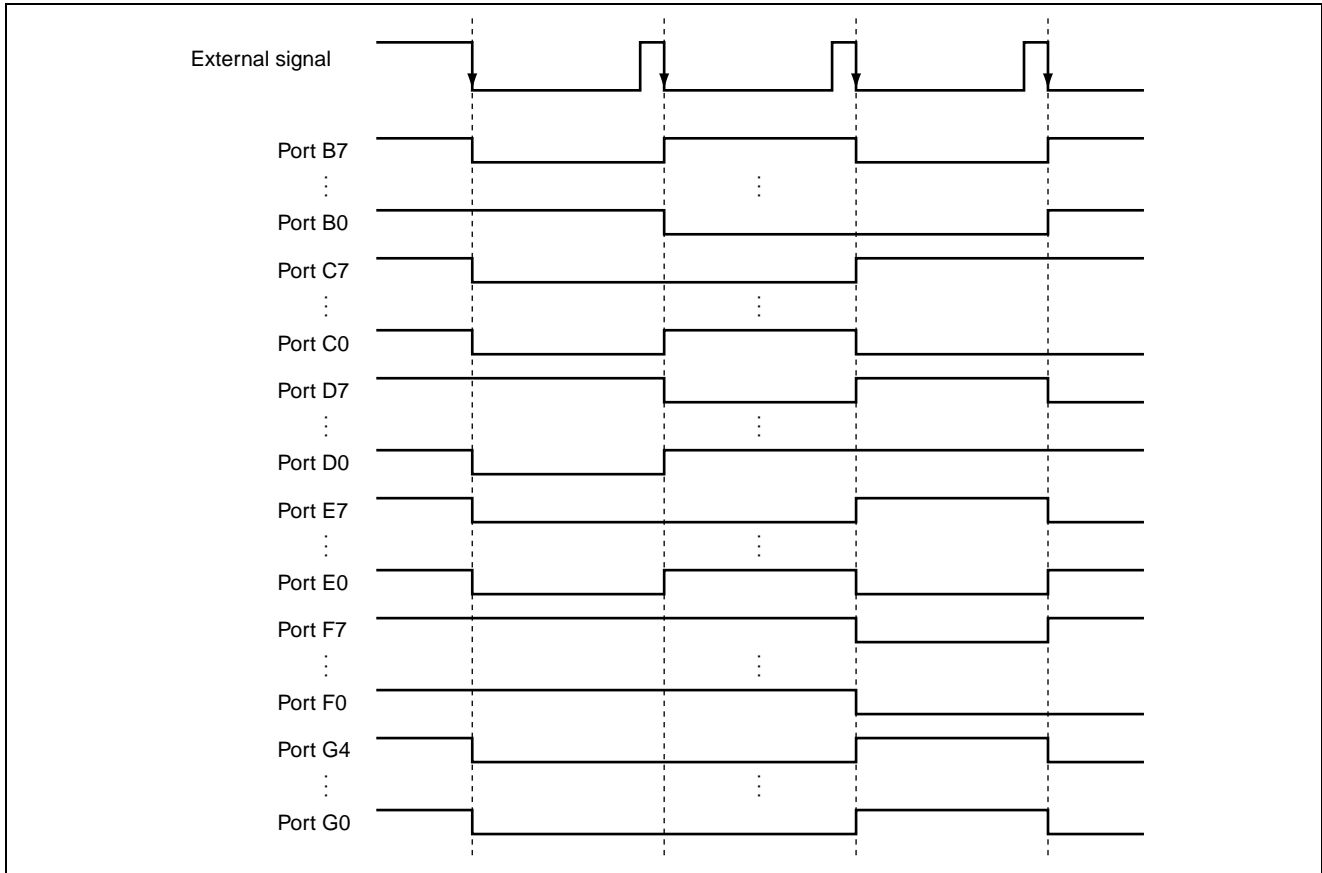


Figure 1 Waveform Output Example

### 2. Description of Functions

1. This sample task starts up DTC each time it detects a falling edge of IRQ1 and outputs 6-byte data to port G from port B.
  - A. The block diagram of DTC used by this sample task is shown in figure 2. This sample task uses the following functions for transferring blocks:
    - Function that starts up DTC on an external request (DTC startup by IRQ)
    - Function that transfers data in the unit of block at DTC startup (block transfer mode)

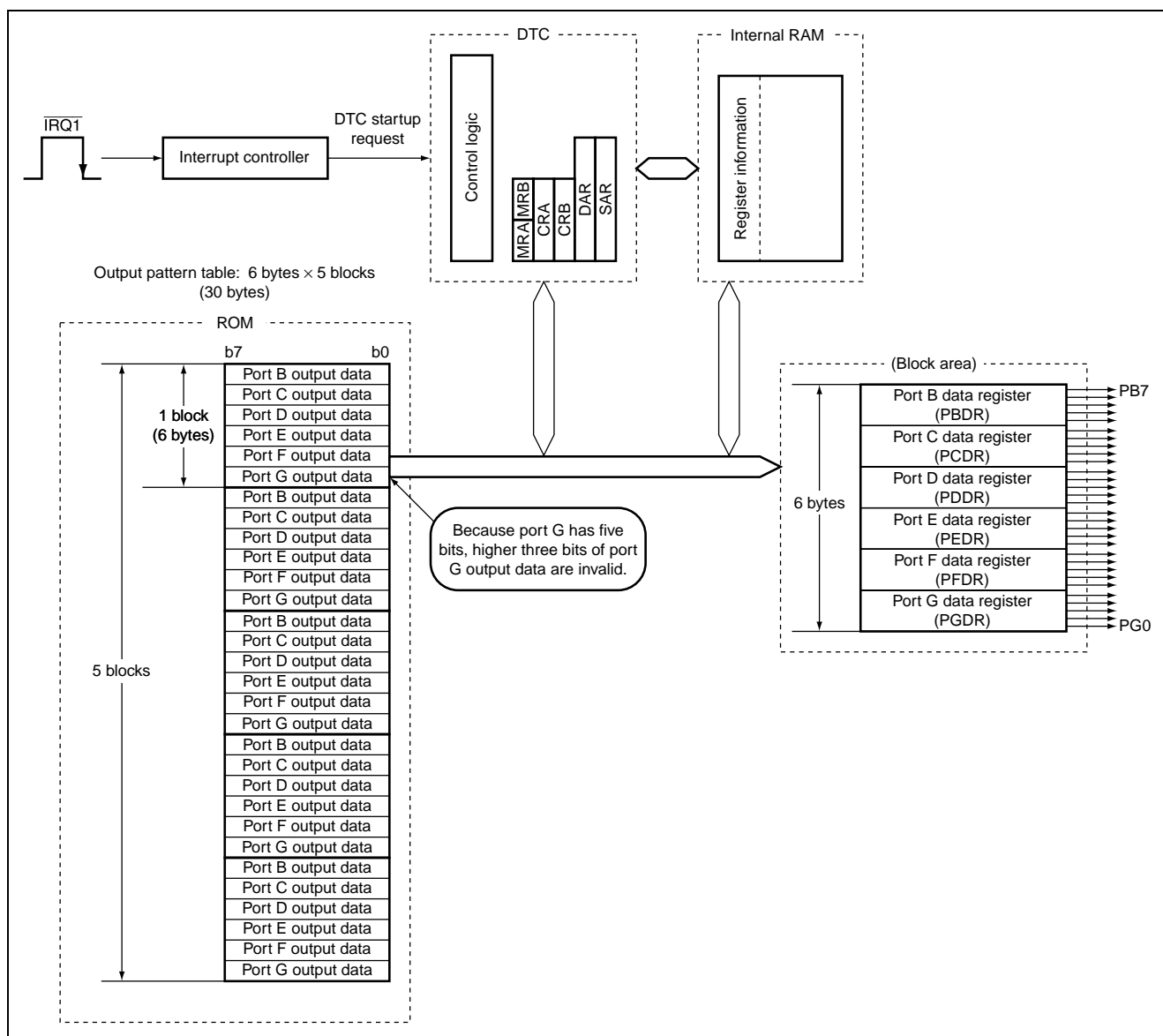
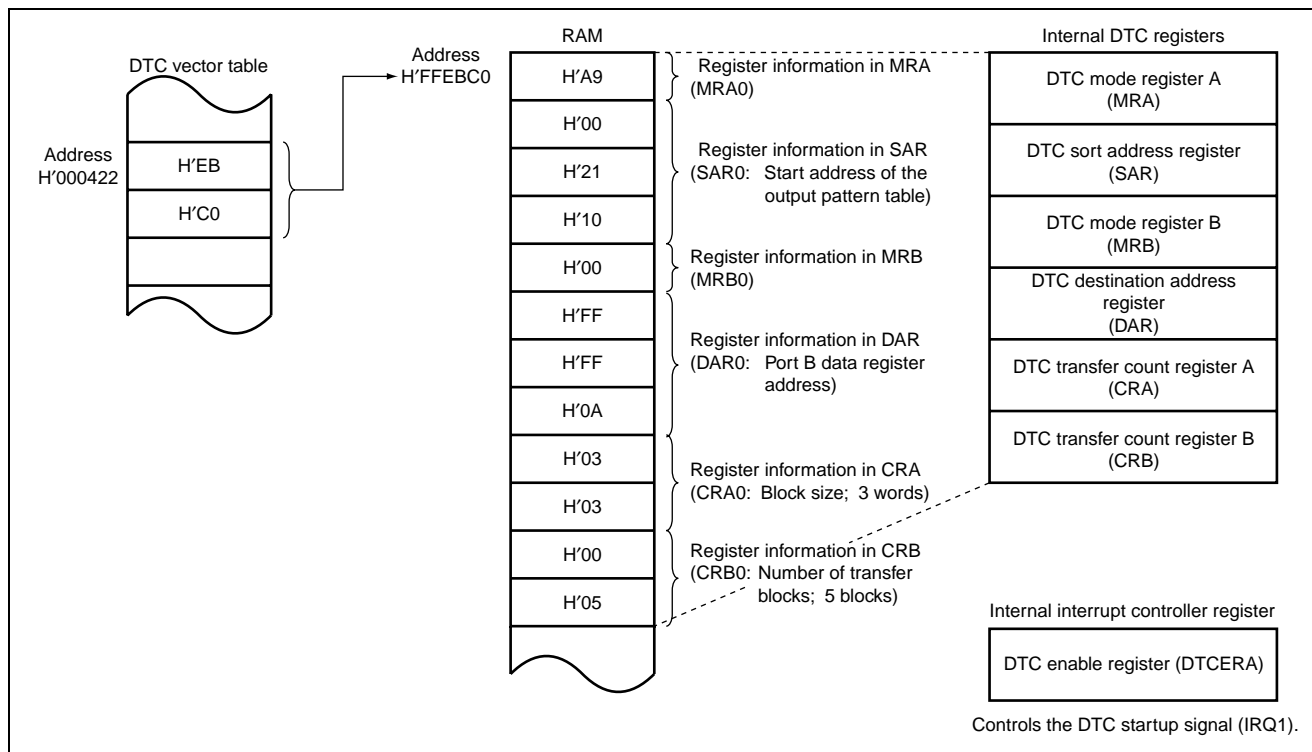


Figure 2 Block Diagram of Block Transfer by DTC

B. The DTC vector table and its allocation in memory are shown in figure 3. DTC register information is allocated in the order of MRA, SAR, MRB, DAR, CRA, and CRB from address H'FFEB0.



**Figure 3 DTC Vector Table and Allocation Example in Memory**

2. Function allocation of this sample task is shown in table 1. This sample task allocates functions as shown in table 1 to transfer blocks.

**Table 1 Assignment of Functions**

DTC Function	Description
MRA, MRB	Controls DTC mode.
SAR	Specifies the transfer source address.
DAR	Specifies the transfer destination address.
CRA	Specifies the number of times to transfer data.
CRB	Specifies the transfer count in block transfer mode.
DTCER	Enables/disables of DTC startup by each interrupt source.

### 3. Principles of Operation

- The principles of operations used of block transfer by DTC are shown in figure 4. This sample task performs hardware and software processing using the timing shown in figure 4 to transfer blocks.

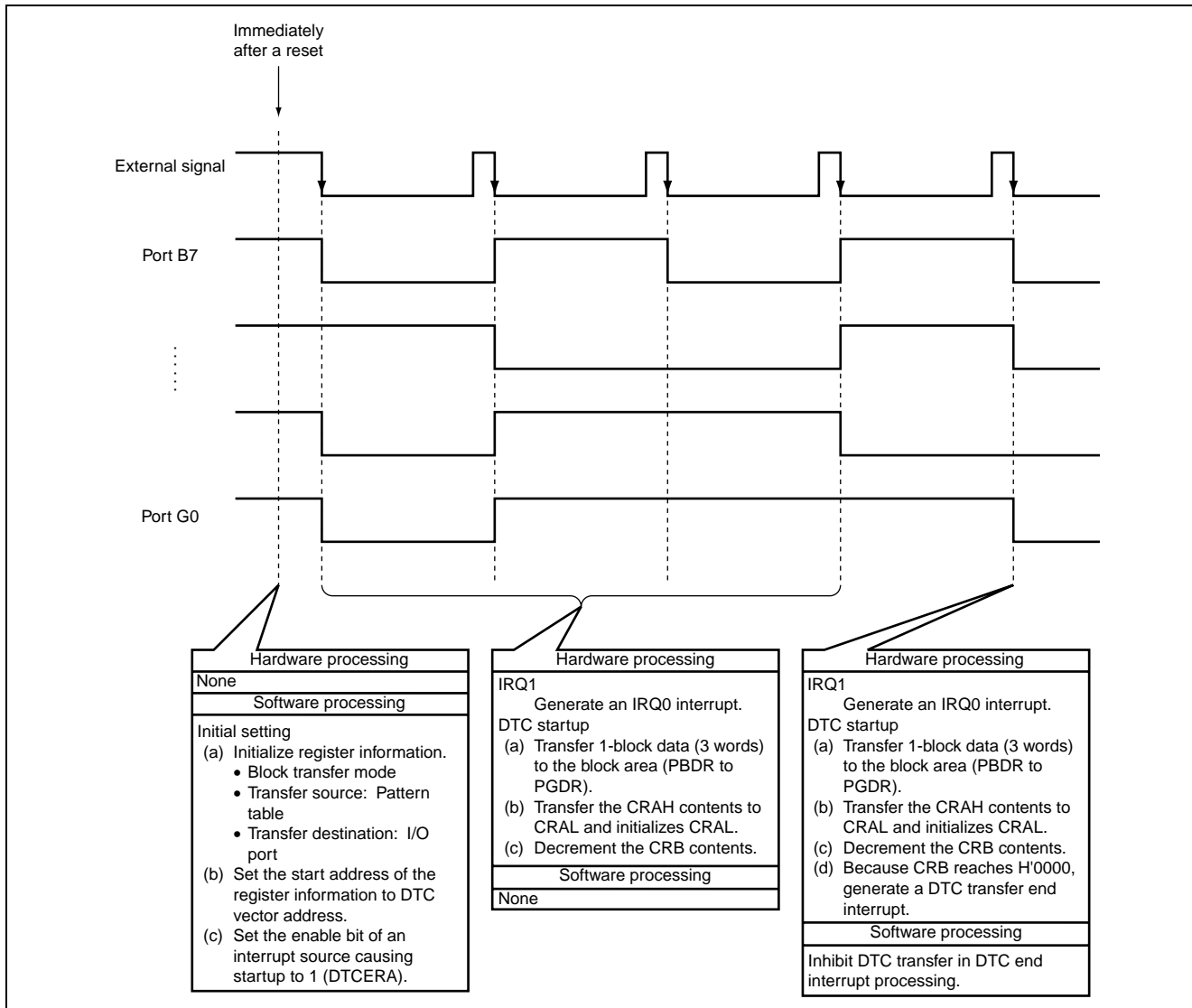


Figure 4 Principles of Operations Used for Block Transfer

## 4. Description of Software

### 1. Description of Modules

Module Name	Label Name	Function
Main routine	blkmn	Performs initial setting for DTC.
Transfer completion	txend	Starts up by a DTC transfer end interrupt and inhibits transfer by DTC.

### 2. Description of Arguments

This sample task uses no inter-module arguments.

### 3. Description of Internal Registers Used

Register Name	Function	Used in
DTCER	Enables DTC startup by an IRQ1 interrupt.	Main routine
MSTPCR	Controls DTC module stop mode.	
ISCLR	Sets an interrupt request at detection of a falling edge of IRQ1.	
IER	Enables an IRQ1 interrupt.	
ISR	Indicates the IRQ1 input status.	

### 4. RAM Usage

Table below describes RAM usage in this sample task.

Label Name	Function	Data Length	Used in
MRA0	Sets DTC0 in block transfer mode.	unsigned char	Main routine
MRB0	Inhibits an interrupt to the CPU.	unsigned char	
SAR0	Sets the transfer source address (PATTBL1).	unsigned long	
DAR0	Sets the transfer destination address (PBDR).	unsigned long	
CRA0	Sets the block size.	unsigned short	
CRB0	Sets the number of blocks to be transferred.	unsigned short	
txendf	Transfer end flag	int	Transfer end

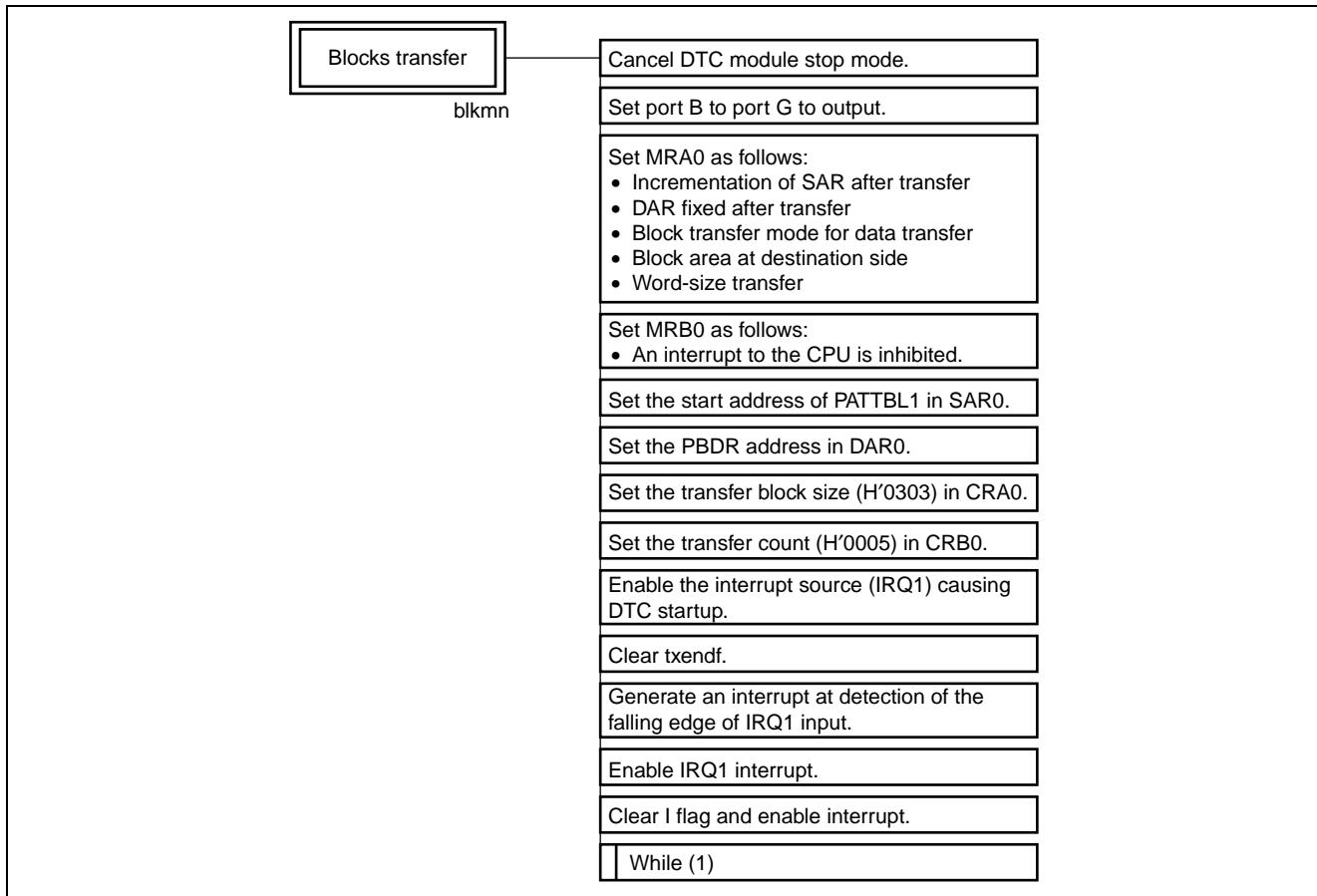
### 5. Description of Data Table

Table Name	Function	Data Length	Data Capacity
PATTBL1	Sets an output pattern.	unsigned short	15 words

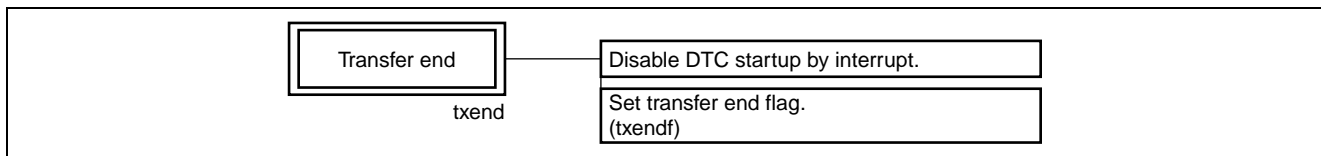


### 5. PAD

#### 1. Main Routine



#### 2. Transfer End



### Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16.04	—	First edition issued

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