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Renesas Electronics Corporation

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H8S/2200 Series

Timing Function Using WDT

Introduction

Time data is created using the WDT's interval timer function.

Target Device

H8S/2215

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1. Overview

Time data is created using the WDT's interval timer function.

2. Configuration

The configuration on which the contents of this Application Note has been confirmed is shown in table 1.

Table 1 Configuration on which Operation was Confirmed

No.	Parts	Specifications
1	Solution Engine H8S/2215 CPU board (from Hitachi ULSI Systems)	Board power supply input: 5 VDC Operating frequency: 16 MHz MCU operating mode: 7

3. Description of Functions

An interrupt is generated every 100 ms by the WDT's interval timer function. The interval timer start is set to 0 hours, 0 minutes, 0 seconds, and timing is started. The hour, minute, and second data areas assigned to internal RAM are updated every second.

When timing is performed up to 23 hours, 59 minutes, 59 seconds, the timer is set to 0 hours, 0 minutes, 0 seconds again, and timing is resumed.

Internal RAM Area Name	Data Length	Function
time_sec	unsigned char	Second data storage area
time_min	unsigned char	Minute data storage area
time_hour	unsigned char	Hour data storage area

A signal toggled every second is output from the PG0 pin of the I/O port.

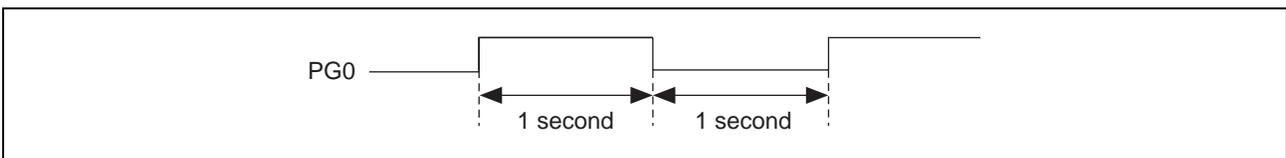


Figure 1 Toggled Signal Output from PG0

4. Principles of Operation

4.1 Initialization Processing

Before timing processing is performed, the microcomputer is started up and the following initial internal register settings are made.

(1) Low-Power Consumption Control and Clock Oscillator Initialization

Register Name

← Set Value	Bit	Bit Name	Set Value	Description
LPWRCR	7:4	—	0000	
← H'03	3	RFCUT	0	Uses built-in feedback resistance control
	2	—	0	
	1:0	STC[1:0]	11	PLL is bypass
MSTPCRA	7	MSTPA7	0	DMAC module operation
← H'0D	6	MSTPA6	0	DTC module operation
	5	MSTPA5	0	TPU module operation
	4	MSTPA4	0	TMR module operation
	3:2	MSTPA[3:2]	11	Reserved
	1	MSTPA1	0	A/D converter operation
	0	MSTPA0	1	Reserved
	MSTPCRB	7	MSTPB7	0
← H'1F	6	MSTPB6	0	SCI_1 module operation
	5	MSTPB5	0	SCI_2 module operation
	4:1	MSTPB[4:1]	1111	Reserved
	0	MSTPB0	1	USB module stopped
	MSTPCRC	7:6	MSTPC[7:6]	11
← H'DF	5	MSTPC5	0	D/A converter operation
	4:0	MSTPC[4:0]	11111	Reserved

(2) I/O Port Initialization

Bit 0 of the PGDDR for port G is set to the output mode.

Port	Register Name		Bit	Bit Name	Set Value	Description
	← Set Value	Bit				
G	PGDDR	7:5	—		111	
	← H'FF		4:2	PG[4:2]DDR	111	Output (not used)
			1	PG1DDR	1	Output (not used)
			0	PG0DDR	1	Output

4.2 Timing Processing by WDT Interval Timer

(1) Overview

An interrupt is generated every 100 ms using the WDT as the interval timer. Conversion to hour, minute, and second data is performed in interrupt processing.

(2) WDT Settings

WDT related register settings are made in order to operate the WDT in the interval timer mode.

No.	Setting	Set Register
1	TCNT overflow bit cleared	TCSR(OVF) ← 0 after TCSR read
2	<ul style="list-style-type: none"> • Interval timer mode set • TCNT count cycle set to $\phi/8192$ 	TCSR ← H'05
3	Status register reset	RSTCSR ← H'00
4	Timer start and TCNT cleared	TCSR ← H'25
5	TCNT set so that interval interrupt is generated every 100 ms Set value depends on microcomputer operating frequency and TCNT count cycle (set value of CKS[2:0] bits of TCSR).	TCNT ← interval_value set value (In this Application Note, interval_value = H'4F)

(3) WDT Operation

When the above settings are made, a WDT interval timer interrupt is generated after 100 ms.

- a) In interrupt processing, the above WDT settings are made so that an interrupt is generated again after 100 ms.
- b) Signals output from pin PG0 of port G are toggled every ten interval timer interrupts (every second).
- c) Hour, minute, and second data is updated every 10 interval timer interrupts (every second).

5. Sample Program

5.1 File Configuration

The sample program is provided as an HEW (High-performance Embedded Workshop) project. When h8s.hws is executed, HEW is started up and the source program can be referenced or modified. Users who do not have HEW should use an editor or similar software to refer directly to the following source files.

No.	File Name	Purpose
1	resetprg.c	This file is executed from reset vector address 0 when a reset is input to the microcomputer.
2	intprg.c	This file is executed in the event of generation of an interrupt from an interrupt source other than a reset.
3	dbstc.c	Processing that sets the start address and end address of a section used by the _INITSTCT function in resetprg.c in the section initialization table. For the contents, see section 9.10 of the H8S, H8/300 Series C/C++ Compiler, Assembler, and Optimizing Linkage Editor User's Manual. This manual can be obtained from Renesas Technology's home page*.
4	wdt_timer.c	Main routine and interrupt handling routine of this Application Note
5	iodefine.h	H8S/2215 internal register structure definition file Partial modifications are added to the file generated automatically by HEW. See the source code for the location of the modifications.
6	stacksct.h	Defines the stack size.

Note: * <http://www.renesas.com>

5.2 Linkage

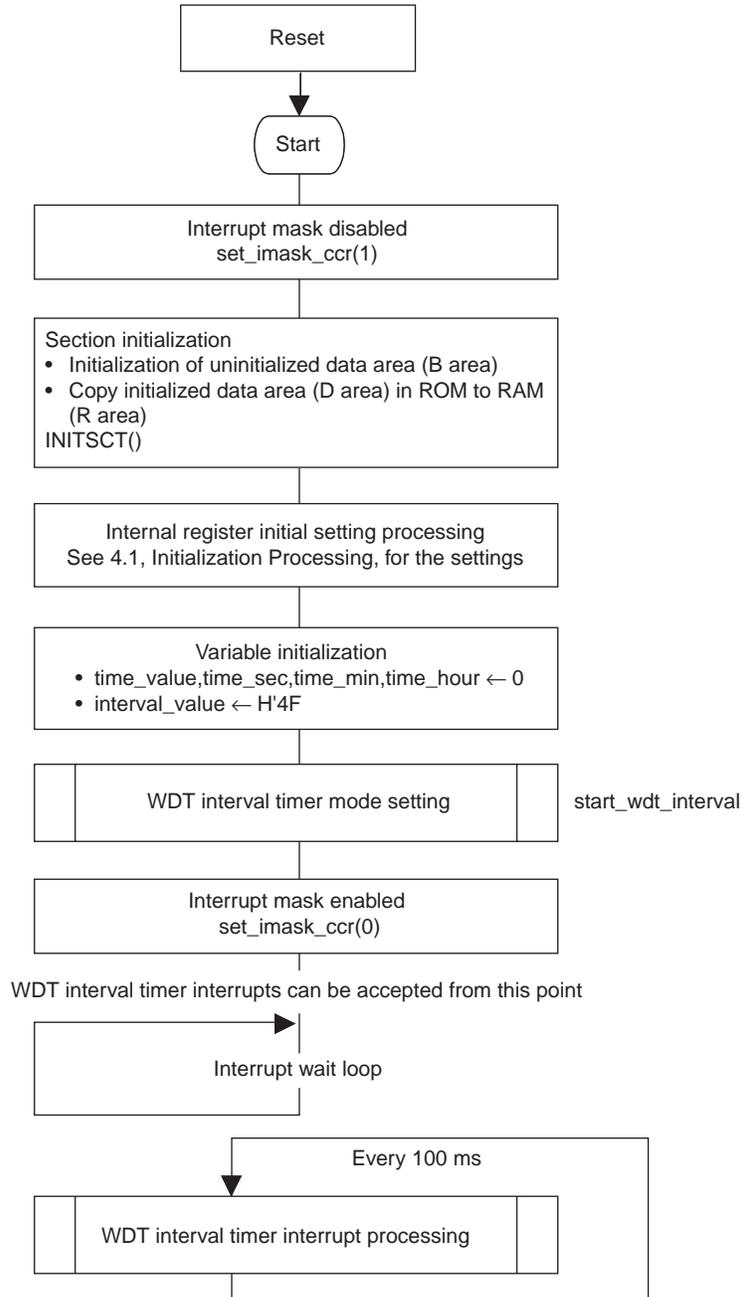
The linkage addresses of the various sections are shown below.

With the HEW project file, referencing and setting can be performed by selecting option –Standard Toolchain option — Link/Librarq tab — Category: section.

Section	Start Address
PResetPRG	H'000400
PIntPRG	
P	H'000800
C\$DSEC	
C\$BSEC	
D	
B	H'FFB000
R	
S	H'FFEDB0

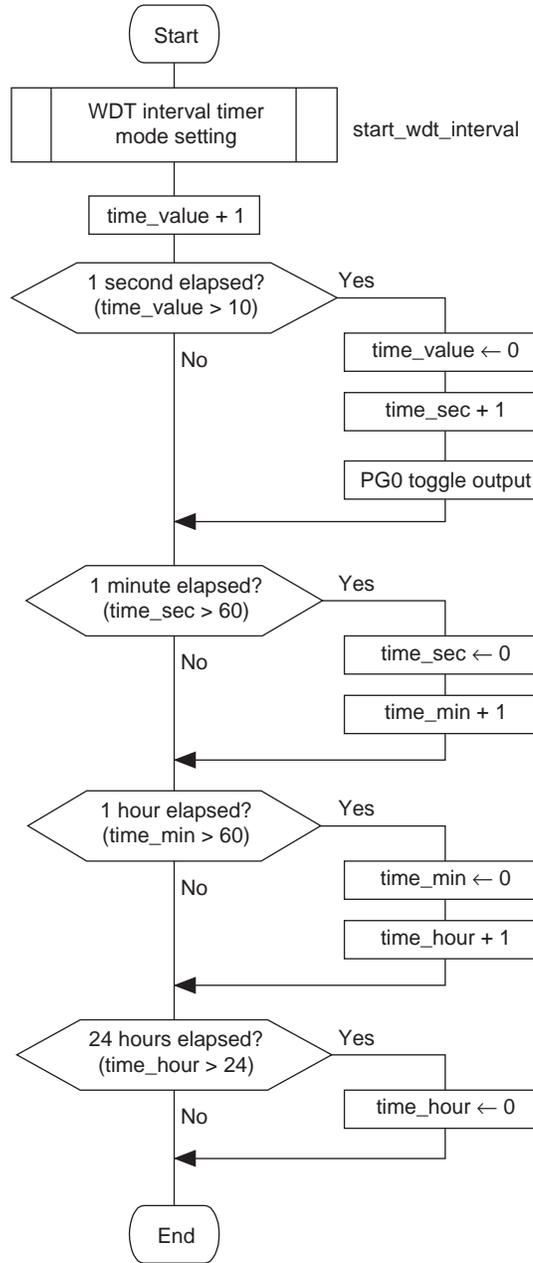
6. Flowcharts

(1) Overall Flow



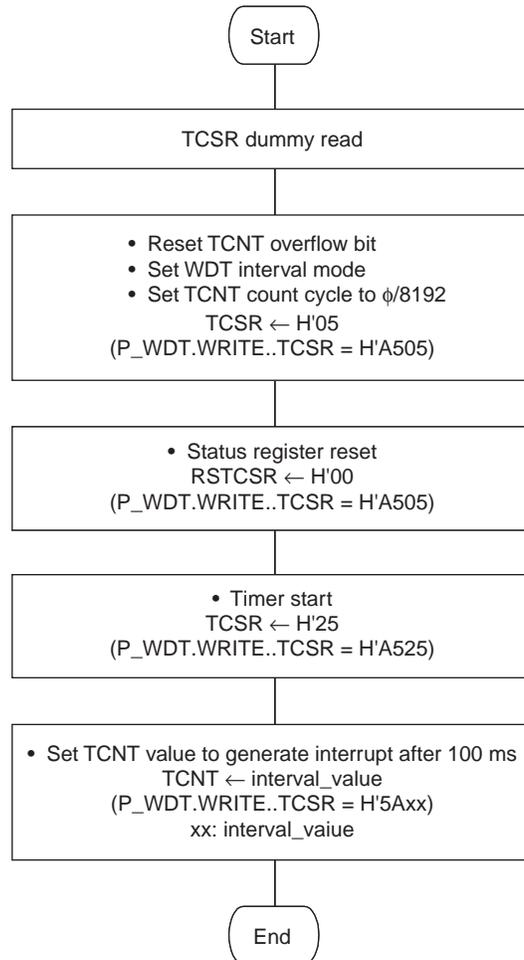
(2) Interrupt Processing

WDT interval timer interrupt processing (interrupt every 100 ms): wovi_int



(3) Detailed Processing

start_wdt_interval



Note: As WDT related registers have a hardware reset operation function, there is a specific writing procedure. See the hardware manual for details.

7. Reference

No.	Document Title	Source
1	H8S/2215 Hardware Manual (REJ09B0140-0400O)	Can be downloaded from Renesas Technology's home page*

Note: * <http://www.renesas.com>

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.03.04	—	First edition issued

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