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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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H8S/2200 Series

8-Bit Timer Overflow Function

Introduction

This application note demonstrates the overflow operation of the 8-bit timer (TMR).

Target Device

H8S/2215

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1. Specifications

1. TCR_1 and TCSR_1 are set to start the counting operation of TCNT_1.
2. When TCNT_1 overflows, the OVF flag in TCSR_1 is set. When the value of TCORA_1, H'0F, matches the counter value, compare-match flag CMFA is set to 1.

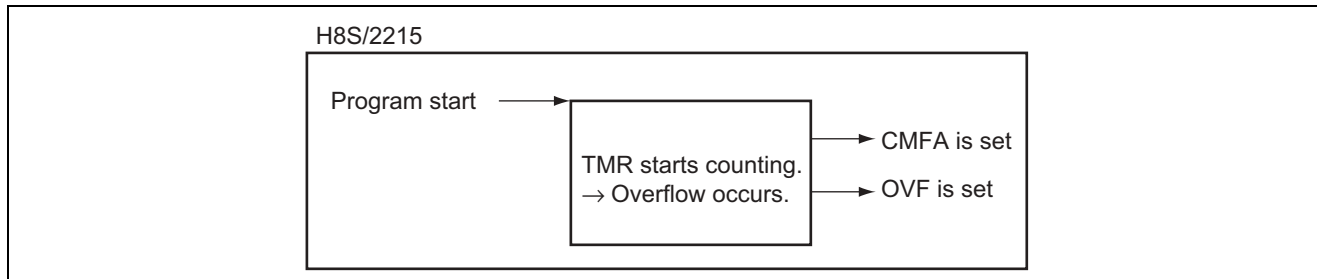


Figure 1 Example of TMR Overflow

2. Description of Functions

1. Figure 2 shows a block diagram of the 8-bit timer, and the following is the description of the block diagram:
 - The timer counter (TCNT) is an 8-bit up counter that can be read or written to. TCNT_0 and TCNT_1 can be used together and can be word-accessed as a 16-bit register. The operating clock is selected by the CKS2 to CKS0 bits in TCR. TCNT can be cleared by an external reset input signal, compare-match A signal, or compare-match B signal, one of which is selected by the CCLR1 and CCLR0 bits in TCR. When TCNT overflows (H'FF → H'00), OVF in TCSR is set to 1. The initial value of TCNT is H'00.
 - The time constant register A/B (TCORA/TCORB) is an 8-bit register that can be read or written to. TCORx_0 and TCORx_1 can also be used together as a 16-bit register and can be word-accessed. TCNT is always compared with the TCORx value and if they match, CMFA in TCSR is set to 1. However, this comparison is disabled in T2 state of a write cycle to TCORx. These match signals (compare-match x) can be used in combination with the settings of OS1 and OS0 bits in TCSR to control timer output from the TMO pin. The initial value of TCORx is H'FF.
 - The timer control register (TCR) selects TCNT input clock, specifies TCNT clearing condition and controls each interrupt request.
 - The timer control/status register (TCSR) contains status flags and controls output on compare-match.

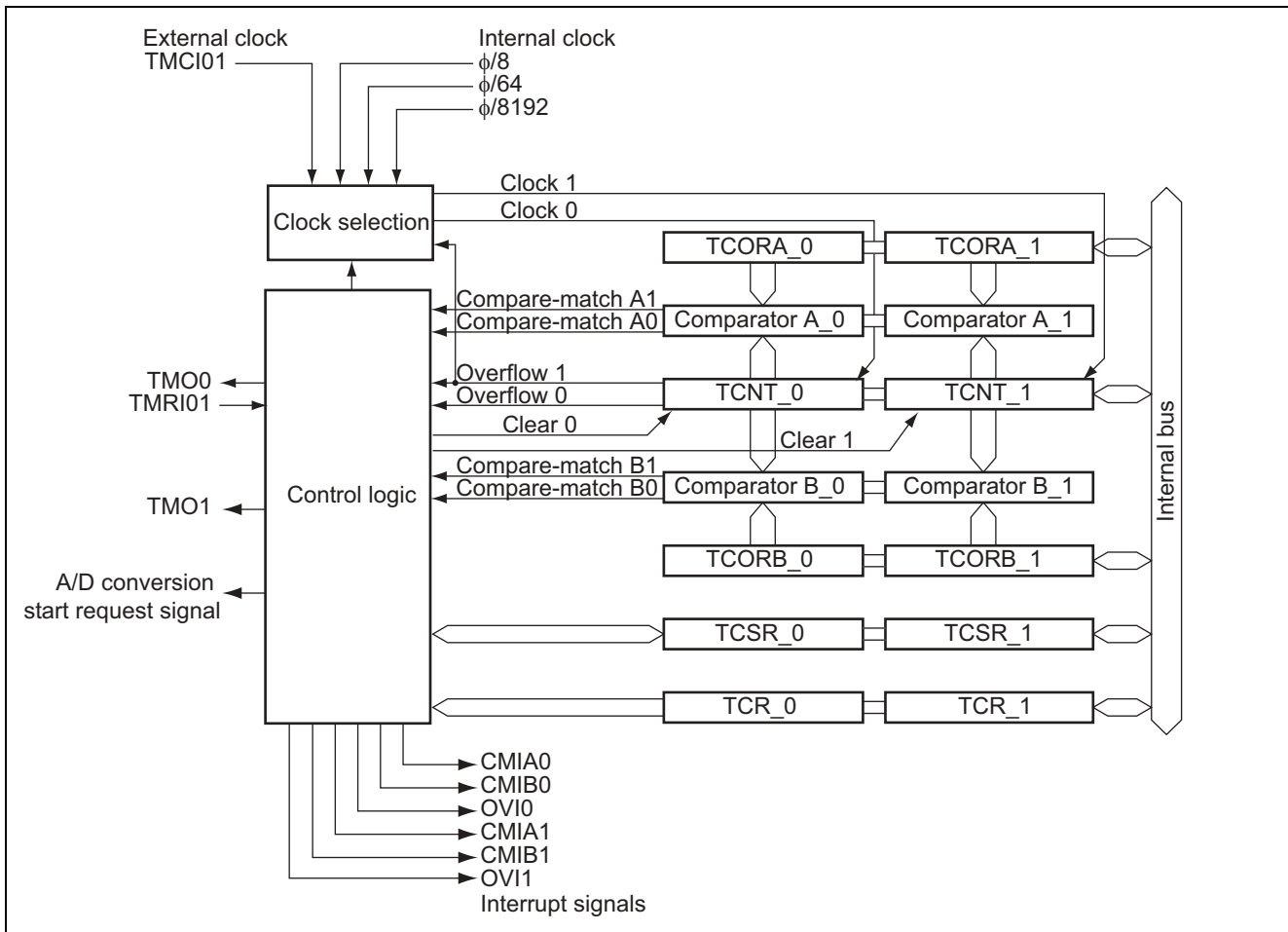


Figure 2 Block Diagram of 8-Bit Timer

2. Table 1 shows the assignment of functions used in this sample task.

Table 1 Assignment of Functions

Elements	Description
TCNT	Provides TCNT_1 count operation. When an overflow occurs, OVF in TCSR_1 is set.
TCORA/TCORB	Sets TCNT period, high-level output, etc.
TCR	TCR_1 is used to control TCNT_1 (selects input clock, TCNT clearing condition, etc.)
TCSR	Contains status flags and sets output level on compare-match.

3. Principles of Operation

Figure 3 illustrates the TMR overflow operation of this sample task, along with the description of hardware and software processing.

1. TCR_1 and TCSR_1 are set to configure a counter operation, and TCNT_1 starts counting.
2. When the TCNT_1 value matches TCORA_1, which was set to H'0F, compare-match flag CMFA in TCSR_1 is set to 1.
3. When TCNT_1 overflows, the OVF flag in TCSR_1 is set.

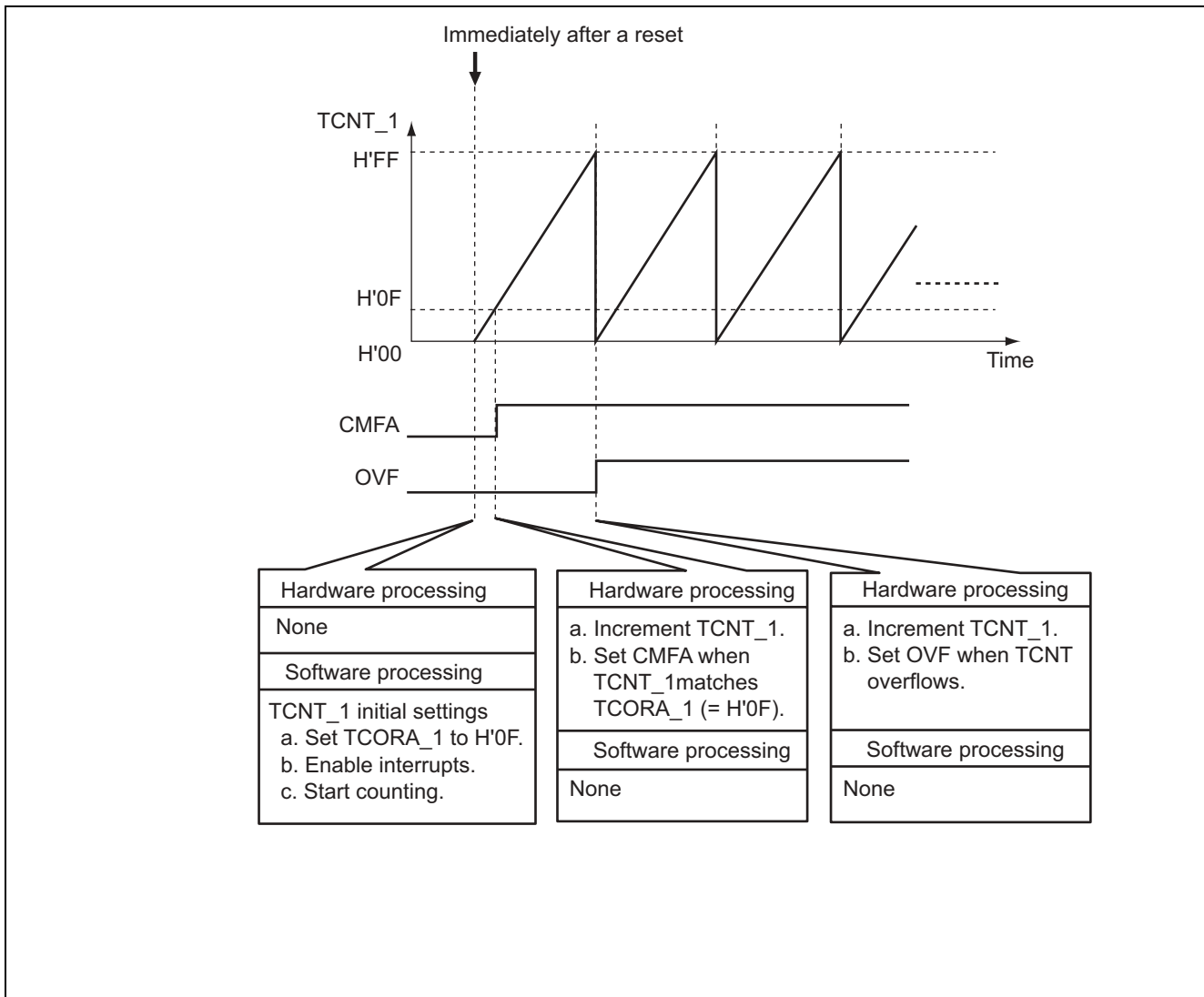


Figure 3 8-Bit Timer Overflow Operation

4. Description of Software

4.1 Module

Table 2 describes the module used in this sample task.

Table 2 Description of Modules

Module	Label	Function
Main routine	main	Sets data for compare-match with TCNT_1 in TCORA_1 and starts counting by TCNT_1. When TCNT_1 matches TCORA_1, the CMFA flag is set; TCNT overflow then follows.

4.2 Arguments

This sample program does not use arguments.

4.3 Internal Registers

The internal registers used in this sample task are described in table 3.

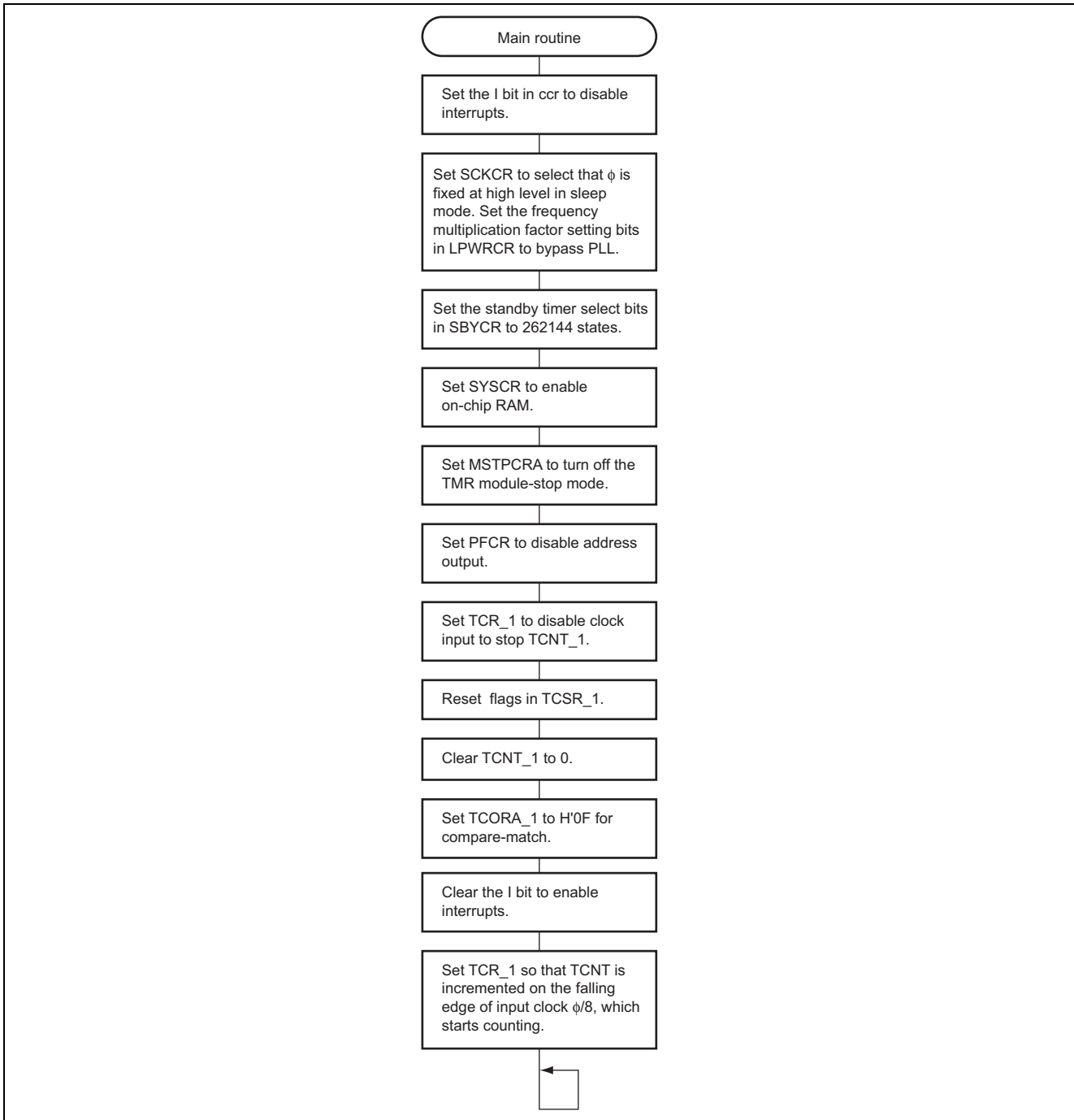
Table 3 Description of Internal Registers

Register	Function	Address	Setting
TCNT_1	Timer Counter 8-bit up counter that can be read or written to	H'FFFF71	H'00
TCORA_1	Time Constant Register A 8-bit register that can be read or written to	H'FFFF6D	H'0F
TCR_1	CMIEB Timer Control Register (Compare-Match Interrupt Enable B) When CMIEB = 0, CMFB interrupt request (CMIB) is disabled. When CMIEB = 1 CMFB interrupt request (CMIB) is enabled.	H'FFFF69	0
	Bit 7		
CMIEA	Timer Control Register (Compare-Match Interrupt Enable A) When CMIEA = 0, CMFA interrupt request (CMIA) is disabled. When CMIEA = 1, CMFA interrupt request (CMIA) is enabled.	H'FFFF69	0
	Bit 6		
OVIE	Timer Control Register (Timer Overflow Interrupt Enable) When OVIE = 0, OVF interrupt request (OVI) is disabled. When OVIE = 1, OVF interrupt request (OVI) is enabled.	H'FFFF69	0
	Bit 5		
CCLR1	Timer Control Register (Counter Clear 1, 0)	H'FFFF69	0, 0
CCLR0	When CCLR1 and CCLR0 = 00, clearing of TCNT_1 is disabled.	Bit 4	
		Bit 3	
CKS2	Timer Control Register (Clock Select 2 to 0)	H'FFFF69	0, 0, 1
CKS1	When CKS2, CKS1 and CKS0 = 000, clock input is disabled.	Bits 2 to 0	
CKS0	When CKS2, CKS1 and CKS0 = 001, TCNT_1 is incremented on the falling edge of the internal clock $\phi/8$.		

Register	Function	Address	Setting
TCSR_1	CMFB Timer Control/Status Register (Compare-Match Flag B) CMFB = 0 indicates that TCNT does not match TCORB. CMFB = 1 indicates that TCNT matches TCORB.	H'FFFF6B Bit 7	0
	CMFA Timer Control/Status Register (Compare-Match Flag A) CMFA = 0 indicates that TCNT does not match TCORA. CMFA = 1 indicates that TCNT matches TCORA.	H'FFFF6B Bit 6	0
	OVF Timer Control/Status Register (Timer Overflow Flag) OVF = 0 indicates that a TCNT overflow has not occurred. OVF = 1 indicates that a TCNT overflow has occurred.	H'FFFF6B Bit 5	0
	ADTE Timer Control/Status Register (A/D Trigger Enable) When ADTE = 0, A/D conversion start request generated on compare-match A is disabled. When ADTE = 1, A/D conversion start request generated on compare-match A is enabled.	H'FFFF6B Bit 4	0
	OS3 Timer Control/Status Register (Output Select 3, 2)	H'FFFF6B	0, 0
	OS2 When OS3 and OS2 = 00, TMO pin output does not change on compare-match B.	Bit 3 Bit 2	
	OS1 Timer Control/Status Register (Output Select 1, 0)	H'FFFF6B	0, 0
	OS0 When OS1 and OS0 = 00, TMO pin output does not change on compare-match A.	Bit 1 Bit 0	

5. Flowchart

1. Main routine



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16, 2004	—	First edition issued

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