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H8S/2200 Series

8-Bit Timer Compare-Match Function

Introduction

This application note demonstrates the compare-match operation of the 8-bit timer (TMR).

Target Device

H8S/2215

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1. Specifications

1. Output pulse period is set in TCORA, and the count value for low-level output is set in TCORB.
2. According to TCR_0 and TCSR_0 settings, TCNT_0 starts counting. A pulse signal of the duty cycle which is determined by TCORA and TCORB settings is output from TMO0 (pin 98).
3. Period f and duty cycle are set according to the following formula:

f = (TIOCRA_0 setting value + 1) × (1/(ϕ/8)) Note: ϕ = 16 MHz
In this sample task, f = (170 + 1) × (1/(ϕ/8)) = 85.5 μs Note: H'AA => 170
Duty cycle = (High-level pulse width × (1/(ϕ/8)))/f
In this sample task, duty cycle = (((170 + 1) – (85 + 1)) × (1/(ϕ/8))/85.5 μs) × 100 % Note: H'55 => 85
= (42.5 μs/85.5 μs) × 100 %
= 49.7 %

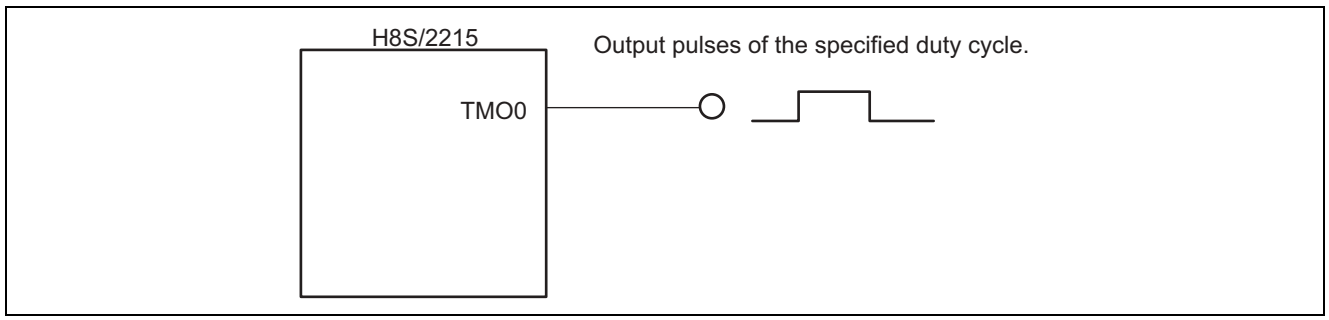


Figure 1 Example of TMR Pulse Output with Controllable Duty Cycle

2. Description of Functions

1. Figure 2 shows a block diagram of the 8-bit timer, and the following is the description of the block diagram:
   - The timer counter (TCNT) is an 8-bit up counter that can be read or written to. TCNT_0 and TCNT_1 can be used together and can be word-accessed as a 16-bit register. The operating clock is selected by the CKS2 to CKS0 bits in TCR. TCNT can be cleared by an external reset input signal, compare-match A signal, or compare-match B signal, one of which is selected by the CCLR1 and CCLR0 bits in TCR. When TCNT overflows (H'FF → H'00), OVF in TCSR is set to 1. The initial value of TCNT is H'00.
   - The time constant register A/B (TCORA/TCORB) is an 8-bit register that can be read or written to. TCORx_0 and TCORx_1 can also be used together as a 16-bit register and can be word-accessed. TCNT is always compared with the TCORx value and if they match, CMFA in TCSR is set to 1. However, this comparison is disabled in T2 state of a write cycle to TCORx. These match signals (compare-match x) can be used in combination with the settings of OS1 and OS0 bits in TCSR to control timer output from the TMO pin. The initial value of TCORx is H'FF.
   - The timer control register (TCR) selects TCNT input clock, specifies TCNT clearing condition and controls each interrupt request.
   - The timer control/status register (TCSR) contains status flags and controls output on compare-match.

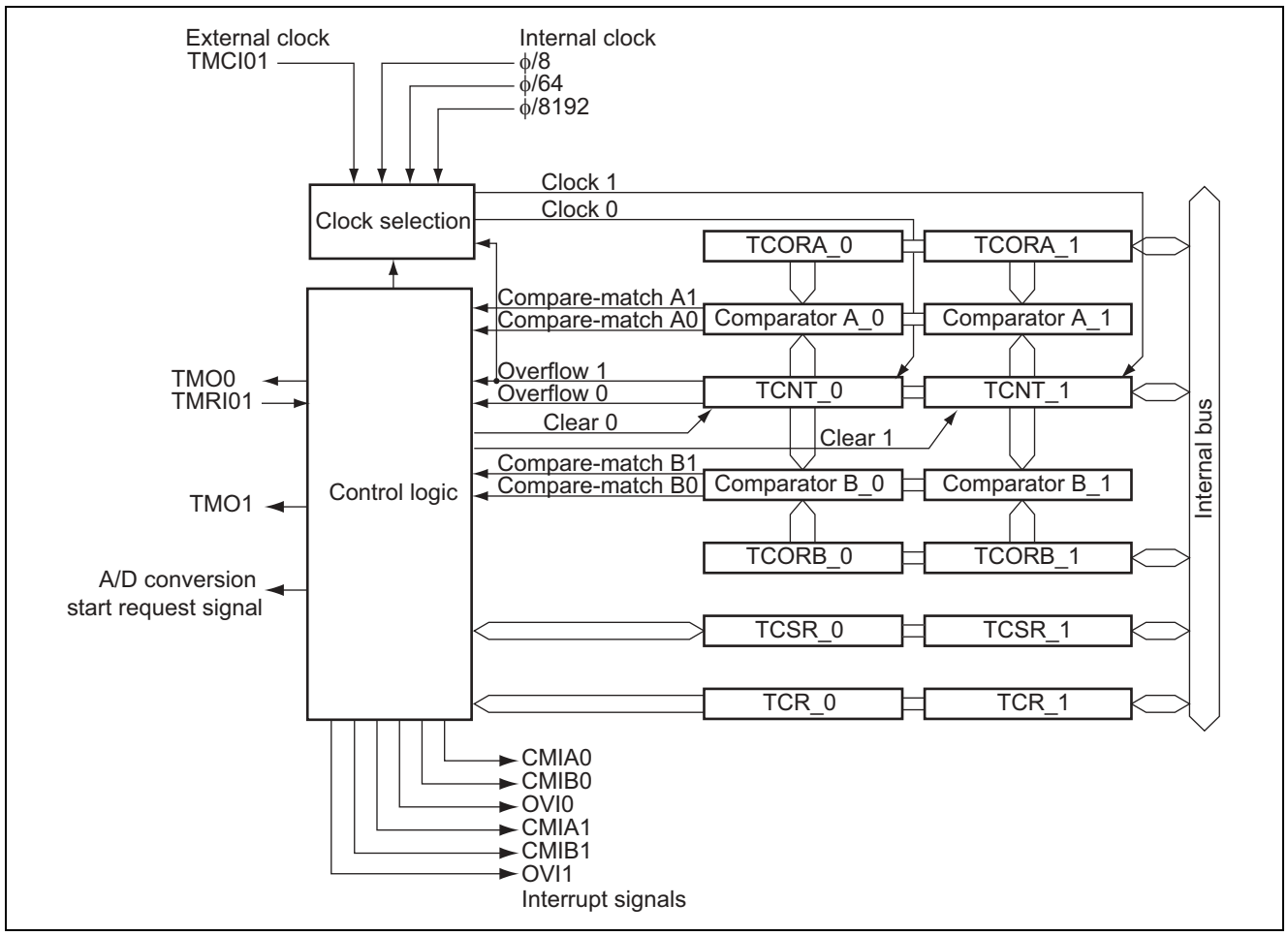


Figure 2 Block Diagram of 8-Bit Timer

2. Table 1 shows the assignment of functions used in this sample task.

Table 1 Assignment of Functions

Elements	Description
TCNT	Timer counter which is compared with TCORA and TCORB.
TCORA/TCORB	TCORA is used to set the period for TCNT_0 and TCORB used to count low-level output.
TCR	Controls TCNT_0 (sets φ/8 as the input clock, TCNT clearing condition, etc.)
TCSR	Contains status flags and sets output level on compare-match.

3. Principles of Operation

Figure 3 illustrates the operation of this sample task. A pulse signal of a specified duty cycle is output using the TMR's compare-match function through the hardware and software processing shown in the figure.

1. The period count value H'AA is set in TCORA_0, and low-level output count value H'55 is set in TCORB_0. Pulses are output according to values in TCORA_0 and TCORB_0, which are controlled by TCR_0 and TCSR_0.
2. Any desired low-level output width (this determines the duty cycle) is obtained with the TCORB_0 setting.

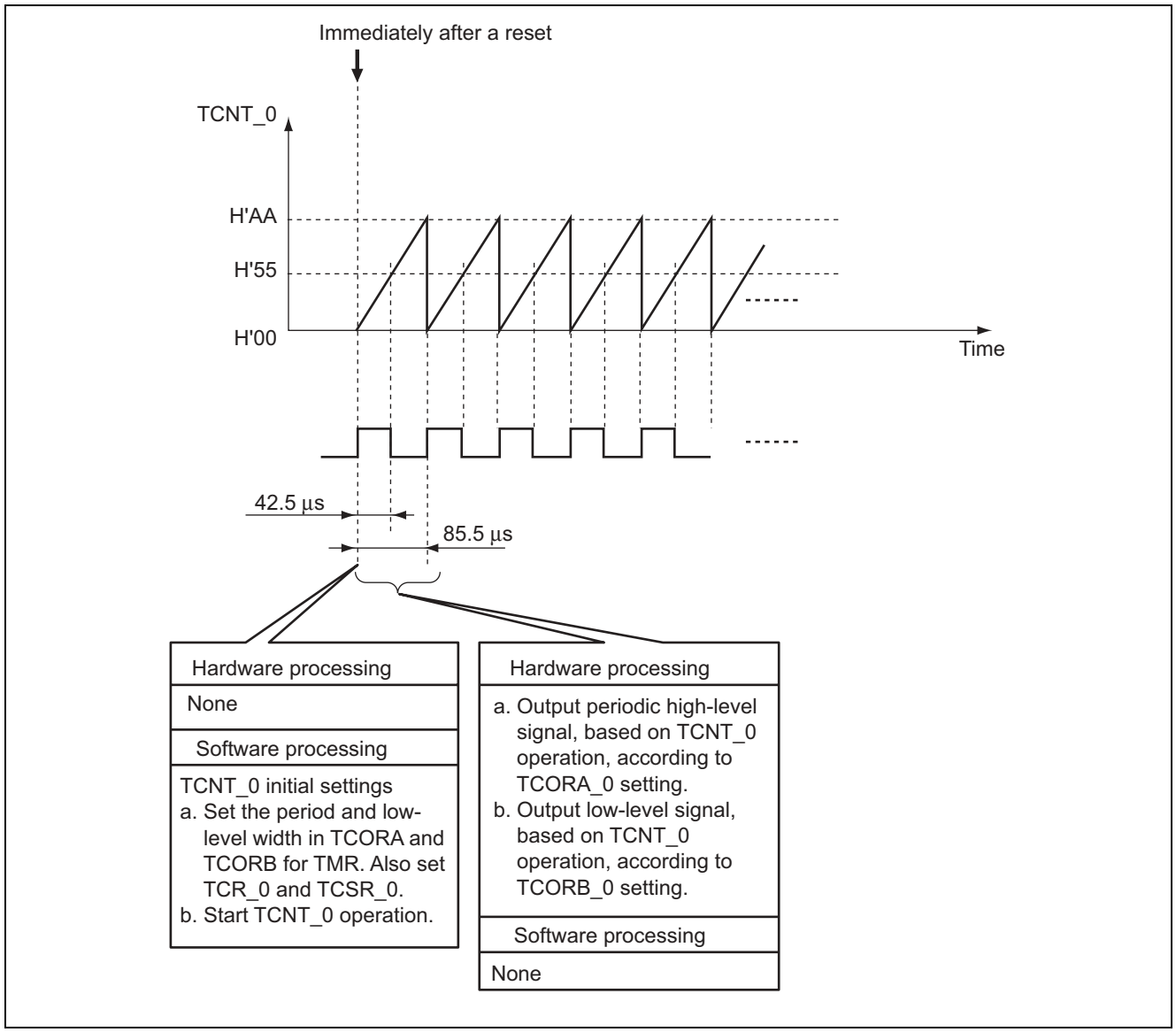


Figure 3 Output of Pulses with a Specified Duty Cycle Using 8-Bit Timer

4. Description of Software

4.1 Module

Table 2 describes the module used in this sample task.

Table 2 Description of Modules

Module	Label	Function
Main routine	main	Outputs pulses with a specified duty cycle based on counting by TCNT_0.

4.2 Arguments

This sample program does not use arguments.

4.3 Internal Registers

The internal registers used in this sample task are described in table 3.

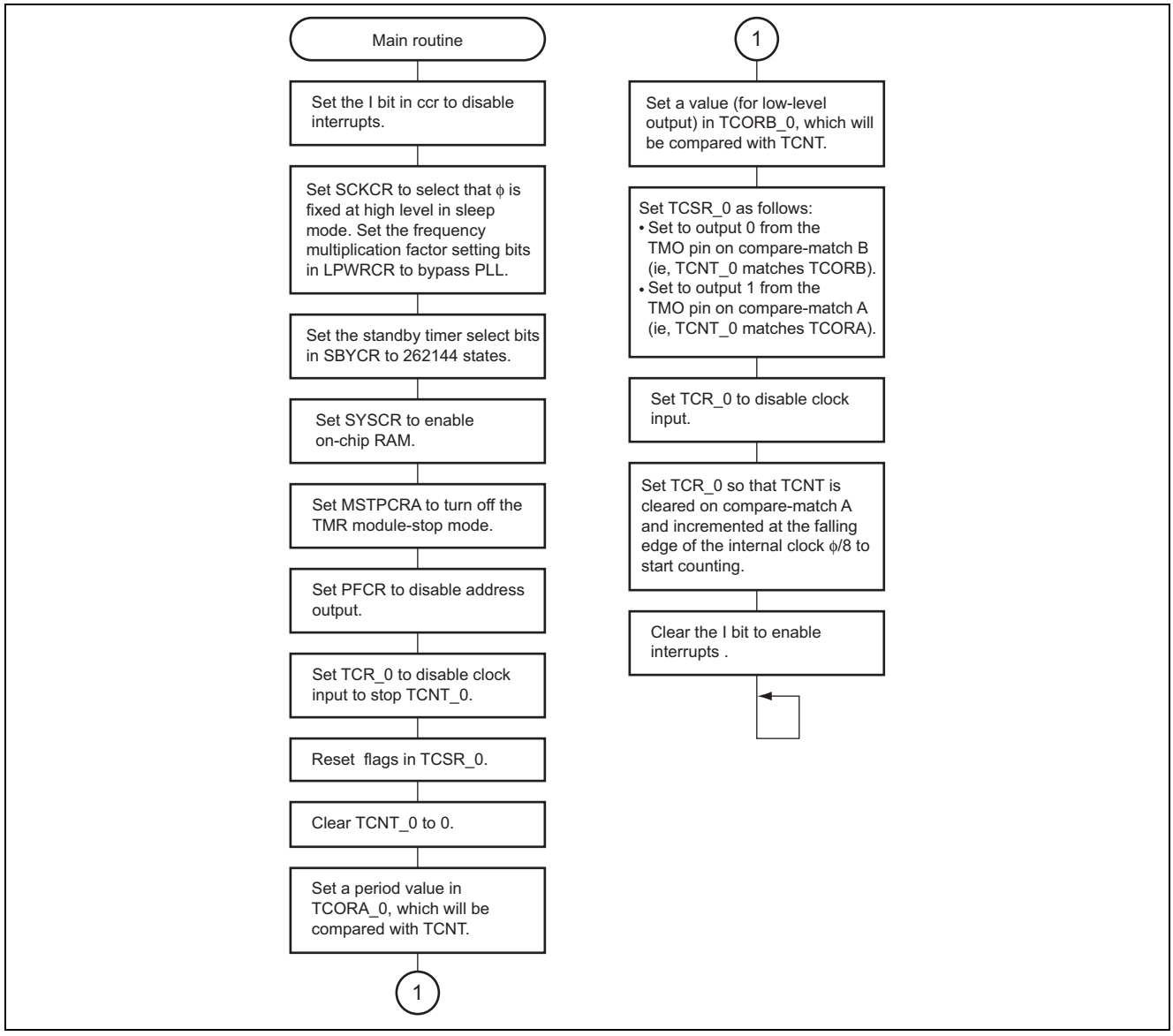
Table 3 Description of Internal Registers

Register		Function	Address	Setting
TCNT_0		Timer Counter 8-bit up counter that can be read or written to	H'FFFF70	H'00
TCORA_0		Time Constant Register A 8-bit register that can be read or written to	H'FFFF6C	H'AA
TCORB_0		Time Constant Register B 8-bit register that can be read or written to	H'FFFF6E	H'55
TCR_0	CMIEB	Timer Control Register (Compare-Match Interrupt Enable B) When CMIEB = 0, CMFB interrupt request (CMIB) is disabled. When CMIEB = 1 CMFB interrupt request (CMIB) is enabled.	H'FFFF68 Bit 7	0
	CMIEA	Timer Control Register (Compare-Match Interrupt Enable A) When CMIEA = 0, CMFA interrupt request (CMIA) is disabled. When CMIEA = 1, CMFA interrupt request (CMIA) is enabled.	H'FFFF68 Bit 6	0
	OVIE	Timer Control Register (Timer Overflow Interrupt Enable) When OVIE = 0, OVF interrupt request (OVI) is disabled. When OVIE = 1, OVF interrupt request (OVI) is enabled.	H'FFFF68 Bit 5	0
	CCLR1 CCLR0	Timer Control Register (Counter Clear 1, 0) When CCLR1 and CCLR0 = 01, TCNT_0 is cleared on compare-match A. When CCLR1 and CCLR0 = 10, TCNT_0 is cleared on compare-match B.	H'FFFF68 Bit 4 Bit 3	0, 1
	CKS2 CKS1 CKS0	Timer Control Register (Clock Select 2 to 0) When CKS2, CKS1 and CKS0 = 000, clock input is disabled. When CKS2, CKS1 and CKS0 = 001, TCNT_0 is incremented on the falling edge of the internal clock ϕ/8.	H'FFFF68 Bits 2 to 0	0, 0, 1

Register		Function	Address	Setting
TCSR_0	CMFB	Timer Control/Status Register (Compare-Match Flag B) CMFB = 0 indicates that TCNT does not match TCORB. CMFB = 1 indicates that TCNT matches TCORB.	H'FFFF6A Bit 7	0
	CMFA	Timer Control/Status Register (Compare-Match Flag A) CMFA = 0 indicates that TCNT does not match TCORA. CMFA= 1 indicates that TCNT matches TCORA.	H'FFFF6A Bit 6	0
	OVF	Timer Control/Status Register (Timer Overflow Flag) OVF = 0 indicates that a TCNT overflow has not occurred. OVF= 1 indicates that a TCNT overflow has occurred.	H'FFFF6A Bit 5	0
	ADTE	Timer Control/Status Register (A/D Trigger Enable) When ADTE = 0, A/D conversion start request generated on compare-match A is disabled. When ADTE = 1, A/D conversion start request generated on compare-match A is enabled.	H'FFFF6A Bit 4	0
	OS3 OS2	Timer Control/Status Register (Output Select 3, 2) When OS3 and OS2 = 00, no change. When OS3 and OS2 = 01, 0 is output on compare-match B	H'FFFF6A Bit 3 Bit 2	0, 1
	OS1 OS0	Timer Control/Status Register (Output Select 1, 0) When OS1 and OS0 = 10, 1 is output on compare-match A. When OS1 and OS0 = 11, the output is toggled on compare-match A.	H'FFFF6A Bit 1 Bit 0	1, 0

5. Flowchart

1 Main routine



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16, 2004	—	First edition issued

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