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April 1st, 2010
Renesas Electronics Corporation

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H8S Family

Using the HCAN (4): Standard Format, 8 Bytes of Data, with Priority

Introduction

The Controller Area Network (HCAN) module is used to control the Controller Area Network (CAN), which provides a means for real-time communications in automobiles and industrial equipment systems.

This application note presents an example of communications operation using the H8S/2636’s on-chip HCAN module and is offered to users for reference in the software and hardware design processes.

Although the operation of the sample application and programs provided in this application note has been confirmed, please verify operation in your environment before actually using them.

Target Device

H8S/2636

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1. Specifications

Between two H8S/2636 devices, eight bytes of data are transmitted in a standard format message from multiple mailboxes in order of message identifier priority. The messages are received solely by mailbox 0.

(1) Specifications common to the transmitter and receiver
- Channel 0 (HCAN0) is used
- Baud rate: 250 Kbps (in 20-MHz operation)

(2) Specifications of the transmitter
- Uses mailboxes 1 to 15
- Transmits messages in order of priority given to the message identifiers
- Data length is eight bytes for each mailbox, and message identifiers and data for transmission are as shown in table 1

Table 1 Setting Values for Mailboxes

<table>
<thead>
<tr>
<th>Mailbox No.</th>
<th>Identifier (11 Bits)</th>
<th>Data (8 Bytes)</th>
<th>Priority</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>H'666</td>
<td>H'1111 1111 1111 1111</td>
<td>12</td>
</tr>
<tr>
<td>2</td>
<td>H'2AA</td>
<td>H'2222 2222 2222 2222</td>
<td>5</td>
</tr>
<tr>
<td>3</td>
<td>H'777</td>
<td>H'3333 3333 3333 3333</td>
<td>14</td>
</tr>
<tr>
<td>4</td>
<td>H'333</td>
<td>H'4444 4444 4444 4444</td>
<td>6</td>
</tr>
<tr>
<td>5</td>
<td>H'088</td>
<td>H'5555 5555 5555 5555</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>H'4CC</td>
<td>H'6666 6666 6666 6666</td>
<td>9</td>
</tr>
<tr>
<td>7</td>
<td>H'199</td>
<td>H'7777 7777 7777 7777</td>
<td>3</td>
</tr>
<tr>
<td>8</td>
<td>H'7FF</td>
<td>H'8888 8888 8888 8888</td>
<td>15</td>
</tr>
<tr>
<td>9</td>
<td>H'111</td>
<td>H'9999 9999 9999 9999</td>
<td>2</td>
</tr>
<tr>
<td>10</td>
<td>H'444</td>
<td>H'AAAA AAAA AAAA AAAA</td>
<td>8</td>
</tr>
<tr>
<td>11</td>
<td>H'555</td>
<td>H'BBBB BBBB BBBB BBBB</td>
<td>10</td>
</tr>
<tr>
<td>12</td>
<td>H'6EE</td>
<td>H'CCCC CCCC CCCC CCCC</td>
<td>13</td>
</tr>
<tr>
<td>13</td>
<td>H'3BB</td>
<td>H'DDDD DDDD DDDD DDDD</td>
<td>7</td>
</tr>
<tr>
<td>14</td>
<td>H'222</td>
<td>H'EEEE EEEE EEEE EEEE</td>
<td>4</td>
</tr>
<tr>
<td>15</td>
<td>H'5DD</td>
<td>H'FFFF FFFF FFFF FFFF</td>
<td>11</td>
</tr>
</tbody>
</table>

- Transmits all messages in sequence at a time
- Polls the transmission-complete flag during transmission
- After confirming that the transmission-complete flag has been set, clears the flag as the final operation
Specifications of the receiver:

- Uses mailbox 0
- Does not set the message identifier mask and receives all messages
- Uses the receive message interrupt (IRRI)
  
  (a) The DTC is activated on a receive message interrupt and stores the received data in on-chip RAM.
  
  (b) The DTC is used in block-transfer mode and transfers 15 blocks, each consisting of eight bytes.
  
  (c) After the DTC transfer has ended, the receive message interrupt routine clears the reception-complete flag and disables the receive message interrupt, after which the operation is over.
### 2. Functional Descriptions of the Transmitter and Receiver

Tables 2 and 3 list the function assignments of the relevant pins and registers.

#### Table 2  Function Assignment for the HCAN Module

<table>
<thead>
<tr>
<th>Pin Usage</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin</td>
<td></td>
</tr>
<tr>
<td>HTxD0</td>
<td>Used for message transmission by the HCAN module (pin 97)</td>
</tr>
<tr>
<td>HRxD0</td>
<td>Used for message reception by the HCAN module (pin 98)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Relevant Registers</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Registers common to transmission and reception</td>
<td></td>
</tr>
<tr>
<td>MSTPCRC</td>
<td>Module stop control register C</td>
</tr>
<tr>
<td></td>
<td>Takes HCAN0 out of the module stop mode.</td>
</tr>
<tr>
<td>IRR</td>
<td>Interrupt register</td>
</tr>
<tr>
<td></td>
<td>Indicates the states of individual interrupt sources.</td>
</tr>
<tr>
<td>BCR</td>
<td>Bit configuration register</td>
</tr>
<tr>
<td></td>
<td>Configures the baud-rate prescaler for CAN and sets up the bit-timing parameters.</td>
</tr>
<tr>
<td>MBCR</td>
<td>Mailbox configuration register</td>
</tr>
<tr>
<td></td>
<td>Configures mailboxes for transmission or reception.</td>
</tr>
<tr>
<td>MCR</td>
<td>Master control register</td>
</tr>
<tr>
<td></td>
<td>Controls the CAN interface.</td>
</tr>
<tr>
<td>GSR</td>
<td>General status register</td>
</tr>
<tr>
<td></td>
<td>Indicates the CAN bus states.</td>
</tr>
<tr>
<td>MCx[n]</td>
<td>Message control registers (x = mailbox number)</td>
</tr>
<tr>
<td>n = 1</td>
<td>Sets the data length for data frames and remote frames.</td>
</tr>
<tr>
<td>n = 2 to 4</td>
<td>Reserved</td>
</tr>
<tr>
<td>n = 5</td>
<td>Holds standard ID bits (STD_ID2 to STD_ID0), extended ID bits (EXD_ID17 and EXD_ID16), RTR (indicates data frame or remote frame), and IDE (indicates standard format or extended format).</td>
</tr>
<tr>
<td>n = 6</td>
<td>Holds standard ID bits (STD_ID10 to STD_ID3)</td>
</tr>
<tr>
<td>n = 7</td>
<td>Holds extended ID bits (EXD_ID7 to EXD_ID0)</td>
</tr>
<tr>
<td>n = 8</td>
<td>Holds extended ID bits (EXD_ID15 to EXD_ID8)</td>
</tr>
<tr>
<td>MDx[n]</td>
<td>Message data registers (x = mailbox number)</td>
</tr>
<tr>
<td>n = 1 to 8</td>
<td>Hold CAN message data for transmission or received CAN message data.</td>
</tr>
</tbody>
</table>

| Transmission-related registers |          |
| TXPR                            | Transmit wait register |
|                                 | After a message for transmission has been stored in the mailbox, the corresponding bit in this register is set, indicating a transmission-wait state. |

| Reception-related registers     |          |
| RXPR                            | Receive complete register |
|                                 | Each bit in this register indicates that a message has been received normally in the corresponding mailbox. |

| LAFMH, LAFML                    | Local acceptance filter mask H, L |
|                                 | Identifier filter mask settings for the mailboxes configured for reception. |
### Relevant Registers

<table>
<thead>
<tr>
<th>Registers</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>MBIMR (Mailbox interrupt mask register)</td>
<td>Enables or disables interrupt requests for the individual mailboxes.</td>
</tr>
<tr>
<td>IMR (Interrupt mask register)</td>
<td>Enables or disables interrupt requests by the IRR interrupt flag.</td>
</tr>
<tr>
<td>IPRM (Interrupt priority register)</td>
<td>Sets the priority level for HCAN interrupts.</td>
</tr>
<tr>
<td>SYSCR (System control register)</td>
<td>Sets the interrupt control mode.</td>
</tr>
</tbody>
</table>

### Table 2 Function Assignment for the DTC

<table>
<thead>
<tr>
<th>DTC-Related Registers</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSTPCRA (Module stop control register A)</td>
<td>Takes the DTC out of module stop mode.</td>
</tr>
<tr>
<td>MRA, MRB (DTC mode register A, B)</td>
<td>Control the operating mode of the DTC.</td>
</tr>
<tr>
<td>SAR (DTC source address register)</td>
<td>Specified the address of the source data area for DTC transfer.</td>
</tr>
<tr>
<td>DAR (DTC destination address register)</td>
<td>Specifies the address of the destination data area for DTC transfer.</td>
</tr>
<tr>
<td>CRA (DTC transfer count register A)</td>
<td>Specifies the number of data transfers by the DTC.</td>
</tr>
<tr>
<td>CRB (DTC transfer count register B)</td>
<td>In block transfer mode, specifies the block length.</td>
</tr>
<tr>
<td>DTCERA to DTCERG (DTC enable register)</td>
<td>Selects the interrupt source that activates the DTC.</td>
</tr>
<tr>
<td>DTVECR (DTC vector register)</td>
<td>Enables or disables activation of the DTC by software and sets the vector number for the software activation interrupt.</td>
</tr>
</tbody>
</table>
3. Flowchart for the Transmitter

Main routine for transmission

Take the HCAN out of module stop mode.

Clear the IRR0 bit.

Set the bit rate.

Set the mailbox for transmission.

Initialize the mailbox (RAM).

Set the priority for transmission.
Take the HCAN out of configuration mode.

For mailboxes 1 to 15, set the mode of transmission and data to be transmitted.

Place mailboxes 1 to 15 in the transmission-wait state.

Transmission from mailboxes 1 to 15 complete?

No

Yes

Clear the transmission-complete flags for mailboxes 1 to 15.

End of transmission

Figure 1 Flowchart for the Transmitter
4. Description of Software (Transmitter)

4.1 Module

Table 3 Description of Module

<table>
<thead>
<tr>
<th>Module</th>
<th>Label</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Routine</td>
<td>t_main</td>
<td>Initialize the HCAN and makes settings for transmission.</td>
</tr>
</tbody>
</table>

4.2 Registers

Table 4 Description of Registers*

<table>
<thead>
<tr>
<th>Register</th>
<th>Function</th>
<th>Setting</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSTP.CRC.BYTE</td>
<td>Takes HCAN0 out of module stop mode.</td>
<td>H'F7</td>
<td>Main routine</td>
</tr>
<tr>
<td>HCAN0.IRR.WORD</td>
<td>The reset interrupt flag in this register is cleared. (Clearing condition: writing a 1 to the bit)</td>
<td>H'0100</td>
<td></td>
</tr>
<tr>
<td>HCAN0.BCR.WORD</td>
<td>Sets the bit rate to 250 Kbps when $\phi = 20$ MHz</td>
<td>H'0334</td>
<td></td>
</tr>
<tr>
<td>HCAN0.MBCR.WORD</td>
<td>Sets mailboxes 1 to 15 for transmission.</td>
<td>H'0100</td>
<td></td>
</tr>
<tr>
<td>HCAN0.MCR.BYTE</td>
<td>Selects transmission in order of message identifier priority and takes the HCAN module out of configuration mode.</td>
<td>H'00</td>
<td></td>
</tr>
<tr>
<td>HCAN0.GSR.BYTE</td>
<td>Checked to confirm that HCAN0 is out of configuration mode.</td>
<td>—</td>
<td></td>
</tr>
<tr>
<td>HCAN0.MC[x][4]</td>
<td>For mailbox x, sets the frame type to data frame and the frame format to standard format. Also holds the message identifier bits, STD_ID2 to STD_ID0.</td>
<td>See table 1</td>
<td></td>
</tr>
<tr>
<td>HCAN0.MC[x][5]</td>
<td>Holds the message identifier bits, STD_ID10 to STD_ID3</td>
<td>See table 1</td>
<td></td>
</tr>
<tr>
<td>HCAN0.MC[x][0]</td>
<td>Sets the data length for transmission from mailbox x to eight bytes.</td>
<td>H'08</td>
<td></td>
</tr>
<tr>
<td>HCAN0.MD[x][y]</td>
<td>Holds data for transmission from mailboxes x.</td>
<td>See table 1</td>
<td></td>
</tr>
<tr>
<td>HCAN0.TXPR.WORD</td>
<td>Places mailboxes 1 to 15 in the transmission-wait state.</td>
<td>H'FEFF</td>
<td></td>
</tr>
<tr>
<td>HCAN0.TXACK.WORD</td>
<td>Checked to see if the transmission-complete flags for mailboxes 1 to 15 are set; when set, the flags are cleared. (Clearing condition: writing a 1 to the bit)</td>
<td>H'FEFF</td>
<td></td>
</tr>
</tbody>
</table>

Note: * The register names shown above are defined in a header file which is available for downloading from the following web page.
http://download.renesas.com/eng/mpumcu/sample_codes/h8sx_h8s_h8_family/io_register/index.html

x = 1 to 15, y = 0 to 7
5. Program Listing (Transmission)

/**************************************************
/* HCAN Transmission Program (No.4) */
/**************************************************
#include <stdio.h> /* Header file for library functions */
#include <machine.h> /* Header file for library functions */
#include "2636S.h" /* Header file of peripheral register definitions */
void t_main(void){
  unsigned char i,j;
  /* Initialization */
  MSTP.CRC.BYTE = 0xF7; /* Cancel module stop mode of HCAN */
  HCAN0.IRR.WORD = 0x0100; /* Initialize reset flag for HCAN module */
  HCAN0.BCR.WORD = 0x0334; /* Bit rate: 250 kbps */
  HCAN0.MBCR.WORD = 0x0100; /* Set mailboxes 1 to 15 for transmission */
  for(i=0; i<=15; i++){
    for(j=0; j<=7; j++){
      HCAN0.MC[i][j] = 0x00;
    }
  }
  for(i=0; i<=15; i++){
    for(j=0; j<=7; j++){
      HCAN0.MD[i][j] = 0x00;
    }
  }
  HCAN0.MCR.BYTE = 0x00; /* Transmission in message identifier priority order */
  while(HCAN0.GSR.BYTE & 0x08); /* Configuration mode cancellation check */
  /* Transmit data setting */
  /***************************************************************************/
  /* Mail Box 1 */
  /***************************************************************************/
  HCAN0.MC[1][4] = 0xC0; /* Standard format, data frame, and identifier setting */
  HCAN0.MC[1][5] = 0xCC; /* Identifier setting (STD: 0x666) */
  HCAN0.MC[1][0] = 0x08; /* Data length: 8 bytes */
  HCAN0.MD[1][0] = 0x11; /* Message data: 00010001 */
  HCAN0.MD[1][1] = 0x11; /* Message data: 00010001 */
  HCAN0.MD[1][2] = 0x11; /* Message data: 00010001 */
  HCAN0.MD[1][3] = 0x11; /* Message data: 00010001 */
  HCAN0.MD[1][4] = 0x11; /* Message data: 00010001 */
  HCAN0.MD[1][5] = 0x11; /* Message data: 00010001 */
  HCAN0.MD[1][6] = 0x11; /* Message data: 00010001 */
  HCAN0.MD[1][7] = 0x11; /* Message data: 00010001 */
  /***************************************************************************/
  /* Mail Box 2 */
  /***************************************************************************/
  HCAN0.MC[2][4] = 0x40; /* Standard format, data frame, and identifier setting */
  HCAN0.MC[2][5] = 0x55; /* Identifier setting (STD: 0x2AA) */
  HCAN0.MC[2][0] = 0x08; /* Data length: 8 bytes */
  HCAN0.MD[2][0] = 0x22; /* Message data: 00010001 */
  HCAN0.MD[2][1] = 0x22; /* Message data: 00010001 */
  HCAN0.MD[2][2] = 0x22; /* Message data: 00010001 */
  HCAN0.MD[2][3] = 0x22; /* Message data: 00010001 */
  HCAN0.MD[2][4] = 0x22; /* Message data: 00010001 */
  HCAN0.MD[2][5] = 0x22; /* Message data: 00010001 */
  HCAN0.MD[2][6] = 0x22; /* Message data: 00010001 */
  HCAN0.MD[2][7] = 0x22; /* Message data: 00010001 */
/******* Mail Box 3 *******
HCAN0.MC[3][4] = 0xE0; /* Standard format, data frame, and identifier setting */
HCAN0.MC[3][5] = 0xEE; /* Identifier setting (STD: 0x777) */
HCAN0.MC[3][0] = 0x08; /* Data length: 8 bytes */
HCAN0.MD[3][0] = 0x33; /* Message data: 00110011 */
HCAN0.MD[3][1] = 0x33; /* Message data: 00110011 */
HCAN0.MD[3][2] = 0x33; /* Message data: 00110011 */
HCAN0.MD[3][3] = 0x33; /* Message data: 00110011 */
HCAN0.MD[3][4] = 0x33; /* Message data: 00110011 */
HCAN0.MD[3][5] = 0x33; /* Message data: 00110011 */
HCAN0.MD[3][6] = 0x33; /* Message data: 00110011 */
HCAN0.MD[3][7] = 0x33; /* Message data: 00110011 */

******* Mail Box 4 *******
HCAN0.MC[4][4] = 0x60; /* Standard format, data frame, and identifier setting */
HCAN0.MC[4][5] = 0x66; /* Identifier setting (STD: 0x333) */
HCAN0.MC[4][0] = 0x08; /* Data length: 8 bytes */
HCAN0.MD[4][0] = 0x44; /* Message data: 01000100 */
HCAN0.MD[4][1] = 0x44; /* Message data: 01000100 */
HCAN0.MD[4][2] = 0x44; /* Message data: 01000100 */
HCAN0.MD[4][3] = 0x44; /* Message data: 01000100 */
HCAN0.MD[4][4] = 0x44; /* Message data: 01000100 */
HCAN0.MD[4][5] = 0x44; /* Message data: 01000100 */
HCAN0.MD[4][6] = 0x44; /* Message data: 01000100 */
HCAN0.MD[4][7] = 0x44; /* Message data: 01000100 */

******* Mail Box 5 *******
HCAN0.MC[5][4] = 0x00; /* Standard format, data frame, and identifier setting */
HCAN0.MC[5][5] = 0x11; /* Identifier setting (STD: 0x088) */
HCAN0.MC[5][0] = 0x08; /* Data length: 8 bytes */
HCAN0.MD[5][0] = 0x55; /* Message data: 01010101 */
HCAN0.MD[5][1] = 0x55; /* Message data: 01010101 */
HCAN0.MD[5][2] = 0x55; /* Message data: 01010101 */
HCAN0.MD[5][3] = 0x55; /* Message data: 01010101 */
HCAN0.MD[5][4] = 0x55; /* Message data: 01010101 */
HCAN0.MD[5][5] = 0x55; /* Message data: 01010101 */
HCAN0.MD[5][6] = 0x55; /* Message data: 01010101 */
HCAN0.MD[5][7] = 0x55; /* Message data: 01010101 */

******* Mail Box 6 *******
HCAN0.MC[6][4] = 0x80; /* Standard format, data frame, and identifier setting */
HCAN0.MC[6][5] = 0x99; /* Identifier setting (STD: 0x4CC) */
HCAN0.MC[6][0] = 0x08; /* Data length: 8 bytes */
HCAN0.MD[6][0] = 0x66; /* Message data: 01100110 */
HCAN0.MD[6][1] = 0x66; /* Message data: 01100110 */
HCAN0.MD[6][2] = 0x66; /* Message data: 01100110 */
HCAN0.MD[6][3] = 0x66; /* Message data: 01100110 */
HCAN0.MD[6][4] = 0x66; /* Message data: 01100110 */
HCAN0.MD[6][5] = 0x66; /* Message data: 01100110 */
HCAN0.MD[6][6] = 0x66; /* Message data: 01100110 */
HCAN0.MD[6][7] = 0x66; /* Message data: 01100110 */
### Mail Box 7

<table>
<thead>
<tr>
<th>HCAN0.MC[7][4]</th>
<th>0x20; /* Standard format, data frame, and identifier setting */</th>
</tr>
</thead>
<tbody>
<tr>
<td>HCAN0.MC[7][5]</td>
<td>0x33; /* Identifier setting (STD: 0x199) */</td>
</tr>
<tr>
<td>HCAN0.MC[7][0]</td>
<td>0x08; /* Data length: 8 bytes */</td>
</tr>
<tr>
<td>HCAN0.MD[7][0]</td>
<td>0x77; /* Message data: 01110111 */</td>
</tr>
<tr>
<td>HCAN0.MD[7][1]</td>
<td>0x77; /* Message data: 01110111 */</td>
</tr>
<tr>
<td>HCAN0.MD[7][2]</td>
<td>0x77; /* Message data: 01110111 */</td>
</tr>
<tr>
<td>HCAN0.MD[7][3]</td>
<td>0x77; /* Message data: 01110111 */</td>
</tr>
</tbody>
</table>

### Mail Box 8

<table>
<thead>
<tr>
<th>HCAN0.MC[8][4]</th>
<th>0xE0; /* Standard format, data frame, and identifier setting */</th>
</tr>
</thead>
<tbody>
<tr>
<td>HCAN0.MC[8][5]</td>
<td>0xFF; /* Identifier setting (STD: 0x7FF) */</td>
</tr>
<tr>
<td>HCAN0.MC[8][0]</td>
<td>0x08; /* Data length: 8 bytes */</td>
</tr>
<tr>
<td>HCAN0.MD[8][0]</td>
<td>0x88; /* Message data: 10001000 */</td>
</tr>
<tr>
<td>HCAN0.MD[8][1]</td>
<td>0x88; /* Message data: 10001000 */</td>
</tr>
<tr>
<td>HCAN0.MD[8][2]</td>
<td>0x88; /* Message data: 10001000 */</td>
</tr>
<tr>
<td>HCAN0.MD[8][3]</td>
<td>0x88; /* Message data: 10001000 */</td>
</tr>
</tbody>
</table>

### Mail Box 9

<table>
<thead>
<tr>
<th>HCAN0.MC[9][4]</th>
<th>0x20; /* Standard format, data frame, and identifier setting */</th>
</tr>
</thead>
<tbody>
<tr>
<td>HCAN0.MC[9][5]</td>
<td>0x22; /* Identifier setting (STD: 0x111) */</td>
</tr>
<tr>
<td>HCAN0.MC[9][0]</td>
<td>0x08; /* Data length: 8 bytes */</td>
</tr>
<tr>
<td>HCAN0.MD[9][0]</td>
<td>0x99; /* Message data: 10011001 */</td>
</tr>
<tr>
<td>HCAN0.MD[9][1]</td>
<td>0x99; /* Message data: 10011001 */</td>
</tr>
<tr>
<td>HCAN0.MD[9][2]</td>
<td>0x99; /* Message data: 10011001 */</td>
</tr>
<tr>
<td>HCAN0.MD[9][3]</td>
<td>0x99; /* Message data: 10011001 */</td>
</tr>
</tbody>
</table>

### Mail Box 10

<table>
<thead>
<tr>
<th>HCAN0.MC[10][4]</th>
<th>0x80; /* Standard format, data frame, and identifier setting */</th>
</tr>
</thead>
<tbody>
<tr>
<td>HCAN0.MC[10][5]</td>
<td>0x88; /* Identifier setting (STD: 0x444) */</td>
</tr>
<tr>
<td>HCAN0.MC[10][0]</td>
<td>0x08; /* Data length: 8 bytes */</td>
</tr>
<tr>
<td>HCAN0.MD[10][0]</td>
<td>0xAA; /* Message data: 10101010 */</td>
</tr>
<tr>
<td>HCAN0.MD[10][1]</td>
<td>0xAA; /* Message data: 10101010 */</td>
</tr>
<tr>
<td>HCAN0.MD[10][2]</td>
<td>0xAA; /* Message data: 10101010 */</td>
</tr>
<tr>
<td>HCAN0.MD[10][3]</td>
<td>0xAA; /* Message data: 10101010 */</td>
</tr>
<tr>
<td>HCAN0.MD[10][4]</td>
<td>0xAA; /* Message data: 10101010 */</td>
</tr>
<tr>
<td>HCAN0.MD[10][5]</td>
<td>0xAA; /* Message data: 10101010 */</td>
</tr>
<tr>
<td>HCAN0.MD[10][6]</td>
<td>0xAA; /* Message data: 10101010 */</td>
</tr>
<tr>
<td>HCAN0.MD[10][7]</td>
<td>0xAA; /* Message data: 10101010 */</td>
</tr>
</tbody>
</table>
HCAN0.MC[11][4] = 0xA0; /* Standard format, data frame, and identifier setting */
HCAN0.MC[11][5] = 0xAA; /* Identifier setting (STD: 0x555) */
HCAN0.MC[11][0] = 0x08; /* Data length: 8 bytes */
HCAN0.MD[11][0] = 0xBB; /* Message data: 10111011 */
HCAN0.MD[11][1] = 0xBB; /* Message data: 10111011 */
HCAN0.MD[11][2] = 0xBB; /* Message data: 10111011 */
HCAN0.MD[11][3] = 0xBB; /* Message data: 10111011 */
HCAN0.MD[11][4] = 0xBB; /* Message data: 10111011 */
HCAN0.MD[11][5] = 0xBB; /* Message data: 10111011 */
HCAN0.MD[11][6] = 0xBB; /* Message data: 10111011 */
HCAN0.MD[11][7] = 0xBB; /* Message data: 10111011 */

HCAN0.MC[12][4] = 0xC0; /* Standard format, data frame, and identifier setting */
HCAN0.MC[12][5] = 0xDD; /* Identifier setting (STD: 0x6EE) */
HCAN0.MC[12][0] = 0x08; /* Data length: 8 bytes */
HCAN0.MD[12][0] = 0xCC; /* Message data: 11001100 */
HCAN0.MD[12][1] = 0xCC; /* Message data: 11001100 */
HCAN0.MD[12][2] = 0xCC; /* Message data: 11001100 */
HCAN0.MD[12][3] = 0xCC; /* Message data: 11001100 */
HCAN0.MD[12][4] = 0xCC; /* Message data: 11001100 */
HCAN0.MD[12][5] = 0xCC; /* Message data: 11001100 */
HCAN0.MD[12][6] = 0xCC; /* Message data: 11001100 */
HCAN0.MD[12][7] = 0xCC; /* Message data: 11001100 */

HCAN0.MC[13][4] = 0x60; /* Standard format, data frame, and identifier setting */
HCAN0.MC[13][5] = 0x77; /* Identifier setting (STD: 0x3BB) */
HCAN0.MC[13][0] = 0x08; /* Data length: 8 bytes */
HCAN0.MD[13][0] = 0xDD; /* Message data: 11011101 */
HCAN0.MD[13][1] = 0xDD; /* Message data: 11011101 */
HCAN0.MD[13][2] = 0xDD; /* Message data: 11011101 */
HCAN0.MD[13][3] = 0xDD; /* Message data: 11011101 */
HCAN0.MD[13][4] = 0xDD; /* Message data: 11011101 */
HCAN0.MD[13][5] = 0xDD; /* Message data: 11011101 */
HCAN0.MD[13][6] = 0xDD; /* Message data: 11011101 */
HCAN0.MD[13][7] = 0xDD; /* Message data: 11011101 */

HCAN0.MC[14][4] = 0x40; /* Standard format, data frame, and identifier setting */
HCAN0.MC[14][5] = 0x44; /* Identifier setting (STD: 0x222) */
HCAN0.MC[14][0] = 0x08; /* Data length: 8 bytes */
HCAN0.MD[14][0] = 0xEE; /* Message data: 11101110 */
HCAN0.MD[14][1] = 0xEE; /* Message data: 11101110 */
HCAN0.MD[14][2] = 0xEE; /* Message data: 11101110 */
HCAN0.MD[14][3] = 0xEE; /* Message data: 11101110 */
HCAN0.MD[14][4] = 0xEE; /* Message data: 11101110 */
HCAN0.MD[14][5] = 0xEE; /* Message data: 11101110 */
HCAN0.MD[14][6] = 0xEE; /* Message data: 11101110 */
HCAN0.MD[14][7] = 0xEE; /* Message data: 11101110 */
/******* Mail Box 15 *******
HCAN0.MC[15][4] = 0xA0; /* Standard format, data frame, and identifier setting */
HCAN0.MC[15][5] = 0xBB; /* Identifier setting (STD: 0x5DD) */
HCAN0.MC[15][0] = 0x08; /* Data length: 8 bytes */
HCAN0.MD[15][0] = 0xFF; /* Message data: 11111111 */
HCAN0.MD[15][1] = 0xFF; /* Message data: 11111111 */
HCAN0.MD[15][2] = 0xFF; /* Message data: 11111111 */
HCAN0.MD[15][3] = 0xFF; /* Message data: 11111111 */
HCAN0.MD[15][4] = 0xFF; /* Message data: 11111111 */
HCAN0.MD[15][5] = 0xFF; /* Message data: 11111111 */
HCAN0.MD[15][6] = 0xFF; /* Message data: 11111111 */
HCAN0.MD[15][7] = 0xFF; /* Message data: 11111111 */

/* Message transmission */
HCAN0.TXPR.WORD = 0xFEFF; /* Place mailboxes 1 to 15 in transmission wait state */
while((HCAN0.TXACK.WORD & 0xFEFF) != 0xFEFF); /* Wait until transmission is complete */

/* Transmission-complete flag clearing */
HCAN0.TXACK.WORD &= 0xFEFF; /* Clear transmission-complete flag */
while(1);
6. Flowchart for the Receiver

**Main routine for reception**
- Take HCAN out of module stop mode.
- Clear the IRR0 bit.
- Set the bit rate.
- Set the mailbox for reception.
- Initialize the mailbox (RAM).
- Take the HCAN out of configuration mode.
- Enable mailbox 0 interrupts.
- Enable message reception interrupts and bus operation interrupts.
- Set the interrupt control mode.
- Set the priority level of HCAN0 interrupts.
- Set the interrupt mask level
- Set the mode of reception.
- Set the identifier filter mask.
- Place the HCAN in sleep mode.

**DTC setting**
- Take the DTC out of module stop mode.
- Set the source address for the DTC.
- Set the DTC operating mode.
- Set the destination address for the DTC.
- Select disabling of interrupts if the transfer counter is non-zero after the end of DTC data transfer.
- Set the block unit for transfer by the DTC to 8 bytes.
- Set the number of DTC block transfers to 15.
- Enable DTC activation by HCAN0 interrupts.
- RTS

*Figure 2 Flowchart for the Receiver*
Figure 3 Flowchart of Interrupt Routines for the Receiver
7. Description of Software (Receiver)

7.1 Modules

Table 5  Description of Modules

<table>
<thead>
<tr>
<th>Module</th>
<th>Label</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Routine</td>
<td>r_main</td>
<td>Initializes the HCAN and makes settings for reception.</td>
</tr>
<tr>
<td>Bus operation</td>
<td>OVR0_IRR12</td>
<td>Clears the bus operation interrupt flag.</td>
</tr>
<tr>
<td>interrupt routine</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DTC transfer-end</td>
<td>DTCend_RM0</td>
<td>Clears the reception flag and places the HCAN in sleep mode.</td>
</tr>
<tr>
<td>interrupt routine</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

7.2 Registers

Table 6  Description of Registers*

<table>
<thead>
<tr>
<th>Register</th>
<th>Function</th>
<th>Setting</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>MAILBOX.MDATA[1][8]</td>
<td>Storage for the received data Address range: H'FFE000 to H'FFE007</td>
<td>—</td>
<td>Main routine</td>
</tr>
<tr>
<td>MSTP.CRA.BYTE</td>
<td>Takes the DTC out of module stop mode.</td>
<td>H'3F</td>
<td></td>
</tr>
<tr>
<td>DTC_SAR</td>
<td>Sets the first address of the message data area for mailbox 0 as the source address for transfer.</td>
<td>H'FFF8B0</td>
<td></td>
</tr>
<tr>
<td>DTC_MRA</td>
<td>Sets the incrementation of both DTC_SAR and DTC_DAR after each transfer, and selects block transfer mode and byte-sized transfer.</td>
<td>H'AA</td>
<td></td>
</tr>
<tr>
<td>DTC_DAR</td>
<td>Sets the first address of the received-data storage area as the destination address for transfer.</td>
<td>H'FFE000</td>
<td></td>
</tr>
<tr>
<td>DTC_MRB</td>
<td>Disables interrupts to the CPU if the transfer counter value is non-zero after the end of DTC transfer.</td>
<td>H'00</td>
<td></td>
</tr>
<tr>
<td>DTC_CRA</td>
<td>Sets the size of a block (8 bytes).</td>
<td>H'0808</td>
<td></td>
</tr>
<tr>
<td>DTC_CRB</td>
<td>Sets the number of block transfers (15 times).</td>
<td>H'000F</td>
<td></td>
</tr>
<tr>
<td>DTC.DTCEG.BYTE</td>
<td>Selects the DTC activation source (RM0).</td>
<td>H'04</td>
<td></td>
</tr>
<tr>
<td>MSTP.CRC.BYTE</td>
<td>Takes HCAN0 out of module stop mode.</td>
<td>H'F7</td>
<td></td>
</tr>
<tr>
<td>HCAN0.IRR.WORD</td>
<td>The reset interrupt flag in this register is cleared. (Clearing condition: writing a 1 to the bit)</td>
<td>H'0100</td>
<td></td>
</tr>
<tr>
<td>HCAN0.BCR.WORD</td>
<td>Sets the bit rate to 250 Kbps when ( \phi = 20 ) MHz</td>
<td>H'0334</td>
<td></td>
</tr>
<tr>
<td>HCAN0.MBCR.WORD</td>
<td>Sets mailbox 0 for reception.</td>
<td>H'0100</td>
<td></td>
</tr>
</tbody>
</table>
### Register Function Setting Used in

**HCAN0.MCR.BYTE**
- Takes HCAN0 out of configuration mode and places it in sleep mode.
- **Setting**: H’FE and H’A0
- **Used in**: Main routine

**HCAN0.GSR.BYTE**
- Checked to confirm that HCAN0 is out of configuration mode.
- **Setting**: —

**HCAN0.MBIMR.WORD**
- Enables interrupt requests of mailbox 0.
- **Setting**: H’FEFF

**HCAN0.IMR.WORD**
- Enables message reception and bus operation interrupts.
- **Setting**: H’FCEF

**SYSCR.BYTE**
- Sets the interrupt control mode.
- **Setting**: H’20

**INTC.IPRM.BYTE**
- Sets the priority level of HCAN interrupts.
- **Setting**: H’07

**HCAN0.MC[0][4]**
- For mailbox 0, sets the frame type to data frame and the frame format to standard format.
- Also holds the message identifier bits, STD_ID2 to STD_ID0 (for message ID = H’555).
- **Setting**: H’A0

**HCAN0.MC[0][5]**
- Holds the message identifier bits, STD_ID10 to STD_ID3 (for message ID = H’555).
- **Setting**: H’AA

**HCAN0.LAFMH.WORD**
- Sets no identifier filter masking.
- **Setting**: H’FFFF

**HCAN0.IRR.WORD**
- The bus-operation interrupt flag in this register is cleared.
- **Setting**: H’0010
- **Used in**: Bus-operation interrupt routine

**HCAN0.RXPR.WORD**
- The reception-complete flag for mailbox 0 in this register is cleared.
- (Clearing condition: writing a 1 to the bit)
- **Setting**: H’FFFF
- **Used in**: DTC transfer-end interrupt routine

---

**Note:** The register names shown above are defined in a header file which is available for downloading from the following web page.

http://download.renesas.com/eng/mpumcu/sample_codes/h8sx_h8s_h8_family/io_register/index.html
8. Program Listing (Reception)

```c
#include <stdio.h>                         /* Header file for library functions                */
#include <machine.h>                       /* Header file for library functions                */
#include "2636S.h"                         /* Header file of peripheral register definitions   */

/* Definitions of Constants                                                                   */

volatile struct MB{                        /* struct MAILBOX0-15                               */
    unsigned char MDATA[15][8];            /* Storage of received data                         */
};
#define MAILBOX     (volatile struct MB        *)0xFFE000) /* First address of */
/* received data storage */
#define DTC_SAR     (*(volatile unsigned long  *)0xFFEBC0) /* DTC register info setting        */
#define DTC_MRA     (*(volatile unsigned char  *)0xFFEBC0) /* DTC register info setting        */
#define DTC_DAR     (*(volatile unsigned long  *)0xFFEBC4) /* DTC register info setting        */
#define DTC_MRB     (*(volatile unsigned char  *)0xFFEBC4) /* DTC register info setting        */
#define DTC_CRA     (*(volatile unsigned short *)0xFFEBC8) /* DTC register info setting        */
#define DTC_CRB     (*(volatile unsigned short *)0xFFEBCA) /* DTC register info setting        */

void r_main(void)
{
    unsigned char i,j;

    /* DTC initialization */
    MSTP.CRA.BYTE = 0x3F;                  /* Cancel module stop mode of DTC                   */
    DTC_SAR = (long)(&HCAN0.MD[0][0]);     /* Set transfer source address                      */
    DTC_MRA = 0xAA;                        /* SAR and DAR incremented after transfer;          */
    DTC_DAR = (long)(&MAILBOX.MDATA[0][0]);/* Set transfer destination address (on-chip RAM)   */
    DTC_MRB = 0x00;                        /* Disable interrupt after end of DTC transfer      */
    DTC_CRA = 0x0808;                      /* Block transfer size: 8 bytes                     */
    DTC_CRB = 0x000F;                      /* Number of block transfers: 15                    */
    DTC.DTCEG.BYTE |= 0x04;                /* Enable activation of DTC by HCAN0 interrupt (RM0)*/

    /* HCAN initialization */
    MSTP.CRC.BYTE = 0xF7;                  /* Cancel module stop mode of HCAN                  */
    HCAN0.IRR.WORD = 0x0100;               /* Initialize reset flag for HCAN module            */
    HCAN0.BCR.WORD = 0x0334;               /* Bit rate: 250 kbps                               */
    HCAN0.MBCR.WORD = 0x0100;              /* Set mailbox 0 for reception                      */
    for(i=0; i<=15; i++){
        for(j=0; j<=7; j++){
            HCAN0.MC[i][j] = 0x00;
        }
    }
    for(i=0; i<=15; i++){
        for(j=0; j<=7; j++){
            HCAN0.MD[i][j] = 0x00;
        }
    }
    HCAN0.MCR.BYTE &= 0xFE;                /* Cancel configuration mode                        */
    while(HCAN0.GSR.BYTE & 0x08);          /* Configuration mode cancellation check            */
}
```
H8S Family
Using the HCAN (4): Standard Format, 8 Bytes of Data, with Priority

/* Interrupt settings */
HCAN0.MB1MR.WORD = 0xFEFF; /* Enable mailbox 0 interrupt requests */
HCAN0.IMR.WORD = 0xFCEF; /* Enable message reception and */
/* bus operation interrupts */
SYSCR.BYTE |= 0x20; /* Set interrupt control mode 2 */
INTC.IPRM.BYTE = 0x07; /* Set the priority level of HCAN0 interrupts to 7 */
set_imask_exr(0); /* Set interrupt request mask level */

/* Reception data settings */
HCAN0.MC[0][4] = 0xA0; /* Standard format, data frame, and */
/* identifier setting */
HCAN0.MC[0][5] = 0xAA; /* Identifier setting */
HCAN0.LAFMH.WORD = 0xFFFF; /* Mailbox 0 receives data for any identifiers */

/* HCAN sleep mode setting */
HCAN0.MCR.BYTE |= 0xA0; /* Put HCAN in sleep mode; enable recovery by */
/* bus operation interrupt */

while(1);

/*******************************************************
/* Bus-Operation Interrupt Routine */
/*******************************************************
#pragma interrupt(OVR0_IRR12)
void OVR0_IRR12(void){
  HCAN0.IRR.WORD &= 0x0010; /* Clear IRR12 (bus-operation interrupt flag) */
}

/*******************************************************
/* DTC Transfer-End Interrupt Routine */
/*******************************************************
#pragma interrupt(DTCend_RM0)
void DTCend_RM0(void){
  HCAN0.RXPR.WORD &= 0xFFFF; /* Clear IRR1 (reception message interrupt flag) */
  HCAN0.MCR.BYTE |= 0xA0; /* Put HCAN in sleep mode */
}
9. Waveforms during Operation (Transmission and Reception)

Figure 4 show the first and last waveforms seen when this application is executed.
## Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Jul.22.05</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>
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