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Renesas Electronics Corporation

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## H8S Family

### Using the 8-Bit PWM Function to Generate Duty Cycle-Controlled Pulse Output

#### Introduction

The 8-bit PWM function is used to output 50% duty cycle pulses from PWM output pin PW0 with the pulse period of 6.51  $\mu$ s and high pulse width of 3.26  $\mu$ s.

#### Target Device

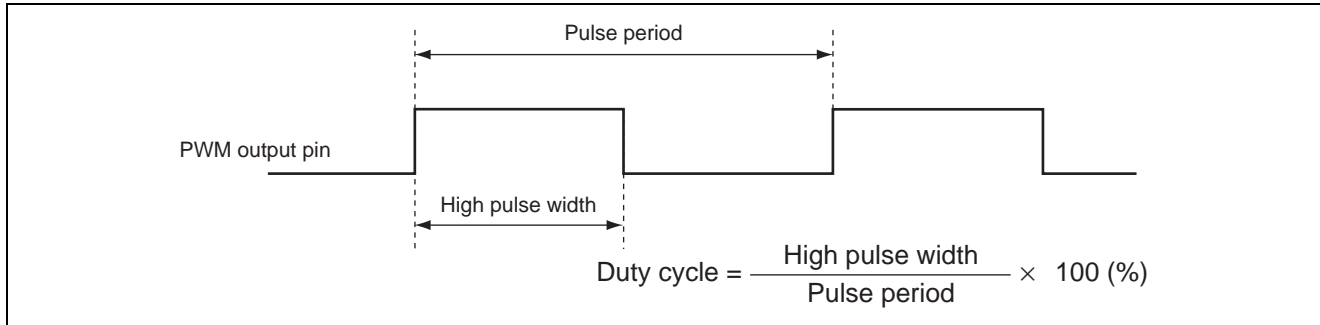
H8S/2128

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## 1. Specifications

- By using the 8-bit PWM function, duty cycle-controlled pulses are output through a PWM output pin as shown in figure 1.
- In this sample task, output pulses have a 50% duty cycle with the pulse period of 6.51  $\mu\text{s}$  and high pulse width of 3.26  $\mu\text{s}$ .



**Figure 1 50% Duty Cycle Pulse Output by 8-bit PWM Function**

## 2. Applicable Conditions

**Table 1 Applicable Conditions**

Item	Description
Operating frequency	Input clock: 19.6608 MHz
	System clock (I $\phi$ ): 19.6608 MHz
	Peripheral module clock (P $\phi$ ): 19.6608 MHz
	External bus clock (B $\phi$ ): 19.6608 MHz
Operating mode	Mode 3 (MD1 = 1, MD0 = 1)
Development tool	HEW: version 3.01 (release 1)
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler: version 6.0.00.005 (from Renesas Technology Corp.)
Compile options	-cpu = 2000N, -code = machinecode, -optimize = 1

### 3. Description of Functions

In this sample task, pulses with 50% duty cycle are output through a PWM output pin by using the 8-bit PWM function. Figure 2 shows the block diagram of the 8-bit PWM function which is described below.

- By pulse division, operation (PWM output) with a maximum carrier frequency of 1.22 MHz (when  $\phi = 19.6608$  MHz) is possible.
- The input clock for the PWM timer is selectable from among  $\phi$ ,  $\phi/2$ ,  $\phi/4$ ,  $\phi/8$ , and  $\phi/16$ .  
The system clock ( $\phi$ ) is a reference clock used to operate the CPU and its peripheral functions. The PWM resolution, period of PWM conversion, and carrier frequency are calculated from the selected internal clock by the following formulae:  
 Resolution (minimum pulse width) =  $1/\text{Internal clock frequency}$   
 PWM conversion period = Resolution  $\times$  256  
 Carrier frequency =  $16/\text{PWM conversion period}$
- The PWM data registers (PWDR0, PWDR15) are 8-bit readable/writable registers that specify the duty cycle of the basic pulses to be output and the number of additional pulses. The value set in PWDR is made up of two parts: the upper 4 bits specify the duty cycle of the basic pulse as 0/16 to 15/16 with a resolution of 1/16, and the lower 4 bits specify how many additional pulses are to be added within the conversion period, which consists of 16 basic pulses. Thus, the specifiable range of PWDR setting is from 0/256 to 255/256. For 256/256 (100%) output, port output should be used.
- The PWM data polarity registers (PWOERA, PWOERB) are a pair of 8-bit readable/writable registers that switch between PWM output and port output. The OS0 to OS15 bits in this register correspond to the PWM outputs of PW0 to PW15, respectively.
- The PWM output enable registers (PWPRA, PWPRB) are a pair of 8-bit readable/writable registers that control the polarity of PWM output. The OE0 to OE15 bits in this register correspond to the PWM outputs of PW0 to PW15, respectively. To make the pins to function as output pins, the data direction register of the corresponding port should also be set.
- Port 1 and port 2 data direction registers (P1DDR, P2DDR) are 8-bit write-only registers. Each bit of these registers sets the I/O direction or PWM output for its corresponding pin of port 1 or port 2. Port 1 pins are shared with the PW0 to PW7 pin functions, and port 2 pins are shared with the PW8 to PW15 pin functions. The bits that correspond to the pins for use as PWM output pins should be set to 1.
- Port 1 and port 2 data registers (P1DR, P2DR) are 8-bit readable/writable registers used to fix the PWM output to 1 (for OS = 0) or 0 (for OS = 1).

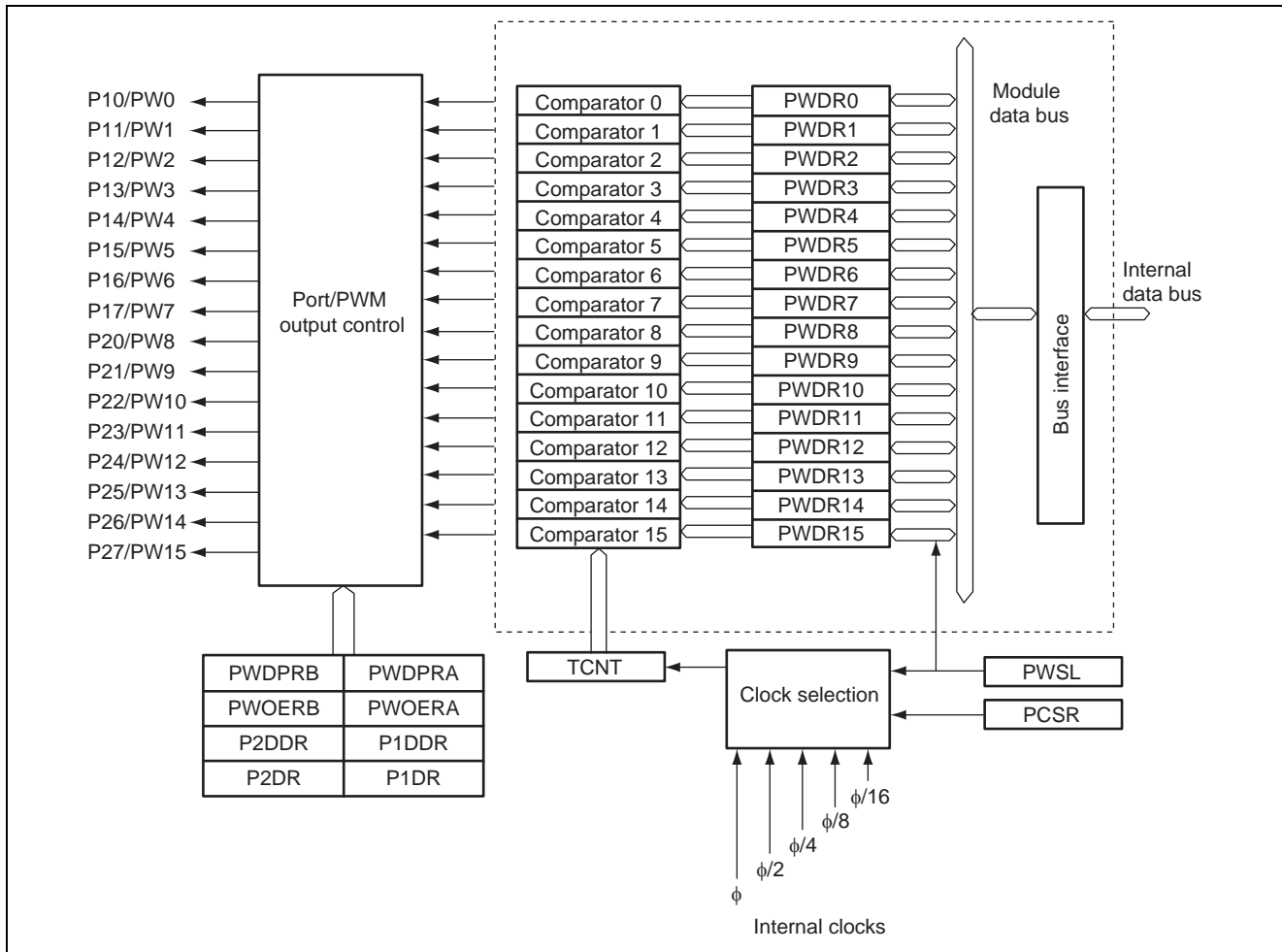


Figure 2 Block Diagram of 8-bit PWM Function

#### 4. Description of Operation

Figure 3 illustrates the output waveform of this sample task. Through the calculation using the formulae shown in figure 3, the period of PWM conversion, carrier frequency, and high pulse width of the basic pulse are found. Pulses with a 50% duty cycle are output by setting 8 in the upper 4 bits of the PWDR register.

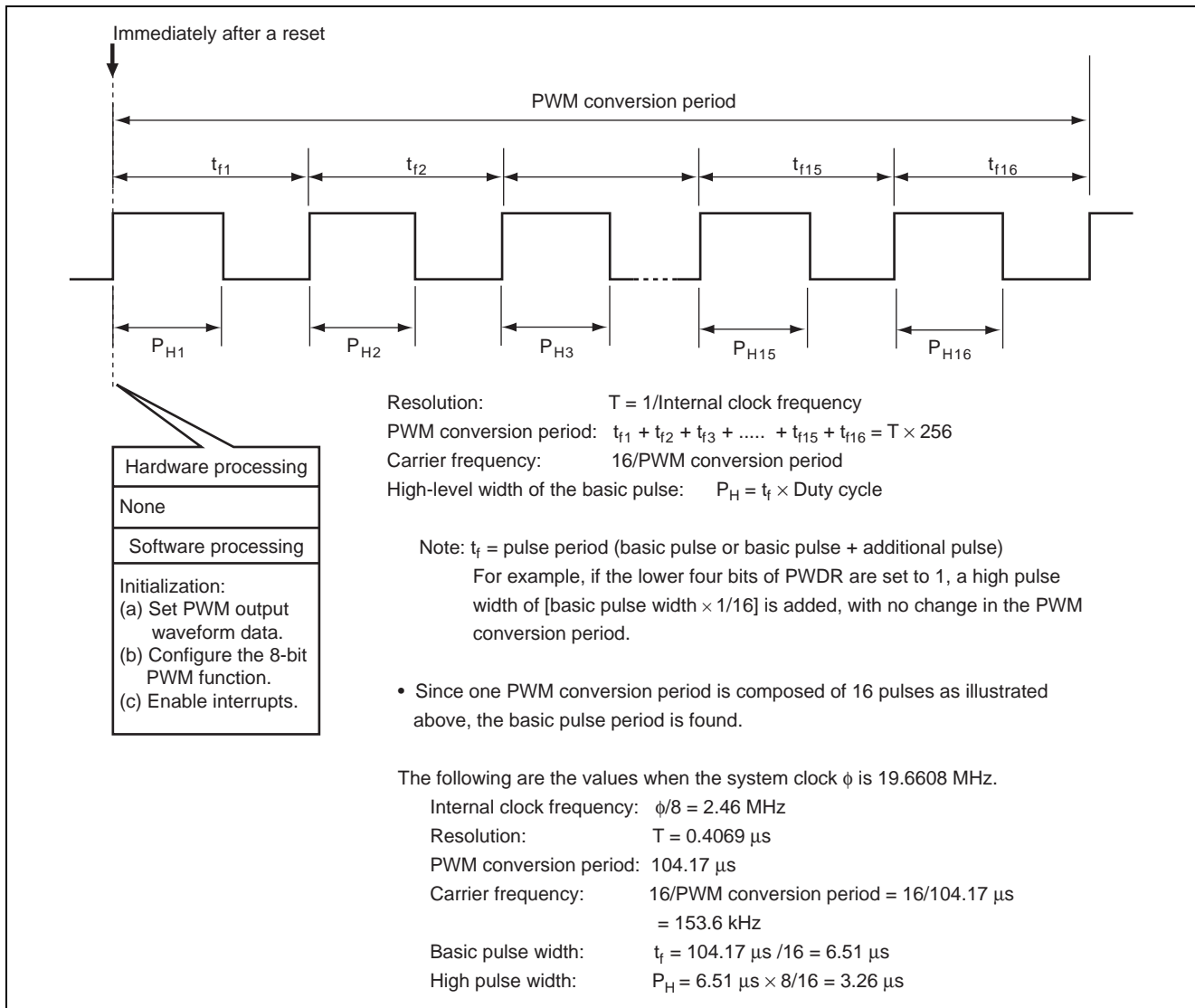
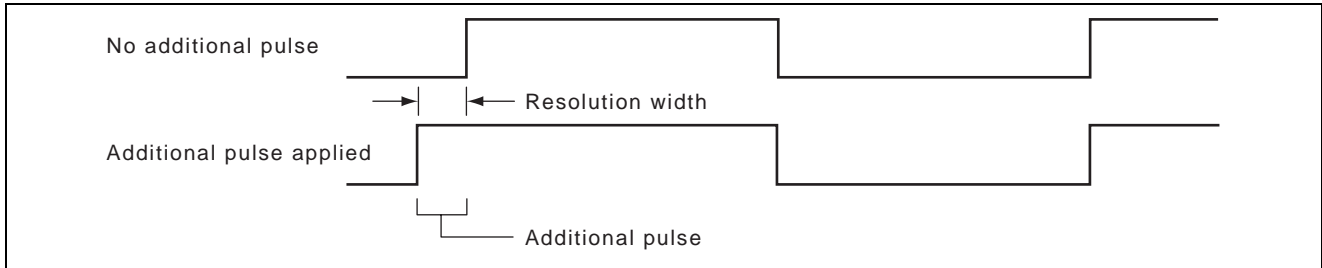


Figure 3 Operation of 50% Duty Cycle Pulse Output by Using 8-bit PWM Function

The position of additional pulse insertion to the 16 basic pulses is specified by the four lower bits of PWDR as shown in the following figure. An additional pulse is inserted before the rising edge of the basic pulse as a high-level period (when OS = 0) with a duration of the resolution. Refer to the hardware manual of the H8S/2128 for details on the additional pulse position with respect to the basic pulse.



**Figure 4 Timing of the Additional Pulse**



## 5. Description of Software

### 5.1 Module

**Table 2 Description of Module**

Module	Label	Function
Main Routine	main	Configures the 8-bit PWM function for pulse output and output the pulses.

### 5.2 Arguments

No argument is used in this sample task.

### 5.3 Internal registers

Table 3 describes the internal registers used in this sample task.

**Table 3 Description of Internal Registers**

Register	Function	Address	Setting
PWSL	PWCKE PWM Register Select (PWM clock enable) When PWCKE = 0, the clock input is disabled. When PWCKE = 1, the clock is as specified by PWCKS and PCSR.	H'FFFFD6 Bit 7	1
	PWCKS PWM Register Select (PWM clock select) When PWCKS = 0, the system clock ( $\phi$ ) is selected. When PWCKS = 1, the clock is selected by PCSR.	H'FFFFD6 Bit 6	1
RS3	PWM Register Select (Register select)	H'FFFFD6	0,0,0,0
RS2	RS3, RS2, RS1, RS0 = [0, 0, 0, 0]: PWDR0 is selected.	Bits 3,2,1,0	
RS1	RS3, RS2, RS1, RS0 = [0, 0, 0, 1] to [1, 1, 1, 0]: PWDR1 to		
RS0	PWDR14 is selected, respectively.		
	RS3, RS2, RS1, RS0 = [1, 1, 1, 1]: PWDR15 is selected.		
PWDR0	PWM Data Register 0 The four upper bits select the duty cycle of the basic pulse in the range from 0/16 to 15/16 with a resolution of 1/16. The four lower bits specify the number of additional pulses inserted within a PWM conversion period consisting of 16 basic pulses.	H'FFFFD7	H'80
PWDPRA	PWM Data Polarity Register A When OS7 to OS0 = 0, direct PWM output is selected for the corresponding bit. When OS7 to OS0 = 1, inverted PWM output is selected for the corresponding bit.	H'FFFFD5	H'00

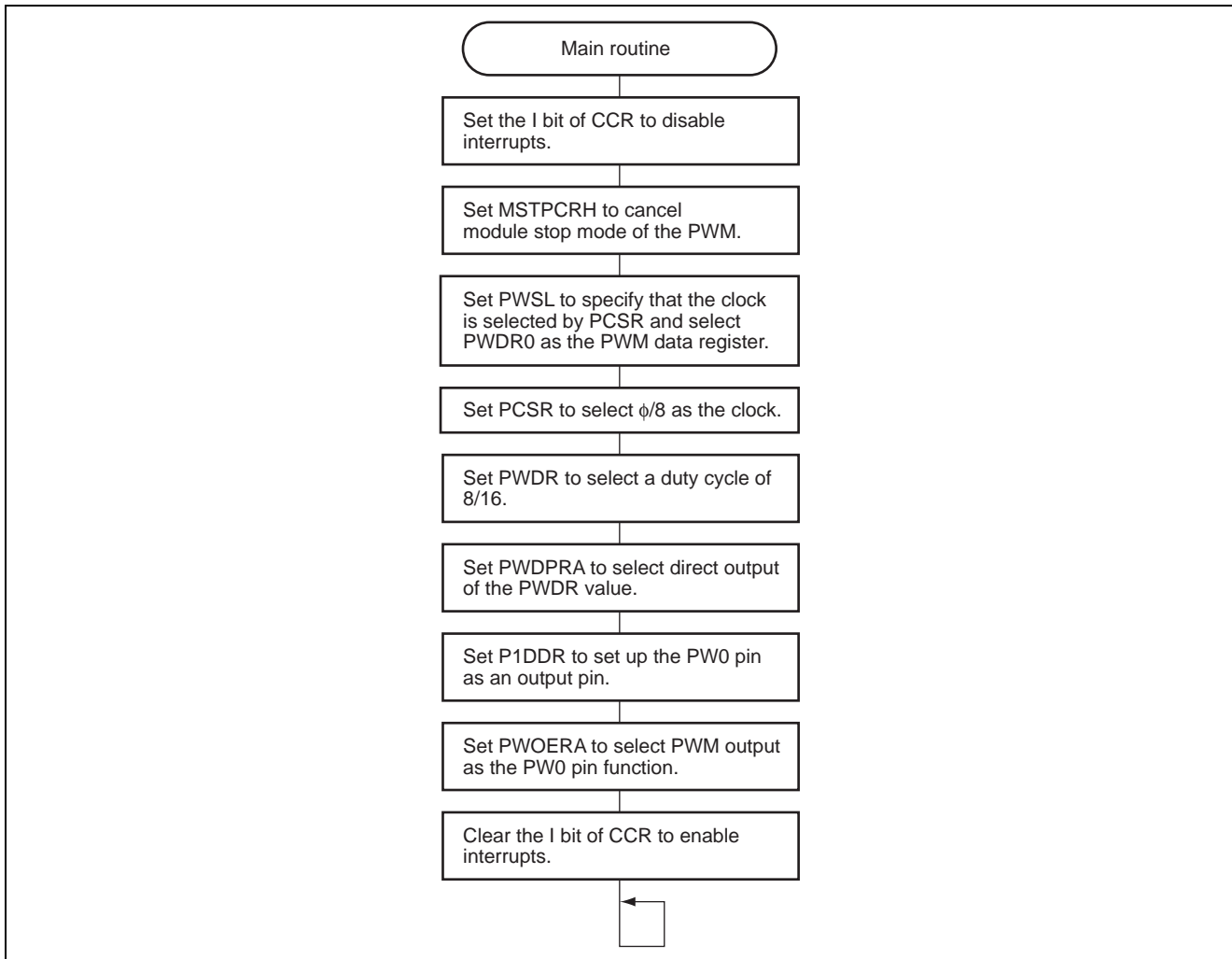
Register	Function	Address	Setting
PWOERA	<p>PWM Output Enable Register A</p> <p>When the bits in the data direction register DDR are cleared: The corresponding pins function as port input pins.</p> <p>When the bits in the data direction register DDR are set to 1: For bits OE7 to OE0 = 0, the corresponding pins function as port output or PWM output (fixed at 256/256) pins. For bits OE7 to OE0 = 1, the corresponding pins function as PWM output (0 to 256/256) pins.</p>	H'FFFFD3	H'01
PCSR	<p>Peripheral Clock Select Register (Peripheral clock select B, A)</p> <p>PWCKB, PWCKA = [0,0]: <math>\phi/2</math> is selected.</p> <p>PWCKB, PWCKA = [0,1]: <math>\phi/4</math> is selected.</p> <p>PWCKB, PWCKA = [1,0]: <math>\phi/8</math> is selected.</p> <p>PWCKB, PWCKA = [1,1]: <math>\phi/16</math> is selected.</p>	H'FFFF82	1, 0 Bits 2,1
P1DDR	<p>Port 1 Data Direction Register</p> <p>When P17DDR to P10DDR = 0, the corresponding bit of port 1 functions as an input pin.</p> <p>When P17DDR to P10DDR = 1, the corresponding bit of port 1 functions as an output pin.</p>	H'FFFFB0	1 Bit 0
MSTPCRH	<p>Module Stop Control Register</p> <p>When MSTP11 = 0, the PWM module stop mode is canceled.</p> <p>When MSTP11 = 1, the PWM module stop mode is set.</p>	H'FFFF86	0 Bit 11

## 5.4 RAM Usage

This sample task does not use RAM.

6. Flowchart

1. Main routine



### Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.09.05	—	First edition issued

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