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April 1\(^{st}\), 2010  
Renesas Electronics Corporation

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H8S Family
Using the 8-Bit PWM Function to Generate Duty Cycle-Controlled Pulse Output

Introduction
The 8-bit PWM function is used to output 50% duty cycle pulses from PWM output pin PW0 with the pulse period of 6.51 µs and high pulse width of 3.26 µs.

Target Device
H8S/2128

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1. Specifications

- By using the 8-bit PWM function, duty cycle-controlled pulses are output through a PWM output pin as shown in figure 1.
- In this sample task, output pulses have a 50% duty cycle with the pulse period of 6.51 µs and high pulse width of 3.26 µs.

\[
\text{Duty cycle} = \left( \frac{\text{High pulse width}}{\text{Pulse period}} \right) \times 100 \%
\]

![Figure 1](image_url)  
**Figure 1** 50% Duty Cycle Pulse Output by 8-bit PWM Function

2. Applicable Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| Operating frequency | Input clock: 19.6608 MHz  
   System clock (Iφ): 19.6608 MHz  
   Peripheral module clock (Pφ): 19.6608 MHz  
   External bus clock (Bφ): 19.6608 MHz |
| Operating mode    | Mode 3 (MD1 = 1, MD0 = 1)                                                  |
| Development tool  | HEW: version 3.01 (release 1)                                              |
| C/C++ compiler    | H8S, H8/300 Series C/C++ Compiler: version 6.0.00.005 (from Renesas Technology Corp.) |
| Compile options   | -cpu = 2000N, -code = machinecode, -optimize = 1                           |
3. **Description of Functions**

In this sample task, pulses with 50% duty cycle are output through a PWM output pin by using the 8-bit PWM function. Figure 2 shows the block diagram of the 8-bit PWM function which is described below.

- **By pulse division, operation (PWM output) with a maximum carrier frequency of 1.22 MHz (when $\phi = 19.6608$ MHz) is possible.**
- **The input clock for the PWM timer is selectable from among $\phi, \phi/2, \phi/4, \phi/8$, and $\phi/16$.**
  - The system clock ($\phi$) is a reference clock used to operate the CPU and its peripheral functions. The PWM resolution, period of PWM conversion, and carrier frequency are calculated from the selected internal clock by the following formulae:
    - Resolution (minimum pulse width) = $1/\text{Internal clock frequency}$
    - PWM conversion period = Resolution $\times 256$
    - Carrier frequency = $16/\text{PWM conversion period}$

- The PWM data registers (PWDR0, PWDR15) are 8-bit readable/writable registers that specify the duty cycle of the basic pulses to be output and the number of additional pulses. The value set in PWDR is made up of two parts: the upper 4 bits specify the duty cycle of the basic pulse as 0/16 to 15/16 with a resolution of 1/16, and the lower 4 bits specify how many additional pulses are to be added within the conversion period, which consists of 16 basic pulses. Thus, the specifiable range of PWDR setting is from 0/256 to 255/256. For 256/256 (100%) output, port output should be used.

- The PWM data polarity registers (PWOERA, PWOERB) are a pair of 8-bit readable/writable registers that switch between PWM output and port output. The OS0 to OS15 bits in this register correspond to the PWM outputs of PW0 to PW15, respectively.

- The PWM output enable registers (PWDPRA, PWDPRB) are a pair of 8-bit readable/writable registers that control the polarity of PWM output. The OE0 to OE15 bits in this register correspond to the PWM outputs of PW0 to PW15, respectively. To make the pins to function as output pins, the data direction register of the corresponding port should also be set.

- Port 1 and port 2 data direction registers (P1DDR, P2DDR) are 8-bit write-only registers. Each bit of these registers sets the I/O direction or PWM output for its corresponding pin of port 1 or port 2. Port 1 pins are shared with the PW0 to PW7 pin functions, and port 2 pins are shared with the PW8 to PW15 pin functions. The bits that correspond to the pins for use as PWM output pins should be set to 1.

- Port 1 and port 2 data registers (P1DR, P2DR) are 8-bit readable/writable registers used to fix the PWM output to 1 (for OS = 0) or 0 (for OS = 1).
Using the 8-Bit PWM Function to Generate Duty Cycle

Figure 2  Block Diagram of 8-bit PWM Function
4. Description of Operation

Figure 3 illustrates the output waveform of this sample task. Through the calculation using the formulae shown in figure 3, the period of PWM conversion, carrier frequency, and high pulse width of the basic pulse are found. Pulses with a 50% duty cycle are output by setting 8 in the upper 4 bits of the PWDR register.

Figure 3 Operation of 50% Duty Cycle Pulse Output by Using 8-bit PWM Function
The position of additional pulse insertion to the 16 basic pulses is specified by the four lower bits of PWDR as shown in the following figure. An additional pulse is inserted before the rising edge of the basic pulse as a high-level period (when OS = 0) with a duration of the resolution. Refer to the hardware manual of the H8S/2128 for details on the additional pulse position with respect to the basic pulse.

![Figure 4 Timing of the Additional Pulse](image-url)

**Figure 4 Timing of the Additional Pulse**
5. Description of Software

5.1 Module

Table 2 Description of Module

<table>
<thead>
<tr>
<th>Module</th>
<th>Label</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Routine</td>
<td>main</td>
<td>Configures the 8-bit PWM function for pulse output and output the pulses.</td>
</tr>
</tbody>
</table>

5.2 Arguments

No argument is used in this sample task.

5.3 Internal registers

Table 3 describes the internal registers used in this sample task.

Table 3 Description of Internal Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Function</th>
<th>Address</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWSL</td>
<td>PWM Register Select (PWM clock enable)</td>
<td>H'FFFFD6</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>When PWCKE = 0, the clock input is disabled.</td>
<td></td>
<td>Bit 7</td>
</tr>
<tr>
<td></td>
<td>When PWCKE = 1, the clock is as specified by PWCKS and PCSR.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWCKS</td>
<td>PWM Register Select (PWM clock select)</td>
<td>H'FFFFD6</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>When PWCKS = 0, the system clock (φ) is selected.</td>
<td></td>
<td>Bit 6</td>
</tr>
<tr>
<td></td>
<td>When PWCKS = 1, the clock is selected by PCSR.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RS3</td>
<td>PWM Register Select (Register select)</td>
<td>H'FFFFD6</td>
<td>0,0,0,0</td>
</tr>
<tr>
<td>RS2</td>
<td>RS3, RS2, RS1, RS0 = [0, 0, 0, 0]: PWDR0 is selected.</td>
<td></td>
<td>Bits 3,2,1,0</td>
</tr>
<tr>
<td>RS1</td>
<td>RS3, RS2, RS1, RS0 = [0, 0, 0, 1] to [1, 1, 1, 0]: PWDR1 to PWDR14 is selected, respectively.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RS0</td>
<td>RS3, RS2, RS1, RS0 = [1, 1, 1, 1]: PWDR15 is selected.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWDR0</td>
<td>PWM Data Register 0</td>
<td>H'FFFFD7</td>
<td>H'80</td>
</tr>
<tr>
<td></td>
<td>The four upper bits select the duty cycle of the basic pulse in the range from 0/16 to 15/16 with a resolution of 1/16.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>The four lower bits specify the number of additional pulses inserted within a PWM conversion period consisting of 16 basic pulses.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PWDTPRA</td>
<td>PWM Data Polarity Register A</td>
<td>H'FFFFD5</td>
<td>H'00</td>
</tr>
<tr>
<td></td>
<td>When OS7 to OS0 = 0, direct PWM output is selected for the corresponding bit.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>When OS7 to OS0 = 1, inverted PWM output is selected for the corresponding bit.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Register Function Address Setting

- **PWOERA**  
  - **Function:** PWM Output Enable Register A  
  - **Register Address:** H'FFFFD3  
  - **Setting:** H'01

When the bits in the data direction register DDR are cleared:
- The corresponding pins function as port input pins.

When the bits in the data direction register DDR are set to 1:
- For bits OE7 to OE0 = 0, the corresponding pins function as port output or PWM output (fixed at 256/256) pins.
- For bits OE7 to OE0 = 1, the corresponding pins function as PWM output (0 to 256/256) pins.

- **PCSR**  
  - **Function:** Peripheral Clock Select Register (Peripheral clock select B, A)  
  - **Register Address:** H'FFFF82  
  - **Setting:** Bits 2,1

- **PWCKB**  
  - **Setting:** φ/2 is selected.

- **PWCKA**  
  - **Setting:** φ/4 is selected.

- **P1DDR**  
  - **Function:** Port 1 Data Direction Register  
  - **Register Address:** H'FFFFB0  
  - **Setting:** Bit 0

When P17DDR to P10DDR = 0, the corresponding bit of port 1 functions as an input pin.
When P17DDR to P10DDR = 1, the corresponding bit of port 1 functions as an output pin.

- **MSTPCRH**  
  - **Function:** Module Stop Control Register  
  - **Register Address:** H'FFFF86  
  - **Setting:** Bit 11

When MSTP11 = 0, the PWM module stop mode is canceled.
When MSTP11 = 1, the PWM module stop mode is set.

### 5.4 RAM Usage

This sample task does not use RAM.
6. Flowchart

1. Main routine

```
Main routine

- Set the I bit of CCR to disable interrupts.
- Set MSTPCR to cancel module stop mode of the PWM.
- Set PWSL to specify that the clock is selected by PCSR and select PWDR0 as the PWM data register.
- Set PCSR to select φ/8 as the clock.
- Set PWDR to select a duty cycle of 8/16.
- Set PWDPRA to select direct output of the PWDR value.
- Set P1DDR to set up the PW0 pin as an output pin.
- Set PW0ERA to select PWM output as the PW0 pin function.
- Clear the I bit of CCR to enable interrupts.
```
## Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Mar.09.05</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>
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