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H8S Family

Using the 14-Bit PWM Function to Generate Duty Cycle-Controlled Pulse Output

Introduction

The 14-bit PWM function is used to output pulses of 5.87% duty cycle from a PWM output pin.

Target Device

H8S/2128

Contents

1. Specifications

- By using the 14-bit PWM function, duty cycle-controlled pulses are output through a PWM output pin as shown in figure 1.
- In this sample task, output pulses have a 5.87% duty cycle with the base cycle of 13.02 µs and high pulse width of 763 ns.

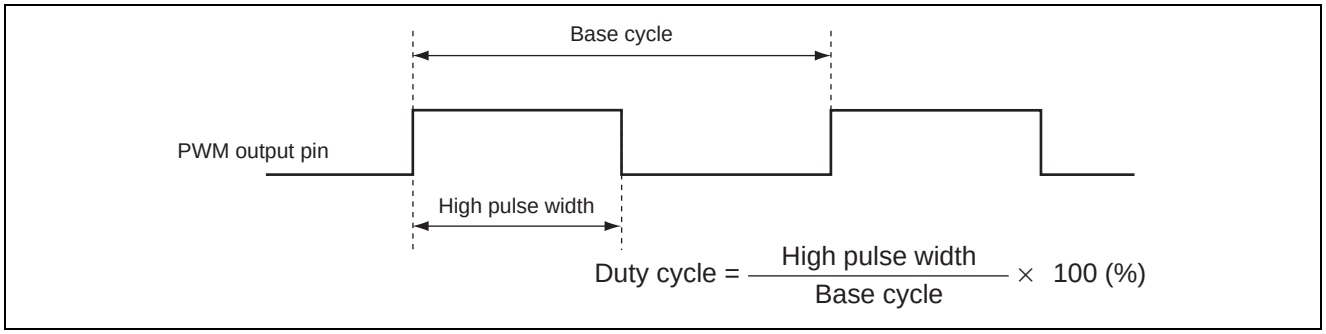


Figure 1 Duty Cycle-Controlled Pulse Output by 14-bit PWM Function

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description	
Operating frequency	Input clock:	19.6608 MHz
	System clock (Iϕ):	19.6608 MHz
	Peripheral module clock (Pϕ):	19.6608 MHz
	External bus clock (Bϕ):	19.6608 MHz
Operating mode	Mode 3 (MD1 = 1, MD0 = 1)	
Development tool	HEW: version 3.01 (release 1)	
C/C++ compiler	H8S, H8/300 Series C/C++ Compiler: version 6.0.00.005 (from Renesas Technology Corp.)	
Compile options	-cpu = 2000N, -code = machinecode, -optimize = 1	

3. Description of Functions

In this sample task, pulses with a specified duty cycle are output through a PWM output pin by using the 14-bit PWM function. Figure 2 shows the block diagram of the 14-bit PWM function which is described below.

- Either one system clock cycle or two system clock cycles can be selected as the resolution. The base cycle is selectable from two types: T × 64 or T × 256. This PWM function uses the pulse division method to reduce ripples.
- PWM (D/A) counter (DACNT)
  DACNT is a readable/writable14-bit up counter that counts the input clock pulses. The input clock is selected by the clock select bit (CKS) of the DACR register.
  DACNT is used to provide time base for the two-channel PWM (D/A). To use the PWM function with 14-bit precision, DACNT should be used with full bits. For 12-bit precision, the 12 lower bits should be used, ignoring the two upper bits.
- D/A data registers A and B (DADRA and DADRB)
  DADR consists of a pair of 16-bit readable/writable registers, DADRA and DADRB, which correspond to channels A and B, respectively, of the PWM (D/A) module. The least significant bit of DADRA has no function, and the value read from this bit is always 1. The upper 14 bits of DADR sets the data for D/A conversion and are continuously compared with the DACNT value to determine the duty cycle of the output waveform for each base cycle and also decide whether to output an additional pulse, which is equal in width to the resolution. To enable this operation, DADR must be set within a range that depends on the carrier frequency select bit (CFS). If any value outside this range is set, the PWM output is held constant.
  When used with 12-precision, the two lowest data bits (DA1 and DA0) are fixed to 0 and the upper 12 data bits are regarded as valid. This two lowest bits correspond to the two highest bits of the counter (DACNT).
- PWM (D/A) control register (DACR)
  DACR is an 8-bit readable/writable register that selects test mode, enables the output, and selects output phase and speed of operation.

Note: Although the CPU can read and write the DACNT and DADR values, data transfer between the CPU and these registers are performed via an 8-bit temporary register (TEMP) because DCANT and DADR are 16-bit registers. For more information, refer to the user's manual.

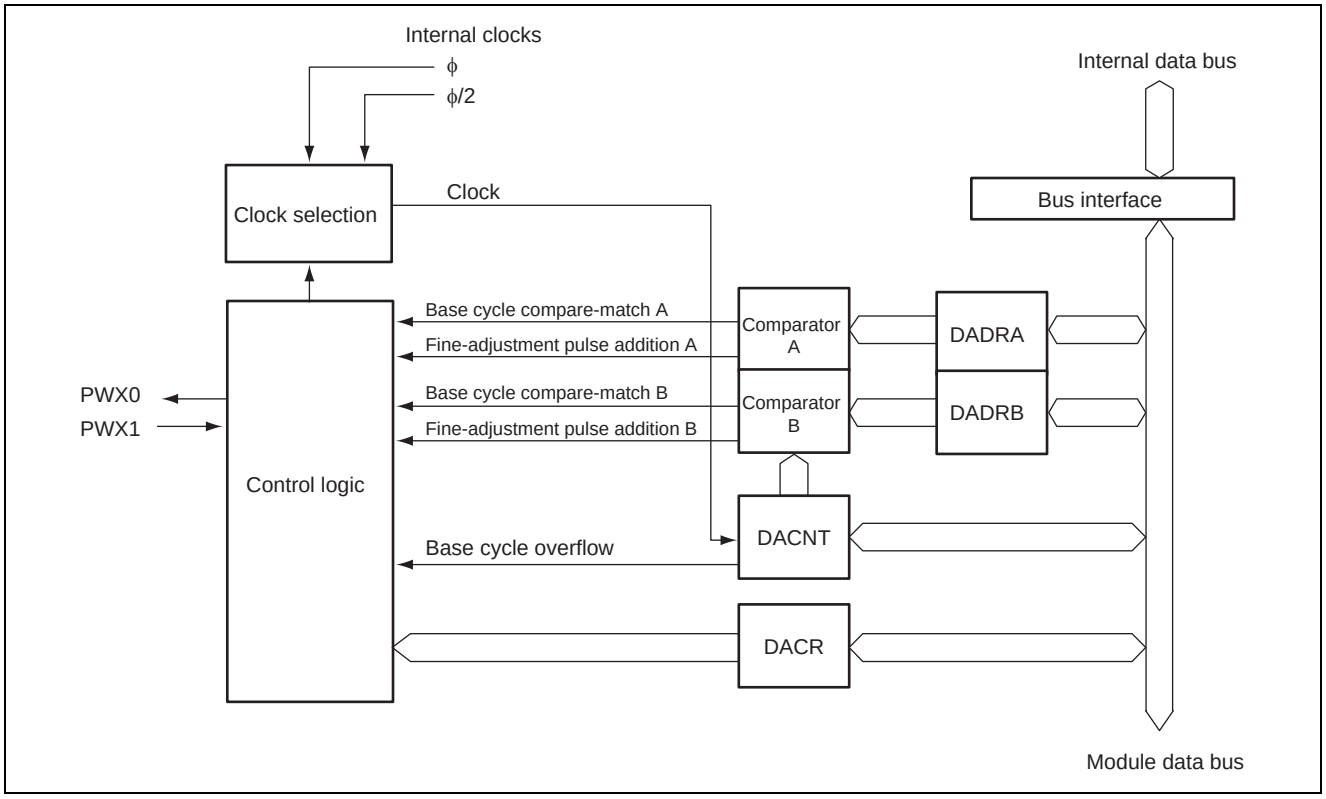


Figure 2 Block Diagram of 14-bit PWM Function

4. Description of Operation

Figure 3 illustrates the output waveform of this sample task. Through the calculation using the formulae shown in figure 3, the period of basic cycle, period of PWM conversion, and high-level pulse width are found.

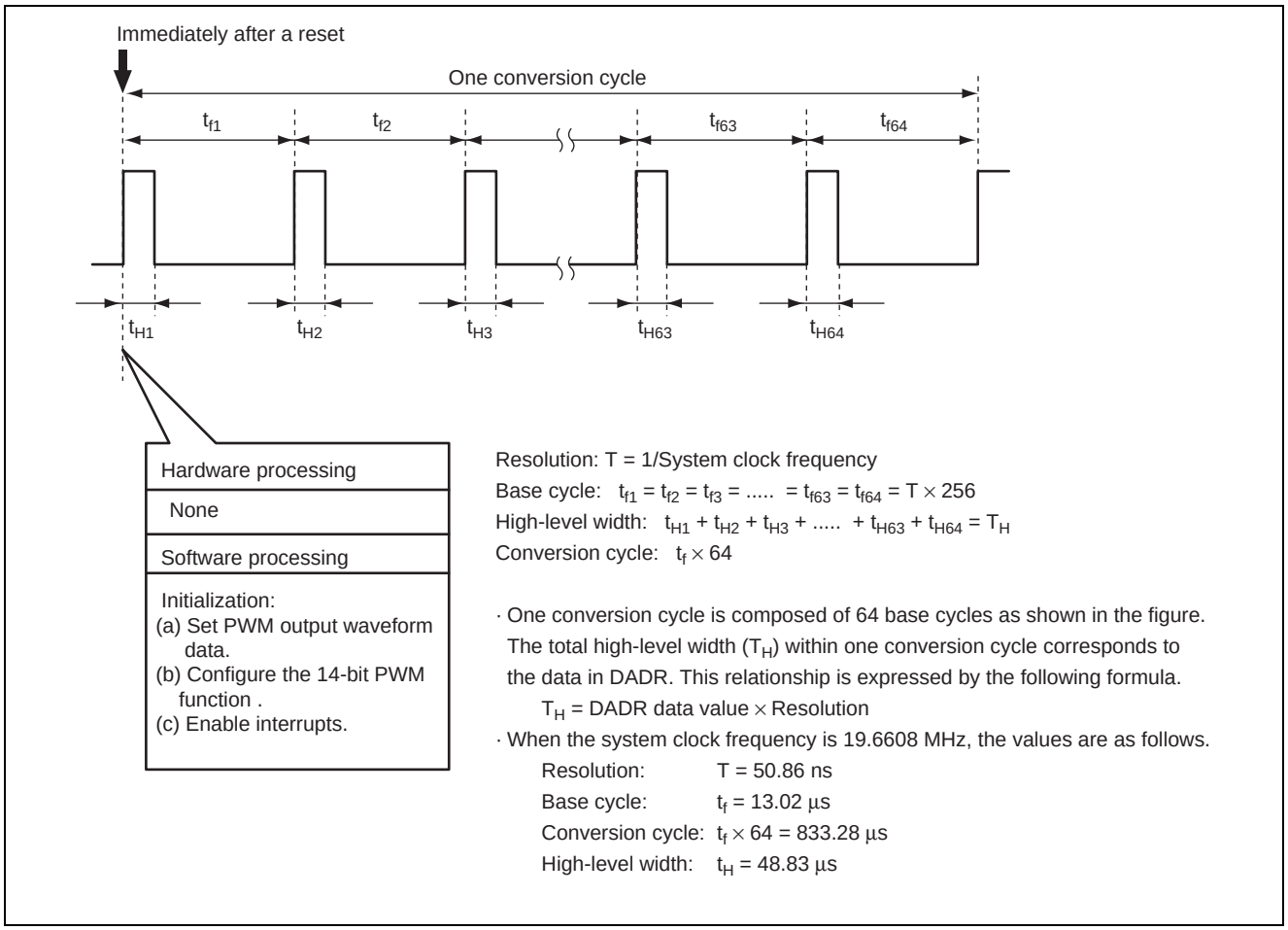


Figure 3 Operation of Duty Cycle-Controlled Pulse Output by Using 14-bit PWM Function

The additional pulse is described below for an example where CFS = 1 (base cycle = resolution (T) × 256) and OS = 1 (inverted PWM output). When CFS = 1, the duty cycle of the basic pulse is determined by the upper 8 bits of DADR (DA13 to DA6) and the position of the additional pulse by the following lower 6 bits (DA5 to DA0).

In this example, assume that DADR = H'0207 (B'0000 0010 0000 0111). The output waveform is shown in figure 4. Since CFS = 1 and the upper 8 bits are valued B'0000 0010, the duty cycle of the basic pulse is determined by the high-level pulse width of 2/256 × (T). Since the lower 6 bits are valued B'0000 0111, the additional pulse is only output for the 63rd basic pulse. (For details on the specification of additional pulse positions, refer to the hardware manual.) The additional pulse is added to a basic pulse by extending the pulse width by 1/256 × (T).

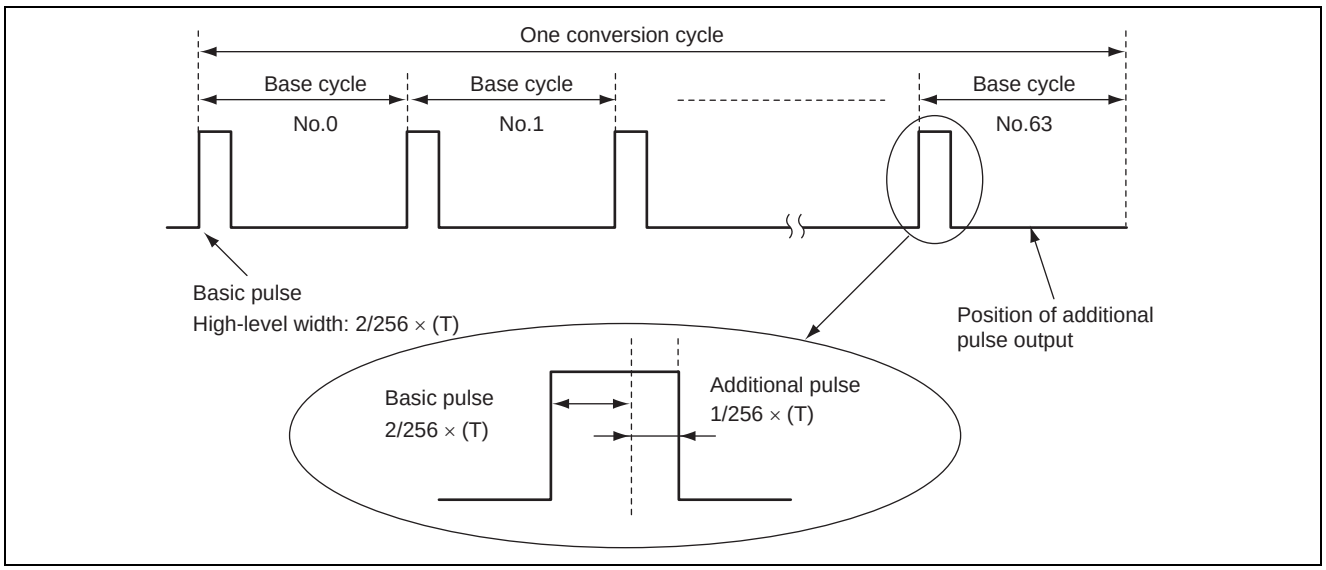


Figure 4 Output Waveform with Additional Pulse (DADR = H'0207, CFS = 1, OS = 1)

5. Description of Software

5.1 Modules

Table 2 describes the module in this sample task.

Table 2 Description of Module

Module	Label	Function
Main Routine	main	Configures the 14-bit PWM function and enables interrupts.

5.2 Arguments

Table 3 describes the argument used in this sample task.

Table 3 Description of Argument

Argument	Function	Used in	Data Size	Input/ Output
data	PWM output waveform data to be set in DADRA	main	1 word	Input

5.3 Internal registers

Table 4 describes the internal registers used in this sample task.

Table 4 Description of Internal Registers

Register		Function	Address	Setting
DACR	TEST	PWM (D/A) Control Register (Test mode) When TEST = 0, the PWM (D/A) module is in user mode for normal operation. When TEST = 1, the PWM (D/A) module is in test mode and does not produce correct results of conversion.	H'FFFFA0 Bit 7	0
	PWME	PWM (D/A) Control Register (PWM enable) When PWME = 0, the PWM (D/A) module operates as a 14-bit up counter. When PWME = 1, the PWM (D/A) module stops on DACNT = H'0003.	H'FFFFA0 Bit 6	0
	OEB	PWM (D/A) Control Register (Output enable B) When OEB = 0, output on channel B (PWX1 output pin) of the PWM (D/A) module is disabled. When OEB = 1, output on channel B (PWX1 output pin) of the PWM (D/A) module is enabled.	H'FFFFA0 Bit 3	0
	OEA	PWM (D/A) Control Register (Output enable A) When OEB = 0, output on channel A (PWX1 output pin) of the PWM (D/A) module is disabled. When OEB = 1, output on channel A (PWX1 output pin) of the PWM (D/A) module is enabled.	H'FFFFA0 Bit 2	1

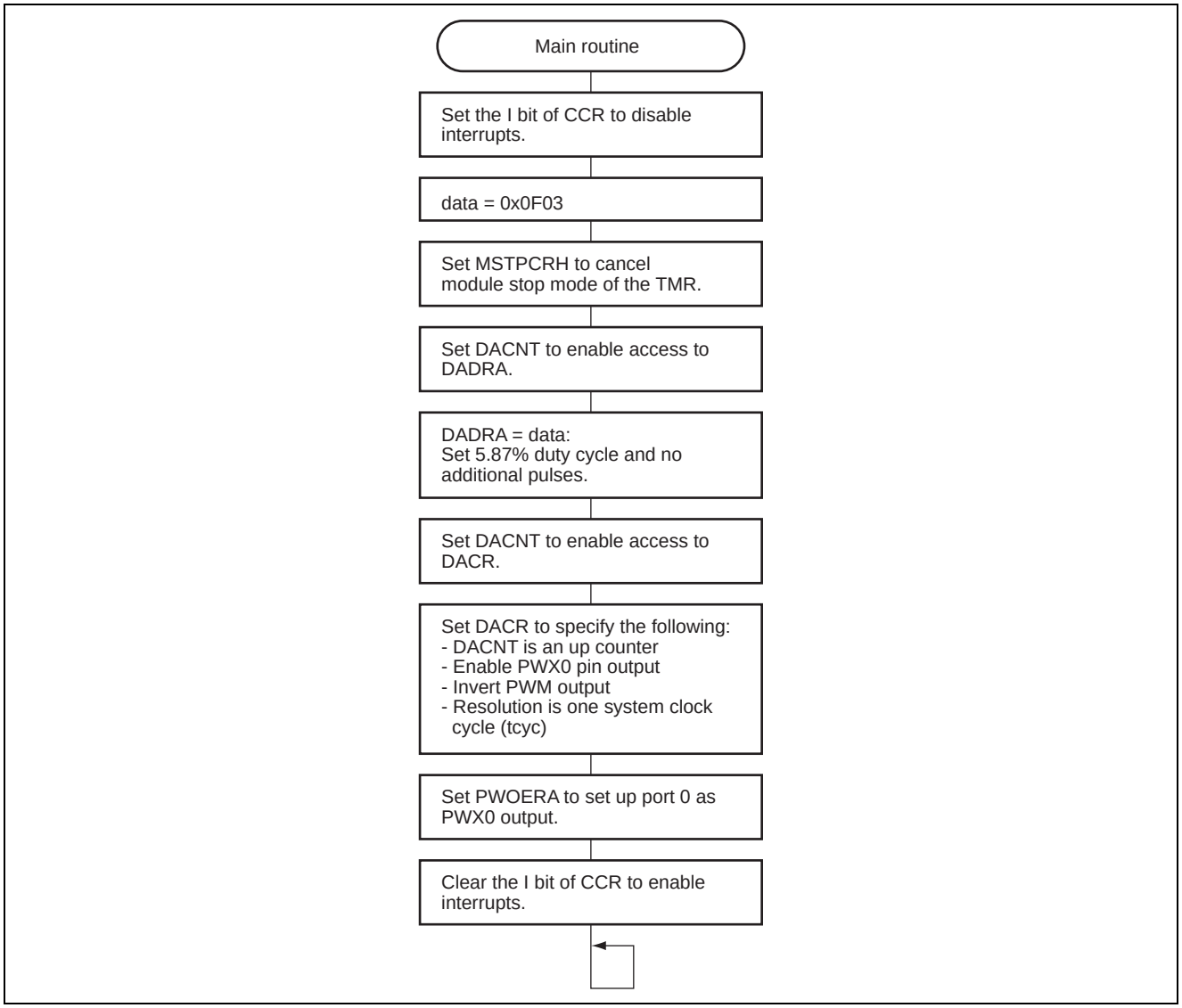
Register		Function	Address	Setting
DACR	OS	PWM (D/A) Control Register (Output select) When OS = 0, direct PWM output is selected. When OS = 1, inverted PWM output is selected.	H'FFFFA0 Bit 1	1
	CKS	PWM (D/A) Control Register (Clock select) When CKS = 0, the PWM (D/A) module operates with resolution (T) = one system clock cycle (t_{cyc}). When CKS = 1, the PWM (D/A) module operates with resolution (T) = two system clock cycles (t_{cyc}).	H'FFFFA0 Bit 0	0
DADRAH	DA13 to DA6	D/A Data Register A These bits set the upper 8 bits of the data for D/A conversion.	H'FFFFA0 Bits 15 to 8	H'FF
DADRAL	DA5 to DA0	D/A Data Register A These bits set the lower 6 bits of the data for D/A conversion.	H'FFFFA1 Bits 7 to 2	1, 1, 1, 1, 1, 1
	CFS	D/A Data Register A (Carrier frequency select) When CFS = 0, the PWM (D/A) module operates with base cycle = resolution (T) × 64. The value of DADR ranges from H'0401 to H'FFFD. When CFS = 1, the PWM (D/A) module operates with base cycle = resolution (T) × 256. The value of DADR ranges from H'0103 to H'FFFF.	H'FFFFA1 Bit 1	1
DACNT	—	PWM (D/A) Counter 14-bit up counter that can be read/written by the CPU.	H'FFFFA6 Bits 15 to 2	H'0000
	REGS	PWM (D/A) Counter (Register select) When REGS = 0, access to DADRA and DADRB is enabled. When REGS = 1, access to DACR and DACNT is enabled.	H'FFFFA6 Bit 0	0

5.4 RAM Usage

This sample task does not use RAM.

6. Flowchart

1. Main routine



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.09.05	—	First edition issued

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