To our customers,

---

**Old Company Name in Catalogs and Other Documents**

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: [http://www.renesas.com](http://www.renesas.com)

---

April 1st, 2010

Renesas Electronics Corporation

---

Issued by: Renesas Electronics Corporation ([http://www.renesas.com](http://www.renesas.com))

Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.

2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.

4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.

5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.

6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.

7. Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.

   "Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.

8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.

9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.

10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.

11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.
H8S Family
Two-Phase Excitation Control of a Stepping Motor

Introduction
This application note discusses how to implement two-phase excitation control of a two-phase stepping motor by using the TPU, PPG, and DTC functions of the H8S/2377.

Target Device
H8S/2377

Contents

1. Specifications .......................................................................................................................... 2
2. Applicable Conditions ........................................................................................................... 3
3. Description of Functions ....................................................................................................... 4
4. Description of Operation ...................................................................................................... 7
5. Description of Software ....................................................................................................... 12
6. Flowchart ............................................................................................................................ 19
1. Specifications

- A two-phase stepping motor is controlled using the TPU, PPG, and DTC functions incorporated in the H8S/2377.
- The stepping motor is controlled through two-phase excitation and repeats the following sequence: forward rotation → stop → reverse rotation → stop.
- Speed-up and slow-down processing is performed without software intervention.
- To protect the driver, a shoot-through current prevention period is set.

Figure 1 shows the connections for two-phase stepping motor control.

![Figure 1 Connections for Two-Phase Stepping Motor Control](image)
2. Applicable Conditions

Table 1  Applicable Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating frequency</td>
<td>Input clock: 19.6608 MHz</td>
</tr>
<tr>
<td></td>
<td>System clock: 19.6608 MHz</td>
</tr>
<tr>
<td></td>
<td>Peripheral module clock: 19.6608 MHz</td>
</tr>
<tr>
<td></td>
<td>External bus clock: 19.6608 MHz</td>
</tr>
<tr>
<td>Operating mode</td>
<td>Mode 4 (MD2 = 1, MD1 = 0, MD0 = 0)</td>
</tr>
<tr>
<td>Development tool</td>
<td>HEW Version 3.01.02</td>
</tr>
<tr>
<td>C/C++ compiler</td>
<td>H8S, H8/300 SERIES C/C++ Compiler Version 6.00.02</td>
</tr>
<tr>
<td></td>
<td>(from Renesas Technology Corp.)</td>
</tr>
<tr>
<td>Compile option</td>
<td>-cpu = 2000a:24, -code = machinecode, -optimize = 1, -regparam = 3</td>
</tr>
<tr>
<td></td>
<td>-speed = (register, shift, struct, expression)</td>
</tr>
</tbody>
</table>

Table 2  Section Settings

<table>
<thead>
<tr>
<th>Address</th>
<th>Section Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>H'000000</td>
<td>CV1</td>
<td>Reset vector</td>
</tr>
<tr>
<td>H'0000A0</td>
<td>CV2</td>
<td>TPU TGI0A interrupt vector</td>
</tr>
<tr>
<td>H'000450</td>
<td>DDTCV</td>
<td>DTC transfer request vector</td>
</tr>
<tr>
<td>H'001000</td>
<td>P</td>
<td>Program area</td>
</tr>
<tr>
<td></td>
<td>C</td>
<td>Data table storage</td>
</tr>
<tr>
<td>H'FF7000</td>
<td>B</td>
<td>RAM area</td>
</tr>
</tbody>
</table>
3. Description of Functions

3.1 Motor Specifications

This sample task uses a permanent magnet-type stepping motor (KP6P8-701 produced by Japan Servo Co., Ltd.). Table 3 summarizes the standard specifications of the KP6P8-701.

<table>
<thead>
<tr>
<th>Item</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Model</td>
<td>KP6P8-701</td>
</tr>
<tr>
<td>Number of phases</td>
<td>2</td>
</tr>
<tr>
<td>Step angle [degree/step]</td>
<td>7.5</td>
</tr>
<tr>
<td>Voltage [V]</td>
<td>12</td>
</tr>
<tr>
<td>Current [A/phase]</td>
<td>0.33</td>
</tr>
<tr>
<td>Winding resistance [Ω/phase]</td>
<td>36</td>
</tr>
<tr>
<td>Inductance [mH/phase]</td>
<td>28</td>
</tr>
<tr>
<td>Maximum static torque [mN•m]</td>
<td>78.4</td>
</tr>
<tr>
<td>Detent torque [mN•m]</td>
<td>1.3</td>
</tr>
<tr>
<td>Rotor inertia [g•cm²]</td>
<td>23.7</td>
</tr>
</tbody>
</table>

3.2 Description of Functions

The H8S/2377’s functions used to control the stepping motor are described below. Figure 2 is a block diagram of the functions used in this sample task.

- **DTC**
  - Activated by compare-match A of the TPU.
  - Transfers an output pattern in the output pattern table to the NDR register of the PPG. After the transfer of an output pattern, the DTC transfers the pulse period data in the period data table to the TGRB register of the TPU by chain transfer.

- **TPU**
  - Compare-match A: Activates the DTC and PPG.
  - Compare-match B: Clears the timer counter and activates the PPG.

- **PPG**
  - In this sample task, outputs 4 bits of pulse signals that include shoot-through current prevention period (non-overlap time).
  - Compare-match B: Outputs pulse signals of high-to-low transition and suspends output of low-to-high transition.
  - Compare-match A: Outputs the low-to-high pulse signals that are suspended on compare-match B above. (This output is delayed by the time set by TGRA.)
Figure 2  H8S/2377’s Functions Used in This Application
3.3 DTC Vector Table

Figure 3 shows an example of DTC vector table and memory allocation. The DTC register information is stored from address H'FFBC00 in this order: MRA, SAR, MRB, DAR, CRA, and CRB. In the DTC vector table, the lower 2 bytes (H'BC00) of the start address of register information is set.

![Diagram of DTC Vector Table and Memory Allocation](image)

**Figure 3** Example of DTC Vector Table and Memory Allocation
4. Description of Operation

4.1 Stepping Motor Operation

Figure 4 shows an example of two-phase stepping motor operation through two-phase excitation where the step angle of the motor is 7.5 degrees/step. The operation is summarized below.

- When the output pulse is high, the corresponding phase is excited, as shown in figure 4.
- Firstly, phases A and \( \overline{B} \) are excited and the rotor is positioned between phases \( \overline{B} \) and A.
- Next, phases A and B are excited simultaneously and the rotor is positioned between phases A and B. Subsequently, two adjacent phases are excited in the following sequence to cause the rotor to rotate: phases \( \overline{B} \) and A → phases A and B → phases B and \( \overline{A} \) → phases \( \overline{A} \) and \( \overline{B} \).
- Reverse rotation of the stepping motor is achieved by exciting the phases in the reverse sequence: phases \( \overline{A} \) and \( \overline{B} \) → phases B and \( \overline{A} \) → phases A and B → phases \( \overline{B} \) and A.
- The stepping motor is stopped by holding the phase excitation for a specified period at the last phase of forward or reverse rotation.
Figure 4  Example of Stepping Motor Operation
4.2 Non-Overlap Time

When the output pattern is switched, the shoot-through current prevention period \( n \) (non-overlap time) is inserted as shown in figure 5. The motor driver may be damaged by a turn-off delay that occurs when the excitation pattern is switched. Non-overlap time is inserted to prevent this problem.

![Figure 5 Example of Output with Non-Overlap Time](image)

4.3 Speed-Up and Slow-Down Operation

Speed-up and slow-down operations effectively prevent motor from being out of step. In particular, if a train of short-period pulses is suddenly output, the motor may not be able to handle the load and does not rotate. Speed-up and slow-down operation control is applied to avoid this problem. The speed-up and slow-down operation sequence is described below.

- The pulse period is gradually shortened until the specified number of pulses has been output (Speed up).
- The specified number of pulses with a fixed pulse period is output (Constant speed).
- The pulse period is gradually extended until the specified number of pulses has been output (Slow down).

![Figure 6 Speed-Up and Slow-Down Operations](image)
4.4 Flow of Stepping Motor Control

Figure 7 shows the flowchart of stepping motor control.
4.5 Example of Four-Phase Pulse Output

Figure 8 shows an example of four-phase output.

**Figure 8 Timing of Stepping Motor Operation**
5. Description of Software

5.1 List of Functions

Table 4 lists the functions used in this sample task. Figure 9 shows the function hierarchy in this sample task.

Table 4 List of Functions

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>init</td>
<td>Initialization routine: Cancels module stop mode, sets clocks, and calls main function.</td>
</tr>
<tr>
<td>main</td>
<td>Main routine: Initializes the TPU, PPG, and DTC and makes settings for forward speed-up operation.</td>
</tr>
<tr>
<td>tgi0a_int</td>
<td>TPU interrupt processing: Controls motor operation in each stage.</td>
</tr>
<tr>
<td>fslowup0</td>
<td>Called after completion of reverse stop operation and changes the DTC transfer modes for forward speed-up operation.</td>
</tr>
<tr>
<td>fconst0</td>
<td>Called after completion of forward speed-up operation and switches the DTC transfer modes for forward constant-speed operation.</td>
</tr>
<tr>
<td>fslowdwn0</td>
<td>Called after completion of forward constant-speed operation and changes the DTC transfer modes for forward slow-down operation.</td>
</tr>
<tr>
<td>rslowup0</td>
<td>Called after completion of forward stop operation and changes the DTC transfer modes for reverse speed-up operation.</td>
</tr>
<tr>
<td>rconst0</td>
<td>Called after completion of reverse speed-up operation and changes the DTC transfer modes for reverse constant-speed operation.</td>
</tr>
<tr>
<td>rslowdwn0</td>
<td>Called after completion of reverse constant-speed operation and changes the DTC transfer modes for reverse slow-down operation.</td>
</tr>
<tr>
<td>frstop0</td>
<td>Called after completion of reverse slow-down operation and changes the DTC transfer modes for stop operation.</td>
</tr>
</tbody>
</table>

![Figure 9 Hierarchy of Functions](image-url)
5.2 Constants

Table 5 lists the constants used in this sample task.

Table 5 Description of Constants

<table>
<thead>
<tr>
<th>Constant Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>UPTIME</td>
<td>49</td>
<td>Number of steps for speed-up and slow-down operations</td>
</tr>
<tr>
<td>CNSTTIME</td>
<td>481</td>
<td>Number of steps for constant-speed operation</td>
</tr>
<tr>
<td>STOPTIME</td>
<td>20</td>
<td>Number of steps for stop operation</td>
</tr>
</tbody>
</table>

5.3 Data Table Variables

- **Output Pattern Table**
  Data table of output patterns for stepping motor excitation.

  pattbl[4] = {
    0xF6, .... Excites phase B (PO0) and phase A (PO3)
    0xF3, .... Excites phase A (PO3) and phase B (PO2)
    0xF9, .... Excites phase B (PO2) and phase A (PO1)
    0xFC, .... Excites phase A (PO1) and phase B (PO0)
  };

- **Period Data Table**

  uptbl[49] = {
    0x4E00, 0x4D00, 0x4C00, 0x4B00, 0x4A00, 0x4900, 0x4800, 0x4700, 0x4600, 0x4500,
    0x4400, 0x4300, 0x4200, 0x4100, 0x4000, 0x3F00, 0x3E00, 0x3D00, 0x3C00, 0x3B00,
    0x3A00, 0x3900, 0x3800, 0x3700, 0x3600, 0x3500, 0x3400, 0x3200, 0x3000, 0x2E00,
    0x2D00, 0x2C00, 0x2B00, 0x2A00, 0x2900, 0x2800, 0x2700, 0x2600, 0x2500, 0x2400,
    0x2300, 0x2200, 0x2100, 0x2000, 0x1F00, 0x1E00, 0x1D00, 0x1C00, 0x1B00,
  };}
## 5.4 Internal Registers

- **System Clock Control Register (SCKCR)**  
  Address: H'FFFF3B

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>SCK2</td>
<td>0</td>
<td>System clock select 2, 1, 0</td>
</tr>
<tr>
<td>1</td>
<td>SCK1</td>
<td>0</td>
<td>00: Division ratio is 1/1.</td>
</tr>
<tr>
<td>0</td>
<td>SCK0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

- **Extension Module Stop Control Register H, L (EXMSTPCRH, EXMSTPCRL)**  
  Address: H'FFFF42, H'FFFF43

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>MSTP20</td>
<td>0</td>
<td>I²C bus interface 2_1 (IIC2_1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Cancels module stop mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Sets module stop mode.</td>
</tr>
<tr>
<td>3</td>
<td>MSTP19</td>
<td>0</td>
<td>I²C bus interface 2_0 (IIC2_0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Cancels module stop mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Sets module stop mode.</td>
</tr>
</tbody>
</table>

- **PLL Control Register (PLLCR)**  
  Address: H'FFFF45

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>STC1</td>
<td>0</td>
<td>Frequency multiplication factor setting</td>
</tr>
<tr>
<td>0</td>
<td>STC0</td>
<td>0</td>
<td>00: Frequency multiplication factor of the PLL circuit is ×1.</td>
</tr>
</tbody>
</table>
## H8S Family
Two-Phase Excitation Control of a Stepping Motor

- **Module Stop Control Register H, L (MSTPCRH, MSTPCRL)**
  - **Address:** H'FFFF40, H'FFFF41

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>ACSE</td>
<td>0</td>
<td>All-module-clocks-stop mode enable&lt;br&gt;0: Disables all-module-clocks-stop mode.&lt;br&gt;1: Enables all-module-clocks-stop mode.</td>
</tr>
<tr>
<td>14</td>
<td>MSTP14</td>
<td>0</td>
<td>EXDMA controller (EXDMA)&lt;br&gt;0: Cancels module stop mode.&lt;br&gt;1: Sets module stop mode.</td>
</tr>
<tr>
<td>13</td>
<td>MSTP13</td>
<td>0</td>
<td>DMA controller (DMAC)&lt;br&gt;0: Cancels module stop mode.&lt;br&gt;1: Sets module stop mode.</td>
</tr>
<tr>
<td>12</td>
<td>MSTP12</td>
<td>0</td>
<td>Data transfer controller (DTC)&lt;br&gt;0: Cancels module stop mode.&lt;br&gt;1: Sets module stop mode.</td>
</tr>
<tr>
<td>11</td>
<td>MSTP11</td>
<td>0</td>
<td>16-bit timer pulse unit (TPU)&lt;br&gt;0: Cancels module stop mode.&lt;br&gt;1: Sets module stop mode.</td>
</tr>
<tr>
<td>10</td>
<td>MSTP10</td>
<td>0</td>
<td>Programmable pulse generator (PPG)&lt;br&gt;0: Cancels module stop mode.&lt;br&gt;1: Sets module stop mode.</td>
</tr>
<tr>
<td>9</td>
<td>MSTP9</td>
<td>0</td>
<td>D/A converter (channels 0, 1)&lt;br&gt;0: Cancels module stop mode.&lt;br&gt;1: Sets module stop mode.</td>
</tr>
<tr>
<td>8</td>
<td>MSTP8</td>
<td>0</td>
<td>D/A converter (channels 2, 3)&lt;br&gt;0: Cancels module stop mode.&lt;br&gt;1: Sets module stop mode.</td>
</tr>
<tr>
<td>7</td>
<td>MSTP7</td>
<td>0</td>
<td>D/A converter (channels 4, 5)&lt;br&gt;0: Cancels module stop mode.&lt;br&gt;1: Sets module stop mode.</td>
</tr>
<tr>
<td>6</td>
<td>MSTP6</td>
<td>0</td>
<td>A/D converter&lt;br&gt;0: Cancels module stop mode.&lt;br&gt;1: Sets module stop mode.</td>
</tr>
<tr>
<td>5</td>
<td>MSTP5</td>
<td>0</td>
<td>Serial communication interface 4 (SCI_4)&lt;br&gt;0: Cancels module stop mode.&lt;br&gt;1: Sets module stop mode.</td>
</tr>
<tr>
<td>4</td>
<td>MSTP4</td>
<td>0</td>
<td>Serial communication interface 3 (SCI_3)&lt;br&gt;0: Cancels module stop mode.&lt;br&gt;1: Sets module stop mode.</td>
</tr>
<tr>
<td>3</td>
<td>MSTP3</td>
<td>0</td>
<td>Serial communication interface 2 (SCI_2)&lt;br&gt;0: Cancels module stop mode.&lt;br&gt;1: Sets module stop mode.</td>
</tr>
<tr>
<td>2</td>
<td>MSTP2</td>
<td>0</td>
<td>Serial communication interface 1 (SCI_1)&lt;br&gt;0: Cancels module stop mode.&lt;br&gt;1: Sets module stop mode.</td>
</tr>
<tr>
<td>1</td>
<td>MSTP1</td>
<td>0</td>
<td>Serial communication interface 0 (SCI_0)&lt;br&gt;0: Cancels module stop mode.&lt;br&gt;1: Sets module stop mode.</td>
</tr>
<tr>
<td>0</td>
<td>MSTP0</td>
<td>0</td>
<td>8-bit timer (TMR)&lt;br&gt;0: Cancels module stop mode.&lt;br&gt;1: Sets module stop mode.</td>
</tr>
</tbody>
</table>
### Port 2 Data direction Register (P2DDR)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>P23DDR</td>
<td>1</td>
<td>1111: P23 (PO3) to P20 (PO0) function as output port pins.</td>
</tr>
<tr>
<td>2</td>
<td>P22DDR</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>P21DDR</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>P20DDR</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

### DTC Enable Register C (DTCERC)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
</table>
| 13  | DTCEC5   | 1       | 0: Disables DCT activation by TG10A interrupt of the TPU_0.  
1: Enables DCT activation by TG10A interrupt of the TPU_0. |

### PPG Output Control Register (PCR)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>G0CMS1</td>
<td>0</td>
<td>Group 0 compare match select 1, 0</td>
</tr>
<tr>
<td>0</td>
<td>G0CMS0</td>
<td>0</td>
<td>00: Output of pulse output group 0 is triggered by compare-match of TPU channel 0.</td>
</tr>
</tbody>
</table>

### PPG Output Mode Register (PMR)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
</table>
| 4   | G0INV    | 1       | Group 0 invert  
0: Inverted output  
1: Direct output |
| 0   | G0NOV    | 1       | Group 0 non-overlap  
0: Normal operation.  
1: Non-overlap operation. |

### Next Data Enable Register L (NDERL)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>NDER7</td>
<td>0</td>
<td>Next data enable 7 to 0</td>
</tr>
<tr>
<td>6</td>
<td>NDER6</td>
<td>0</td>
<td>When a bit in this register is set to 1, data of the corresponding bit in NDRL is transferred to PODRL, triggered by the selected output trigger. Data transfer from NDRL to PODRL does not take place for the bits whose corresponding bits in this register are clear.</td>
</tr>
<tr>
<td>5</td>
<td>NDER5</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>NDER4</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>NDER3</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>NDER2</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>NDER1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>NDER0</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>
### Output Data Register L (PODRL)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>POD7</td>
<td>0</td>
<td>Output data register 7 to 0</td>
</tr>
<tr>
<td>6</td>
<td>POD6</td>
<td>0</td>
<td>For the bits set to generate pulse outputs by NDERL, the values of the corresponding bits in NDRL are transferred to this register by the output trigger during PPG operation. While a bit in NDERL is set to 1, the CPU cannot write to the corresponding bit of this register. While a bit in NDERL is clear, the initial pulse output value can be set in the corresponding bit of this register.</td>
</tr>
<tr>
<td>5</td>
<td>POD5</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>POD4</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>POD3</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>POD2</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>POD1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>POD0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

### Next Data Register L (NDRL)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>NDER3</td>
<td>1</td>
<td>Next data 3 to 0</td>
</tr>
<tr>
<td>2</td>
<td>NDER2</td>
<td>1</td>
<td>The contents of this register are transferred to the corresponding bits in the PODRL by the output trigger specified by PCR.</td>
</tr>
<tr>
<td>1</td>
<td>NDER1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>NDER0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

### Timer Start Register (TSTR)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>CST0</td>
<td>1</td>
<td>Counter start 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Stops counting by TCNT_0 of the TPU.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Starts counting by TCNT_0 of the TPU.</td>
</tr>
</tbody>
</table>

### Timer Control Register_0 (TCR_0)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>CCLR2</td>
<td>0</td>
<td>Counter clear 2 to 0</td>
</tr>
<tr>
<td>6</td>
<td>CCLR1</td>
<td>1</td>
<td>010: Clear TCNT_0 on compare match or input capture by TGRB_0.</td>
</tr>
<tr>
<td>5</td>
<td>CCLR0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>CKEG1</td>
<td>0</td>
<td>Clock edge 1, 0</td>
</tr>
<tr>
<td>3</td>
<td>CKEG0</td>
<td>0</td>
<td>00: The counter counts the falling edges when an internal clock is input, or counts the rising edges when an external clock is input.</td>
</tr>
<tr>
<td>2</td>
<td>TPSC2</td>
<td>0</td>
<td>Timer prescaler 2 to 0</td>
</tr>
<tr>
<td>1</td>
<td>TPSC1</td>
<td>1</td>
<td>010: The counter clock source is the internal clock Pφ/16.</td>
</tr>
<tr>
<td>0</td>
<td>TPSC0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

### Timer Interrupt Enable Register_0 (TIER_0)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>TGIEA</td>
<td>1</td>
<td>TGR interrupt enable A</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disables interrupt request (TGIA) generation by the TGFA bit.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enables interrupt request (TGIA) generation by the TGFA bit.</td>
</tr>
</tbody>
</table>
• Timer Status Register_0 (TSR_0)  
  Address: H'FFFFD5

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
</table>
| 1   | TGFB     | 0       | Input capture/output compare flag B  
Indicates the occurrence of TGRB input capture or compare match.  
0: Input capture or compare match has not occurred.  
1: Input capture or compare match has occurred. |
| 0   | TGFA     | 0       | Input capture/output compare flag A  
Indicates the occurrence of TGRA input capture or compare match.  
0: Input capture or compare match has not occurred.  
1: Input capture or compare match has occurred. |

• Timer General Register A_0 (TGRA_0)  
  Address: H'FFFFD8
  — Function: A 16-bit register that is compared with the counter in output compare operation.
  — Setting value: H'00000064

• Timer General Register B_0 (TGRB_0)  
  Address: H'FFFFDA
  — Function: A 16-bit register that is compared with the counter in output compare operation.
  — Setting value: H'0000FF00

5.5 RAM Usage

Table 6 describes the RAM usage in this sample task.

<table>
<thead>
<tr>
<th>Type</th>
<th>Variable Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DTC_tag</td>
<td>PTN0</td>
<td>Output pattern register information for motor</td>
</tr>
<tr>
<td>DTC_tag</td>
<td>CYC0</td>
<td>Period data register information for motor</td>
</tr>
</tbody>
</table>
| unsigned char | nextmode0   | Sets stepping motor operating mode.  
0: Forward speed-up control  
1: Forward constant-speed control  
2: Forward slow-down control  
3: Stop control  
4: Reverse speed-up control  
5: Reverse constant-speed control  
6: Reverse slow-down control  
7: Stop control |
6. Flowchart

6.1 init Function

- **init**
  - H'80 → CCR
    - Initialize CCR to disable interrupts.
  - H'00 → SCKCR
    - System clock division ratio = 1/1
  - H'00 → PLLCR
    - Frequency multiplication factor of the PLL circuit = ×1
  - H'00 → MSTPCRH
  - H'00 → MSTPCRL
  - H'FF → EXMSTPCRH
  - H'E5 → EXMSTPCRH
    - Cancel module stop mode of all the modules.

- **main**
### 6.2 main Function

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
</table>
| 1    | nextmode0 = 1  
Set the initial value of motor control mode. |
| 1    | PODRL = H'09  
Set the first output value in PODR. |
| 1    | NDERL = H'0F  
Set up PPG output pins. |
| 1    | PCR = H'E4  
Select the compare match output trigger: for Group 0, compare match of TPU0. |
| 1    | PMR = H'FF  
For all groups, select - Direct output - Non-overlap operation |
| 1    | NDRL_B = H'FC  
Set the next pulse output value. |
| 1    | P2DDR = H'0F  
Specifies P20 to P23 as output pins. |
| 1    | tmp = DTCCR  
DTCCR=H'00  
Stop the DTC and clear flags. |
| 1    | PTN0.DTC1.SAR = pattbl  
Set the start address of output pattern table as transfer source. |
| 2    | PTN0.DTC2.DAR = (&NDRL_B)  
Set NDRL_B as transfer source. |
| 2    | TCNT_0 = H'0065  
Load TCNT with the initial value. |
| 2    | PTN0.DTC2.MRB = H'80  
- Execute chain transfer.  
- Disable DTC interrupts. |
| 2    | PTN0.CRA = H'0404  
- Number of transfers = 4  
- Transfer counter = 4 |
| 2    | CYC0.DTC1.SAR = uptbl  
Set the start address of period data table as transfer source. |
| 2    | CYC0.DTC1.MRA = H'81  
- Increment SAR after transfer.  
- Fix DAR after transfer.  
- Select normal transfer mode.  
- Select word transfer. |
| 2    | CYC0.DTC2.DAR = (&TGRB_0)  
Set TBRB_0 as transfer source. |
| 2    | CYC0.DTC2.MRB = H'00  
- Disable chain transfer.  
- Disable DTC interrupts. |
| 2    | CYC0.CRA = UPTIME  
- Transfer counter = UPCNT |
| 2    | DTCERC.b5 = 1  
Enable DTC activation by TGIOA interrupts. |
| 2    | CYC0.DTC1.MRA = H'86  
- Increment SAR after transfer.  
- Fix DAR after transfer.  
- Select repeat transfer mode.  
- Specify the source as the repeat area.  
- Select byte transfer. |
| 2    | CYC0.DTC2.MRB = H'00  
- Disable chain transfer.  
- Disable DTC interrupts. |
| 2    | CYC0.CRA = UPTIME  
- Transfer counter = UPCNT |
| 2    | TGRB_0 = H'FF00  
Set the period of PPG output trigger. |
| 2    | TGRB_0 = H'FF00  
Set the non-overlap period. |
| 2    | TIER_0 = H'41  
Enable TGIA interrupt requests. |
| 2    | TSR_0 = H'C0  
Clear the TPU flag. |
| 2    | I = 0  
Enable interrupts. |
| 2    | TPU_TSTR = H'01  
Start counting by TCNT0. |
6.3  tgi0a_int Function

```
\begin{center}
\begin{tikzpicture}
  \node[coordinate] (start) at (0,0) {tgi0a_int};
  \node[coordinate] (mode) at (0,-1) {nextmode0 \?}
  \node[coordinate] (fslowup0) at (-2,-2) {fslowup0 \ Forward speed-up}
  \node[coordinate] (fconst0) at (-1,-2) {fconst0 \ Forward constant-speed}
  \node[coordinate] (fslowdwn0) at (0,-2) {fslowdwn0 \ Forward slow-down}
  \node[coordinate] (frstop0) at (1,-2) {frstop0 \ Rotation stop}
  \node[coordinate] (rslowup0) at (-2,-3) {rslowup0 \ Reverse speed-up}
  \node[coordinate] (rconst0) at (-1,-3) {rconst0 \ Reverse constant-speed}
  \node[coordinate] (rslowdwn0) at (0,-3) {rslowdwn0 \ Reverse slow-down}
  \node[coordinate] (frstop0) at (1,-3) {frstop0 \ Rotation stop}

  \draw[->] (start) -- (mode);
  \draw[->] (mode) -- node[above] {0} (fslowup0);
  \draw[->] (mode) -- node[above] {1} (fconst0);
  \draw[->] (mode) -- node[above] {2} (fslowdwn0);
  \draw[->] (mode) -- node[above] {3} (frstop0);

  \draw[->] (mode) -- node[above] {4} (rslowup0);
  \draw[->] (mode) -- node[above] {5} (rconst0);
  \draw[->] (mode) -- node[above] {6} (rslowdwn0);
  \draw[->] (mode) -- node[above] {7} (frstop0);

  \draw[->] (fslowup0) -- node[above] {nextmode = 1} node[below] {Go on to forward constant-speed mode.} (fconst0);
  \draw[->] (fconst0) -- node[above] {nextmode = 2} node[below] {Go on to forward slow-down mode.} (fslowdwn0);
  \draw[->] (fslowdwn0) -- node[above] {nextmode = 3} node[below] {Go on to rotation stop mode.} (frstop0);
  \draw[->] (frstop0) -- node[above] {nextmode = 4} node[below] {Go on to reverse speed-up mode.} (rslowup0);

  \draw[->] (rslowup0) -- node[above] {nextmode = 5} node[below] {Go on to constant-speed mode.} (rconst0);
  \draw[->] (rconst0) -- node[above] {nextmode = 6} node[below] {Go on to reverse slow-down mode.} (rslowdwn0);
  \draw[->] (rslowdwn0) -- node[above] {nextmode = 7} node[below] {Go on to rotation stop mode.} (frstop0);
  \draw[->] (frstop0) -- node[above] {nextmode = 0} node[below] {Go on to forward speed-up mode.} (fslowup0);

  \draw[->] (rslowup0) -- node[above] {1} (fconst0);
  \draw[->] (rconst0) -- node[above] {1} (fslowdwn0);
  \draw[->] (rslowdwn0) -- node[above] {1} (frstop0);
  \draw[->] (frstop0) -- node[above] {1} (rslowup0);

  \node[draw,rounded corners] at (-2,-4) {DTCERC.b5 = 1 \ Enable DTC activation by TGI0A interrupts.};
  \node[draw,rounded corners] at (-2,-5) {TSR_0 \&= H'FE \ Clear the flag.};

  \node[draw,rounded corners] at (-2,-8) {End};
\end{tikzpicture}
\end{center}
```
6.4 fslowup0 Function

PTN0.DTC1.SAR = pattbl
Set the start address of the output pattern table as transfer source.

PTN0.DTC1.MRA = H'86
- Increment SAR after transfer.
- Fix DAR after transfer.
- Select repeat transfer mode.
- Set the source as repeat area.
- Select byte transfer.

PTN0.CRA = H'0404
- Number of transfers = 4
- Transfer counter = 4

CYC0.DTC1.SAR = uptbl
Set the start address of the period data table as transfer source.

CYC0.DTC1.MRA = H'81
- Increment SAR after transfer.
- Fix DAR after transfer.
- Select normal transfer mode.
- Select word transfer.

CYC0.CRA = UPTIME
- Transfer counter = UPTIME

End
### 6.5 fconst0 Function

<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTN0.DTC1.SAR = pattbl</td>
<td>Set the start address of the output pattern table as transfer source.</td>
</tr>
</tbody>
</table>
| PTN0.DTC1.MRA = H'86 | - Increment SAR after transfer.  
- Fix DAR after transfer.  
- Select repeat transfer mode.  
- Set the source as repeat area.  
- Select byte transfer. |
| PTN0.CRA = H'0404 | - Number of transfers = 4  
- Transfer counter = 4 |
| CYC0.DTC1.SAR = &uptbl[UPTIME-1] | Set the end address of the period data table as transfer source. |
| CYC0.DTC1.MRA = H'01 | - Increment SAR after transfer.  
- Fix DAR after transfer.  
- Select normal transfer mode.  
- Select word transfer. |
| CYC0.CRA = CNSTTIME | - Transfer counter = CNSTTIME |

End
6.6 fslowdwn0 Function

- **PTN0.DTC1.SAR = pattbl**
  - Set the start address of the output pattern table as transfer source.

- **PTN0.DTC1.MRA = H'86**
  - Increment SAR after transfer.
  - Fix DAR after transfer.
  - Select repeat transfer mode.
  - Set the source as repeat area.
  - Select byte transfer.

- **PTN0.CRA = H'0404**
  - Number of transfers = 4
  - Transfer counter = 4

- **CYC0.DTC1.SAR = & uptbl[UPTIME - 1]**
  - Set the end address of the period data table as transfer source.

- **CYC0.DTC1.MRA = H'C1**
  - Decrement SAR after transfer.
  - Fix DAR after transfer.
  - Select normal transfer mode.
  - Select word transfer.

- **CYC0.CRA = UPTIME**
  - Transfer counter = UPTIME

**End**
6.7  rslowup0 Function

PTN0.DTC1.SAR=&pattbl[3]
Set the end address of the output pattern table as transfer source.

PTN0.DTC1.MRA = H'C6
- Decrement SAR after transfer.
- Fix DAR after transfer.
- Select repeat transfer mode.
- Set the source as repeat area.
- Select byte transfer.

PTN0.CRA = H'0404
- Number of transfers = 4
- Transfer counter = 4

CYC0.DTC1.SAR=uptbl
Set the start address of the period data table as the transfer source.

CYC0.DTC1.MRA = H'81
- Increment SAR after transfer.
- Fix DAR after transfer.
- Select normal transfer mode.
- Select word transfer.

CYC0.CRA = UPTIME
- Transfer counter = UPTIME

End
6.8 rconst0 Function

PTN0.DTC1.SAR = & pattbl[3]
- Set the end address of the output pattern table as transfer source.

PTN0.DTC1.MRA = H'C6
- Decrement SAR after transfer.
- Fix DAR after transfer.
- Select repeat transfer mode.
- Set the source as repeat area.
- Select byte transfer.

PTN0.CRA = H'0404
- Number of transfers = 4
- Transfer counter = 4

CYC0.DTC1.SAR = & uptbl[UPTIME-1]
- Set the end address of the perioddata table as transfer source.

CYC0.DTC1.MRA = H'01
- Increment SAR after transfer.
- Fix DAR after transfer.
- Select normal transfer mode.
- Select word transfer.

CYC0.CRA = CNSTTIME
- Transfer counter = CNSTTIME

End
6.9 rslowdwn0 Function

PTN0.DTC1.SAR = & pattbl[3]
Set the end address of the output pattern table as transfer source.

PTN0.DTC1.MRA = H'C6
- Decrement SAR after transfer.
- Fix DAR after transfer.
- Select repeat transfer mode.
- Set the source as repeat area.
- Select byte transfer.

PTN0.CRA = H'0404
- Number of transfers = 4
- Transfer counter = 4

CYC0.DTC1.SAR = & uptbl[UPTIME-1]
Set the end address of the period data table as transfer source.

CYC0.DTC1.MRA = H'C1
- Increment SAR after transfer.
- Fix DAR after transfer.
- Select normal transfer mode.
- Select word transfer.

CYC0.CRA = UPTIME
- Transfer counter = UPTIME

End
6.10 frstop0 Function

frstop0

PTN0.DTC1.SAR = & pattbl[3]
Set the end address of the output pattern table as transfer source.

PTN0.DTC1.MRA = H'06
- Fix SAR after transfer.
- Fix DAR after transfer.
- Select repeat transfer mode.
- Set the source as repeat area.
- Select byte transfer.

PTN0.CRA = H'0404
- Number of transfers = 4
- Transfer counter = 4

CYC0.DTC1.SAR = uptbl
Set the address of the stop time storage memory as transfer source.

CYC0.DTC1.MRA = H'10
- Select normal transfer mode.
- Select word transfer.
- Fix SAR after transfer.

CYC0.CRA = STOPTIME
- Transfer counter = STOPTIME

End
## Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Mar.09.05</td>
<td></td>
<td></td>
<td>First edition issued</td>
</tr>
</tbody>
</table>
Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.

2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.

3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.

   The information described here may contain technical inaccuracies or typographical errors. Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.

   Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (http://www.renesas.com).

4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.

5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.

6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.

7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.

   Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.

8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.