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April 1st, 2010
Renesas Electronics Corporation

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H8S Family

D/A Conversion

Introduction

Starts up the DMAC by the TPU and performs D/A conversion of data stored in the RAM.

Target Device

H8S/2339

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1. Specifications

1. As shown in figure 1, this sample task starts up the DMACs from ch0 and ch1 of the TPUs to perform D/A conversion of data stored in the RAM.
2. The RAM areas start at address H'FF7C10 and end at address H'FF7C4F.
3. The H8S/2339 runs at about 20 (19.6608)-MHz internal operating frequency.

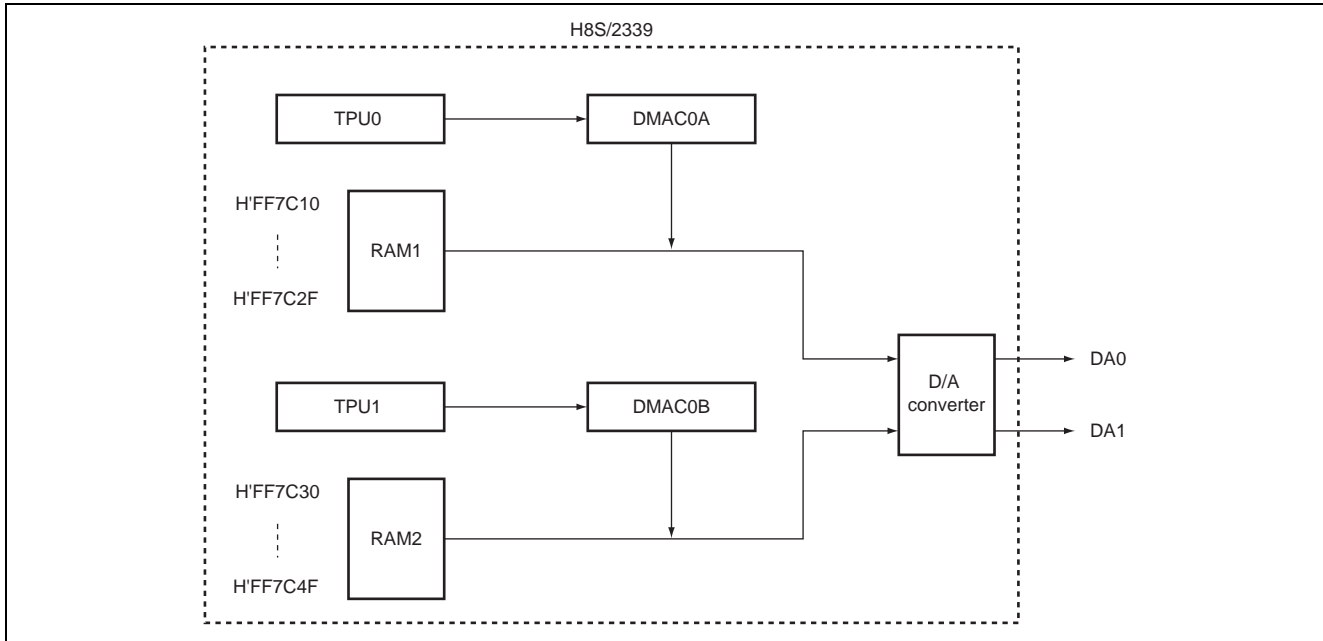


Figure 1 D/A Conversion Block Diagram

2. Description of Functions

- The block diagram of the DMACs, D/A converter, and TPUs to be used by this sample task is shown in figure 2. This sample task uses the H8S/2339 function as follows to perform D/A conversion:

[DMACs]

Start up by a TPU compare match A and transfers data in the data buffer to D/A converter DADR.

[TPUs]

Operate ch0 and ch1 synchronously to start up the DMACs.

Clear the timer counter each time a ch1 compare match A occurs.

[D/A converter]

Starts D/A conversion immediately after the conversion data is written in DADRs and outputs the conversion results after conversion time passes. An analog conversion voltage range can be set, using AVcc as the reference voltage.

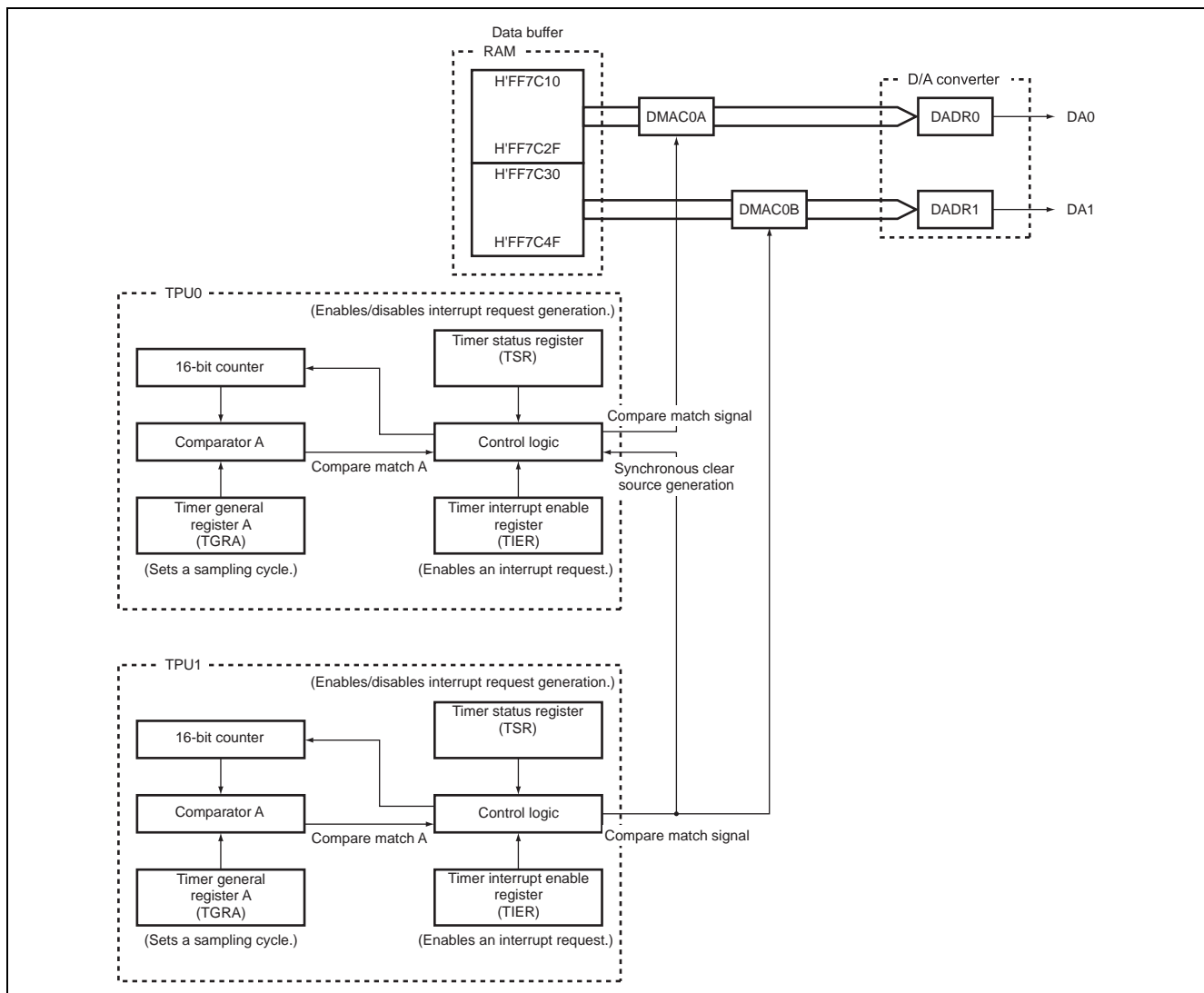


Figure 2 Block Diagram of Analog Output Circuit

3. Principles of Operation

The principles of operations used are shown in figure 3. This sample task performs hardware and software processing of the H8S/2339 as shown in figure 3 to perform D/A conversion.

1. Analog Output

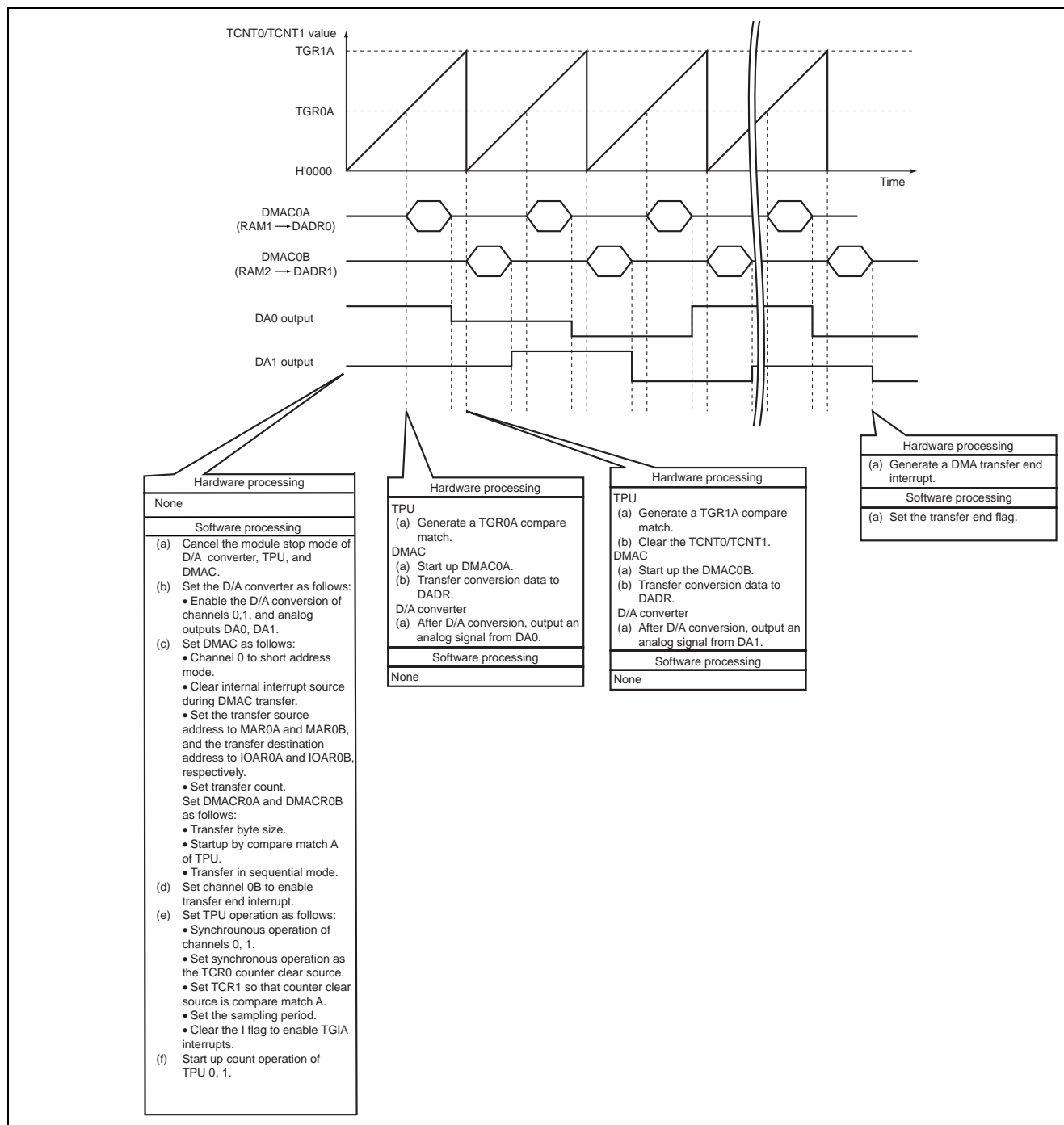


Figure 3 Principles of Operations Used for Analog Output

4. Description of Software

1. Description of Modules

Module Name	Label Name	Function
Main routine	dacvtmn	Performs initial setting of the TPU, DMAC, and D/A converter, and sets the RAM to be used.
D/A conversion end	datrend	Sets the D/A conversion end flag.

2. Description of Argument

Label Name	Function	Data Length	Used in	I/O
trs_end	Indicates end of transfer of data in H'FF7C10 to H'FF7C4F. 1: Data transfer ended 0: Data transfer in progress	unsigned char	D/A conversion end	Input Output

3. Description of Internal Registers Used

Implemented Function	Register Name	Function	
TPU	TGR0A	Sets the sampling cycle of D/A conversion.	
	TIER0	Enables a TGIA interrupt.	
	TCR0	Sets the TPU0 as follows: <ul style="list-style-type: none"> • Synchronous clear • Count by internal clock ϕ 	
	TGR1A	Sets the sampling cycle of D/A conversion.	
	TIER1	Enables a TGIA interrupt.	
	TCR1	Sets the TPU0 as follows: <ul style="list-style-type: none"> • Counter clear by a TGR1A compare match • Count by internal clock ϕ 	
	TSTR	Enables count operation of the TCNT0 and TCNT1.	
	TSYR	Sets channels 0 and 1 to synchronous operation.	
	DMAC	DMABCR	Controls operation of each channel.
		DMACR0A	Sets the DMAC0A as follows: <ul style="list-style-type: none"> • Byte size transfer • Sequential mode • Enables clear of the internal interrupt source during DMA transfer • Enables data transfer
DMACR0B		Sets the DMAC0B as follows: <ul style="list-style-type: none"> • Byte size transfer • Sequential mode • Enables clear of the internal interrupt source during DMA transfer • Enables data transfer and a transfer end interrupt 	
MAR0A		Sets the transfer source address (start address of RAM1)	
MAR0B		Sets the transfer source address (start address of RAM2)	
IOAR0A		Sets the transfer destination address (DADR0).	
IOAR0B		Sets the transfer destination address (DADR1).	
ETCR0A		Sets the transfer count (H'001F).	
ETCR0B		Sets the transfer count (H'001F).	
D/A		DACR0	Sets DACR as follows: <ul style="list-style-type: none"> • Enables D/A conversion of channel 0 and analog output from DA0
	DADR0	Stores data to be converted.	
	DADR1	Stores data to be converted.	
MSTPCR		Cancels the module stop mode.	

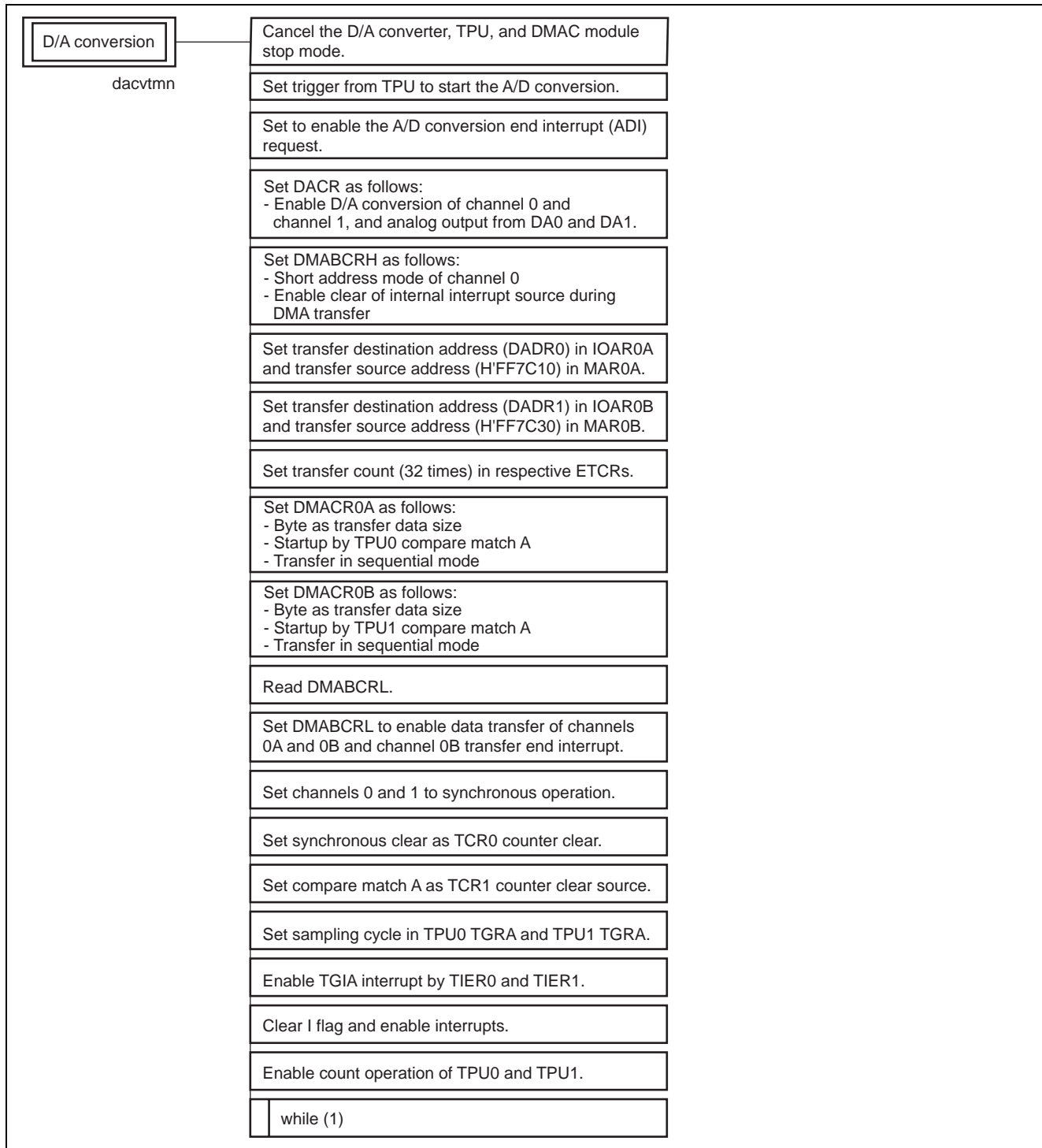
4. RAM Usage

Table below describes RAM usage in this sample task.

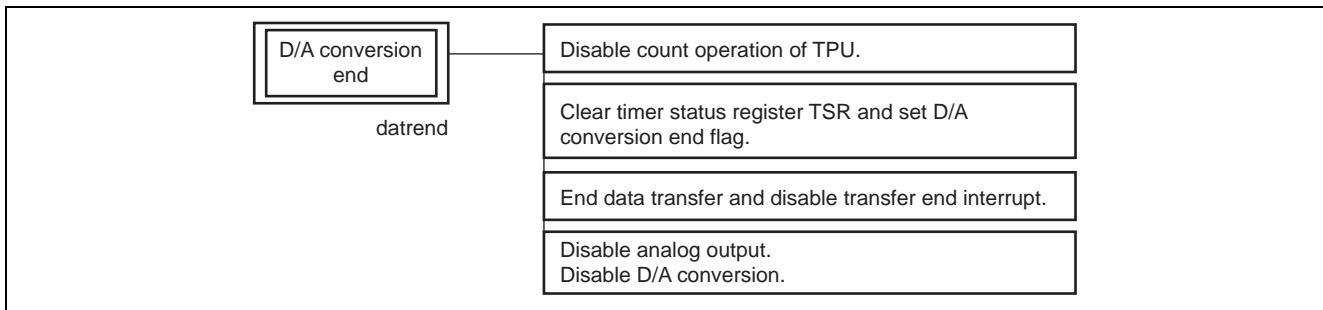
Label Name	Function	Data Length	Data Capacity
da_data1, 2	Stores D/A conversion data.	unsigned char	64 bytes

5. PAD

1. Main Routine



2. D/A Conversion End



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Feb.17.05	—	First edition issued

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