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April 1st, 2010
Renesas Electronics Corporation

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H8S Family
Pulse-Train Output

Introduction
Pulses with duty ratio of 50% is output using the 16-bit counter based on the cyclic data set in the RAM.

Target Device
H8S/2339

Contents

1. Specifications .............................................................................................................. 2
2. Description of Module Usage ................................................................................... 3
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1. Specifications

(1) Outputs a pulse train with a 50% duty cycle as shown in figure 1. The period is set by cycle data in RAM.

(2) When the microcomputer is operating at 19.66 MHz, the cycle of the pulse for output can be set as desired to values between about 101.72 ns and 3.33 ms.

Figure 1 Example of Pulse Output
2. Description of Module Usage

(1) TPU0 is used to output a pulse with duty cycle of 50%.
   (a) A block diagram of TPU0, the timer used in this application, is given in figure 2.
   The following functions of the TPU0 are used:
   • Automatic output of a pulse by hardware with no software intervention (output compare)
   • Clearing of the counter (counter clear) on a compare-match
   • Inversion of the output for every occurrence of a compare match (toggled output)

![Diagram](image-url)

Figure 2  Configuration for Pulse-Train Output
3. **Principles of Operation**

Task operation is depicted in figure 3. The pulses are output through a combination of hardware and software processing by the H8S/2339.

<table>
<thead>
<tr>
<th>Initial setting</th>
<th>Hardware processing</th>
<th>Software processing</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) Takes TPU out of module stop mode</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>(b) Sets the input to TCNT0 as φ and the source of the counter-clearing signal as compare-match A.</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>(c) Sets TPU0 so that its output is toggled on matches of compare-match A.</td>
<td>(a) Detects compare-match A for TPU0</td>
<td>(a) Detects compare-match A for TPU0</td>
</tr>
<tr>
<td>(d) Sets the 1/2-cycle period for the pulse signal in TGR0A</td>
<td>(b) Clears the counter</td>
<td>(b) Clears the counter</td>
</tr>
<tr>
<td>(e) Starts the counter</td>
<td>(c) Outputs a high-level signal from TIOCA0</td>
<td>(c) Outputs a low-level signal from TIOCA0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>In the counter</th>
<th>Hardware processing</th>
<th>Software processing</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) Detects compare-match A for TPU0</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>(b) Clears the counter</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>(c) Outputs a high-level signal from TIOCA0</td>
<td>None</td>
<td>None</td>
</tr>
</tbody>
</table>

**Figure 3  Principle of Pulse-Output Operation**
4. Software Description

(1) Function

<table>
<thead>
<tr>
<th>Function</th>
<th>Label</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>poutmn</td>
<td>Makes initial settings of TPU and RAM</td>
</tr>
</tbody>
</table>

(2) Arguments

<table>
<thead>
<tr>
<th>Label</th>
<th>Description</th>
<th>Data Length</th>
<th>Used in</th>
<th>I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>pul_cyc</td>
<td>Sets the timer value which is equivalent to the pulse cycle. The pulse cycle is obtained by the following expression: Pulse cycle (ns) = Timer value x 2(\phi) period (50.86 ns in operation at 19.66 MHz)</td>
<td>unsigned short</td>
<td>Main routine</td>
<td>Input</td>
</tr>
</tbody>
</table>

(3) Internal Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSTR</td>
<td>Enables and disables the timer counter</td>
<td>Main routine</td>
</tr>
<tr>
<td>TCR0</td>
<td>Selects the clock for input to TCNT and the source of the counter-clearing signal</td>
<td>Main routine</td>
</tr>
<tr>
<td>TIOR0</td>
<td>Configures output-pulse behavior in response to compare-match A</td>
<td>Main routine</td>
</tr>
<tr>
<td>TGR0A</td>
<td>Sets the 1/2-cycle period for the output pulse</td>
<td>Main routine</td>
</tr>
<tr>
<td>MSTPCR</td>
<td>Clears the TPU module-stopped mode</td>
<td>Main routine</td>
</tr>
</tbody>
</table>

(4) RAM Usage

Internal RAM other than that for argument-storage is not used.
5. PAD

(1) Main routine

```c
while (1) {
    Pulse output
    poutmin
    Clear the TPU module-stopped mode.
    Set the TCNT input clock and counter-clearing source in TCR0.
    Set the TIOR to select output toggling by compare-match A.
    Set the value that corresponds to half of the pulse-train cycle in TGR0A.
    Start counting by channel 0.
}
```
<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Feb.17.05</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>
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