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April 1st, 2010
Renesas Electronics Corporation

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H8S Family
One-Shot Pulse Output

Introduction
Outputs a one-shot pulse, synchronizing with a falling edge of an external signal. The delay time from the falling edge and pulse width can be varied.

Target Device
H8S/2339

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1. Specifications

1. As shown in figure 1, this function outputs a one-shot pulse, synchronizing with the falling edge of the external signal.

2. The delay time from the falling edge of the external signal and pulse width can be changed within the following ranges. Set the reference pulse cycle shorter than the cycle set in TCNT0.

   1 \mu s \leq \text{delay time} < \text{reference pulse cycle} - \text{pulse width}

   50.86 \text{ ns} \leq \text{pulse width} < \text{reference pulse cycle} - \text{delay time}

![Figure 1 One-Shot Pulse Output](image-url)
2. Description of Functions

1. This sample task outputs a one-shot pulse by using DMAC0A, DMAC0B, and TPU0.
   A. The block diagram of internal functions used in this sample task is shown in figure 2.

   In this sample task, a one-shot pulse is output by using the following TPU and DMAC functions:

   [TPU]
   - Function that transfers the buffer register contents to a timer general register at occurrence of compare match. (Buffer operation)
   - Function that can set an output/input capture register for each register.
   - Function that can clear a counter by input capture.

   [DMAC]
   - Function that starts up DMAC at occurrence of TPU input capture.

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**Figure 2  Block Diagram of One-Shot Pulse Output**
3. Principles of Operation

The principles of operations used are shown in figure 3. As shown in figure 3, a one-shot pulse is output by H8S/2339 hardware and software processing.

Figure 3  Principles of Operations Used of One-Shot Pulse Output
4. Description of Software

1. Description of Modules

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Label Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>ONEMN</td>
<td>Sets the delay time and pulse width in TGR0B and TGR0D, and a one-shot pulse reset value to TGR0C to output a one-shot pulse.</td>
</tr>
<tr>
<td>Pulse output disabled</td>
<td>POUTDLE</td>
<td>Disables pulse output.</td>
</tr>
</tbody>
</table>

2. Description of Arguments

<table>
<thead>
<tr>
<th>Label Name</th>
<th>Function</th>
<th>Data Length</th>
<th>Used in</th>
<th>I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>set_dly</td>
<td>Sets a timer value that governs the delay time of one-shot pulse. The delay time is obtained by the following expression: Delay time (ns) = timer value × φ cycle (50.86 ns during 19.66-MHz operation)</td>
<td>unsigned short</td>
<td>Main routine</td>
<td>Input</td>
</tr>
<tr>
<td>one_rst</td>
<td>Sets a timer value that governs the reset timing of one-shot pulse. The reset timing is obtained by the following expression: Pulse reset timing (ns) = timer value × φ cycle (50.86 ns during 19.66-MHz operation)</td>
<td>unsigned short</td>
<td>Main routine</td>
<td>Input</td>
</tr>
<tr>
<td>io_cntr</td>
<td>Sets one-shot pulse output enabled data. (A falling edge is set as the input capture A detection edge and compare match B is toggled during output.)</td>
<td>unsigned char</td>
<td>Main routine</td>
<td>Output</td>
</tr>
</tbody>
</table>
3. Description of Internal Registers Used

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Function</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPU</td>
<td>TSTR Selects operation/stop of the timer counter.</td>
<td>Main routine</td>
</tr>
<tr>
<td>TPU0</td>
<td>TMDR Sets TGR0B and TGR0D to buffer operation.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TCR0 Sets a clock to be input to TCNT and a counter clearing source.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TIOR0 Detects a falling edge of an input pulse.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Sets a level to be output from TIOCB0 at occurrence of compare match B.</td>
<td>Pulse output disabled</td>
</tr>
<tr>
<td></td>
<td>TIER0 Enables an interrupt by TGI0C.</td>
<td>Main routine/ pulse output disabled</td>
</tr>
<tr>
<td>TSR0</td>
<td>Indicates occurrence of compare match by TGR0B.</td>
<td>Main routine</td>
</tr>
<tr>
<td>TGR0B</td>
<td>Sets the delay time of one-shot pulse.</td>
<td></td>
</tr>
<tr>
<td>TGR0C</td>
<td>Sets a pulse output disabled timing value of one-shot pulse.</td>
<td></td>
</tr>
<tr>
<td>TGR0D</td>
<td>Sets a reset timing value of one-shot pulse.</td>
<td></td>
</tr>
<tr>
<td>DMAC</td>
<td>DMABCR0 Set the operation of each DMAC channel.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>DMACR0A</td>
<td></td>
</tr>
<tr>
<td></td>
<td>DMACR0B</td>
<td></td>
</tr>
<tr>
<td>MAR0A</td>
<td>Set the address of data to be transferred to each register.</td>
<td></td>
</tr>
<tr>
<td>MAR0B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IOAR0A</td>
<td>Set the transfer destination register address of each channel.</td>
<td></td>
</tr>
<tr>
<td>IOAR0B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ETCR0A</td>
<td>Set the transfer count of each channel.</td>
<td></td>
</tr>
<tr>
<td>ETCR0B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MSTPCR</td>
<td>Cancel the TPU and DMAC module stop mode.</td>
<td></td>
</tr>
</tbody>
</table>

4. RAM Usage

<table>
<thead>
<tr>
<th>Label</th>
<th>Set Value of the Sample Task</th>
</tr>
</thead>
<tbody>
<tr>
<td>io_cntr</td>
<td>H’39</td>
</tr>
</tbody>
</table>
5. PAD

1. Main Routine

```
Main routine

ONEMN

Cancel TPU and DMAC module stop mode.
Set TCR0 and set input capture A as counter clearing source.
Set TMDR0 and set TGR0B and TGR0D to buffer operation.
Set compare-match output disabled timing of one-shot pulse in TGR0C.
Set reset timing of one-shot pulse (one_rst) in TGR0D.
Set TIOR0 so that input capture occurs on the falling edge of the TIOCA0 signal.
Set TIOCB0 output enabled data in (io_cntr).
Set address setting one-shot pulse delay time (set_dly) in MAR0A as transfer source address.
Set the address setting TPU0 compare-match output (io_cntr) in MAR0B as transfer source address.
Set TGR0B address in IOAR0A as transfer destination address.
Set TIOR0 address in IOAR0B as transfer destination address.
Set transfer count in ETCR0A and ETCR0B respectively.
Set DMAC0A operation according to DMACR0A.
  - TPU0 input capture A as startup source
  - Repeat mode
  - 1-word data transfer
Set DMAC0B operation according to DMACR0B.
  - TPU0 input capture A as startup source
  - Repeat mode
  - 1-byte data transfer
Read DMACR0L.
Set DMAC0A and DMAC0B to transfer enabled according to DMACR0H/DMACR0L.
Set interrupt enabled, DMAC startup source, in TIER0.
Set TIER0 to enable interrupts by TGFA and TGFC.
Clear I flag to enable interrupts.
Start TPU0 counter operation.

while (1)
```
2. Pulse Output Disabled

<table>
<thead>
<tr>
<th>Pulse output disabled</th>
<th>Clear interrupt request flag (TGFC).</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Set TIOR0 and disables TGR0B compare-match output.</td>
</tr>
</tbody>
</table>
## Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Feb.17.05</td>
<td>—</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>
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