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April 1\(^{st}\), 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation ([http://www.renesas.com](http://www.renesas.com))

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H8S Family
Normal Mode Data Transfer by the EXDMAC

Introduction
Data transfer is performed by the EXDMAC in normal transfer mode.

Target Device
H8S/2377

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1. Specifications ........................................................................................................................................... 2
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1. Specifications

- The EXDMAC is activated by software and transfers 1024 bytes of data in flash memory to SRAM.
- DMA transfer is configured as shown in table 1.
- Flash memory is allocated to CS1 and SRAM is allocated to CS2.

![Figure 1 Transfer by EXDMAC](image)

Table 1 Configuration of EXDMAC

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMA transfer request</td>
<td>Auto-request mode</td>
</tr>
<tr>
<td>Bus mode</td>
<td>Cycle steal mode</td>
</tr>
<tr>
<td>Transfer mode</td>
<td>Normal transfer mode</td>
</tr>
<tr>
<td>Address mode</td>
<td>Dual-address mode</td>
</tr>
<tr>
<td>Transfer size</td>
<td>One byte</td>
</tr>
</tbody>
</table>
2. Applicable Conditions

Table 2  Applicable Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating frequency</td>
<td>Input clock: 19.6608 MHz</td>
</tr>
<tr>
<td></td>
<td>System clock (Iφ): 19.6608 MHz</td>
</tr>
<tr>
<td></td>
<td>Peripheral module clock (Pφ): 19.6608 MHz</td>
</tr>
<tr>
<td></td>
<td>External bus clock (Bφ): 19.6608 MHz</td>
</tr>
<tr>
<td>Operating mode</td>
<td>Mode 4 (MD2 = 1, MD1 = 0, MD0 = 0)</td>
</tr>
<tr>
<td>Development tool</td>
<td>HEW: version 3.01.02</td>
</tr>
<tr>
<td>C/C++ compiler</td>
<td>H8S, H8/300 Series C/C++ Compiler: version 6.00.02</td>
</tr>
<tr>
<td></td>
<td>(from Renesas Technology Corp.)</td>
</tr>
<tr>
<td>Compile options</td>
<td>-cpu = 2000a:24, -code = machinecode, -optimize=1, -regparam = 3</td>
</tr>
<tr>
<td></td>
<td>-speed = (register, shift, struct, expression)</td>
</tr>
</tbody>
</table>

Table 3  Section Settings

<table>
<thead>
<tr>
<th>Address</th>
<th>Section Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>H'0000000</td>
<td>CV1</td>
<td>Reset vector</td>
</tr>
<tr>
<td>H'0010000</td>
<td>P</td>
<td>Program area</td>
</tr>
</tbody>
</table>
3. Description of Functions

Figure 2 shows the block diagram of the EXDMAC, which is described below.

- The EXDMA source address register 2 (EDSAR_2)
  EDSAR_2 is a 32-bit readable/writable registers that specifies the transfer source address. It has an address update function which allows the register contents to be updated to the next source address each time transfer processing is performed.

- The EXDMA destination address register 2 (EDDAR_2)
  EDDAR_2 is a 32-bit readable/writable registers that specifies the transfer destination address. It has an address update function which allows the register contents to be updated to the next destination address each time transfer processing is performed.

- The EXDMA transfer count register 2 (EDTCR_2)
  EDTCR_2 is loaded with the size of data to be transferred (total transfer size). Each time data is transferred, the value of this register is decremented according to the access size of the transferred data. In this sample task, EDTCR_2 is loaded with H'00000400, which corresponds to 1024 bytes, and the data access size is set to one byte. During EXDMA operation, EDTCR_2 value is decremented by 1, indicating the number of remaining transfers.

- The EXDMA mode control register 2 (EDMDR_2)
  EDMDR_2 controls the operation of the EXDMAC.

- The EXDMA address control register 2 (EDACR_2)
  EDACR_2 sets the operating mode, transfer method, etc.

![Figure 2 Block Diagram of EXDMAC](image-url)
4. **Description of Operation**

The operation of normal transfer in dual-address mode is outlined below.

![Figure 3 Example of Normal Transfer Operation](image)

- **PΦ**: Hardware processing
  - Activate EXDMAC channel 2 to start transfer.
- **Address bus**: Hardware processing
  - Set the EDA bit of the EDMDR register to 1 to activate the EXDMAC.
- **RD**: Software processing
  - Drive ETEND low when the last data is transferred.
- **WD**: Software processing
  - Clear the EDA bit of the EDMDR register to 0 after the end of transfer.
- **EDA**: None
  - Software processing
  - None
- **ETEND**: None
  - None
5. Description of Software

5.1 List of Functions

Table 4 List of Functions

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>init</td>
<td>Initialization routine&lt;br&gt;Sets CCR, configures clocks, cancels module stop modes, and calls the BscInit and main functions.</td>
</tr>
<tr>
<td>BscInit</td>
<td>BSC setting&lt;br&gt;Configures the bus.</td>
</tr>
<tr>
<td>main</td>
<td>Main routine&lt;br&gt;Configures transfer functions and starts transfer.</td>
</tr>
</tbody>
</table>

![Hierarchy of Functions](image)

5.2 Arguments

No argument is used in this sample task.

5.3 Internal registers

This section describes the internal registers used in this sample task.

- **System Clock Control Register (SCKCR)**<br>Address: H'FFFF3B

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>SCK2</td>
<td>0</td>
<td>System clock select 2, 1, 0</td>
</tr>
<tr>
<td>1</td>
<td>SCK1</td>
<td>0</td>
<td>000: Division ratio is 1/1.</td>
</tr>
<tr>
<td>0</td>
<td>SCK0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

- **PLL Control Register (PLLCR)**<br>Address: H'FFFF45

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>STC1</td>
<td>0</td>
<td>Frequency multiplication factor setting</td>
</tr>
<tr>
<td>0</td>
<td>STC0</td>
<td>0</td>
<td>00: Frequency multiplication factor of the PLL circuit is ×1.</td>
</tr>
<tr>
<td>Bit</td>
<td>Bit Name</td>
<td>Setting</td>
<td>Function</td>
</tr>
<tr>
<td>-----</td>
<td>----------</td>
<td>---------</td>
<td>----------</td>
</tr>
</tbody>
</table>
| 15  | ACSE     | 0       | All-module-clocks-stop mode enable  
|     |          |         | 0: Disables all-module-clocks-stop mode.  
|     |          |         | 1: Enables all-module-clocks-stop mode.  |
| 14  | MSTP14   | 0       | EXDMA controller (EXDMA)  
|     |          |         | 0: Cancels module stop mode.  
|     |          |         | 1: Sets module stop mode.  |
| 13  | MSTP13   | 0       | DMA controller (DMAC)  
|     |          |         | 0: Cancels module stop mode.  
|     |          |         | 1: Sets module stop mode.  |
| 12  | MSTP12   | 0       | Data transfer controller (DTC)  
|     |          |         | 0: Cancels module stop mode.  
|     |          |         | 1: Sets module stop mode.  |
| 11  | MSTP11   | 0       | 16-bit timer pulse unit (TPU)  
|     |          |         | 0: Cancels module stop mode.  
|     |          |         | 1: Sets module stop mode.  |
| 10  | MSTP10   | 0       | Programmable pulse generator (PPG)  
|     |          |         | 0: Cancels module stop mode.  
|     |          |         | 1: Sets module stop mode.  |
| 9   | MSTP9    | 0       | D/A converter (channels 0, 1)  
|     |          |         | 0: Cancels module stop mode.  
|     |          |         | 1: Sets module stop mode.  |
| 8   | MSTP8    | 0       | D/A converter (channels 2, 3)  
|     |          |         | 0: Cancels module stop mode.  
|     |          |         | 1: Sets module stop mode.  |
| 7   | MSTP7    | 0       | D/A converter (channels 4, 5)  
|     |          |         | 0: Cancels module stop mode.  
|     |          |         | 1: Sets module stop mode.  |
| 6   | MSTP6    | 0       | A/D converter  
|     |          |         | 0: Cancels module stop mode.  
|     |          |         | 1: Sets module stop mode.  |
| 5   | MSTP5    | 0       | Serial communication interface 4 (SCI_4)  
|     |          |         | 0: Cancels module stop mode.  
|     |          |         | 1: Sets module stop mode.  |
| 4   | MSTP4    | 0       | Serial communication interface 3 (SCI_3)  
|     |          |         | 0: Cancels module stop mode.  
|     |          |         | 1: Sets module stop mode.  |
| 3   | MSTP3    | 0       | Serial communication interface 2 (SCI_2)  
|     |          |         | 0: Cancels module stop mode.  
|     |          |         | 1: Sets module stop mode.  |
| 2   | MSTP2    | 0       | Serial communication interface 1 (SCI_1)  
|     |          |         | 0: Cancels module stop mode.  
|     |          |         | 1: Sets module stop mode.  |
| 1   | MSTP1    | 0       | Serial communication interface 0 (SCI_0)  
|     |          |         | 0: Cancels module stop mode.  
|     |          |         | 1: Sets module stop mode.  |
| 0   | MSTP0    | 0       | 8-bit timer (TMR)  
|     |          |         | 0: Cancels module stop mode.  
|     |          |         | 1: Sets module stop mode.  |
### Extension Module Stop Control Register H, L (EXMSTPCRH, EXMSTPCRL)

Address: H'FFFF42, H'FFFF43

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>MSTP20</td>
<td>0</td>
<td>I^2C bus interface 2_1 (IIC2_1)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Cancels module stop mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Sets module stop mode.</td>
</tr>
<tr>
<td>3</td>
<td>MSTP19</td>
<td>0</td>
<td>I^2C bus interface 2_0 (IIC2_0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Cancels module stop mode.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Sets module stop mode.</td>
</tr>
</tbody>
</table>

### System Control Register (SYSCR)

Address: H'FFFF3D

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>RAME</td>
<td>1</td>
<td>RAM enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disables the on-chip RAM.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enables the on-chip RAM.</td>
</tr>
</tbody>
</table>

### Port Function Control Register 0 (PFCR0)

Address: H'FFFE32

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>CS7E</td>
<td>1</td>
<td>CS7 to CS0 enable</td>
</tr>
<tr>
<td>6</td>
<td>CS6E</td>
<td>1</td>
<td>Each bit of this register enables/disables the corresponding CSn output.</td>
</tr>
<tr>
<td>5</td>
<td>CS5E</td>
<td>1</td>
<td>0: The pin functions as an I/O port pin.</td>
</tr>
<tr>
<td>4</td>
<td>CS4E</td>
<td>1</td>
<td>1: The pin functions as the CSn output pin. (n = 7 to 0)</td>
</tr>
<tr>
<td>3</td>
<td>CS3E</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>CS2E</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>CS1E</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>CS0E</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

### Port Function Control Register 1 (PFCR1)

Address: H'FFFE33

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>A23E</td>
<td>1</td>
<td>Address A23 to A16 enable</td>
</tr>
<tr>
<td>6</td>
<td>A22E</td>
<td>1</td>
<td>Each bit of this register enables/disables the corresponding address output (A23 to A16).</td>
</tr>
<tr>
<td>5</td>
<td>A21E</td>
<td>1</td>
<td>0: Outputs DR when PAnDDR = 1. (n = 7 to 0)</td>
</tr>
<tr>
<td>4</td>
<td>A20E</td>
<td>1</td>
<td>1: Outputs Amm when PAnDDR = 1. (n = 7 to 0, mm = 23 to 16)</td>
</tr>
<tr>
<td>3</td>
<td>A19E</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>A18E</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>A17E</td>
<td>1</td>
<td>In this sample task, PFCR1 is set to H'FF to enable address outputs</td>
</tr>
<tr>
<td>0</td>
<td>A16E</td>
<td>1</td>
<td>A23 to A16.</td>
</tr>
</tbody>
</table>
- Port Function Control Register 2 (PFCR2)  
  Address: H'FFFE34

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Function</th>
</tr>
</thead>
</table>
| 3   | ASOE     | 1       | AS output enable  
  0: PF6 functions as an I/O port pin.  
  1: PF6 functions as the AS output pin. |
| 2   | LWROE    | 1       | LWR output enable  
  0: PF3 functions as an I/O port pin.  
  1: PF3 functions as the LWR output pin. |

- Port A data direction register (PADDR)  
  Address: H'FFFE29  
  Function: Sets the PA7 to PA0 pins to function as address output pins.  
  Setting: H'FF

- Port B data direction register (PBDDR)  
  Address: H'FFFE2A  
  Function: Sets the PB7 to PB0 pins to function as address output pins.  
  Setting: H'FF

- Port C data direction register (PCDDR)  
  Address: H'FFFE2B  
  Function: Sets the PC7 to PC0 pins to function as address output pins.  
  Setting: H'FF

- Port F data direction register (PFDDR)  
  Address: H'FFFE2E  
  Function: Sets the PF7 pin to output φ, and PF6 to PF0 to function as input pins.  
  Setting: H'80

- Port G data direction register (PGDDR)  
  Address: H'FFFE2F  
  Function: Sets the PG3 to PG0 pins to function as the CS3 to CS0 input pins.  
  Setting: H'0F

- Port H data direction register (PHDDR)  
  Address: H''FFFF74  
  Function: Sets the PH3 to PH0 pins to function as the CS7 to CS4 input pins.  
  Setting: H'0F

- Bus width control register (ABWCR)  
  Address: H'FFFE0  
  Function: Designates areas 7 to 3, 1, 0 as 16-bit access space and area 2 as 8-bit access space.  
  Setting: H'04

- Access state control register (ASTCR)  
  Address: H'FFFC1  
  Function: Designates areas 7 to 0 as 3-state access space  
  Setting: H'FF

- Wait control register A (WTCRA)  
  Address: H'FFFE2  
  Function: Selects the number of program wait states to be inserted: 7 states for areas 7 and 6, and 3 states for areas 5 and 4.  
  Setting: H'7733

- Wait control register B (WTCRB)  
  Address: H'FFFC4  
  Function: Selects the number of program wait states to be inserted: 1 state for areas 3 and 2, and 2 states for areas 1 and 0.  
  Setting: H'1122
- **Read strobe timing control register (RDNCR)**
  
  **Function:** Sets so that, in read access to areas 7 to 0, RD is negated at the end of the read cycle.
  
  **Setting:** H'00

- **Bus control register (BCR)**

  **Function:**

  **Bit** | **Bit Name** | **Setting** | **Function**
  -- | -- | -- | --
  15 | BRLE | 0 | External bus release enable
  | | | 0: Disables external bus release.
  | | | 1: Enables external bus release.
  12 | IDLC | 1 | Select number of states in idle cycle
  | | | Specifies the number of states in the idle cycles set by ICIS2, ICIS1 and ICIS0
  | | | 0: One state.
  | | | 1: Two states.
  11 | ICIS1 | 1 | Idle cycle insertion 1
  | | | When consecutive external read cycles are executed in different areas, an idle cycle can be inserted between the bus cycles.
  | | | 0: Idle cycle not inserted
  | | | 1: Idle cycle inserted
  10 | ICIS0 | 1 | Idle cycle insertion 0
  | | | When an external read cycle and external write cycle are performed consecutively, an idle cycle can be inserted between the bus cycles.
  | | | 0: Idle cycle not inserted
  | | | 1: Idle cycle inserted
  8 | WAITE | 1 | WAIT pin enable
  | | | 0: Disables wait insertion by the WAIT pin. The WAIT pin can be used as an I/O port pin.
  | | | 1: Enables wait insertion by the WAIT pin.
  2 | ICIS2 | 0 | Idle cycle insertion 2
  | | | When an external write cycle and external read cycle are performed consecutively, an idle cycle can be inserted between the bus cycles.
  | | | 0: Idle cycle not inserted
  | | | 1: Idle cycle inserted
- **EXDMA source address register 2 (EDSAR_2)**
  - Function: Sets the transfer source address.
  - Setting: H'00200000
  - Address: H'FFFDE0

- **EXDMA destination address register 2 (EDDAR_2)**
  - Function: Sets the transfer destination address.
  - Setting: H'00400000
  - Address: H'FFFDE4

- **EXDMA transfer count register 2 (EDTCR_2)**
  - Function: Sets the transfer source address.
  - Setting: H'00200000
  - Address: H'FFFDE8

- **EXDMA mode control register 2 (EDMDR_2)**
  - Address: H'FFFDEC

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>EDA</td>
<td>0</td>
<td>EXDMA active</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Disables data transfer.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Enables data transfer.</td>
</tr>
<tr>
<td>10</td>
<td>AMS</td>
<td>0</td>
<td>Address mode select</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: Dual-address mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: Single-address mode</td>
</tr>
<tr>
<td>9</td>
<td>MDS1</td>
<td>0</td>
<td>Mode select 1, 0</td>
</tr>
<tr>
<td>8</td>
<td>MDS0</td>
<td>0</td>
<td>00: Auto-request, cycle steal mode, normal transfer mode</td>
</tr>
<tr>
<td>3</td>
<td>DTSIZE</td>
<td>0</td>
<td>Data transmit size</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0: One byte</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1: One word</td>
</tr>
</tbody>
</table>

- **EXDMA address control register 2 (EDACR_2)**
  - Address: H'FFFDEE

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Name</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15</td>
<td>SAT1</td>
<td>1</td>
<td>Source address update mode</td>
</tr>
<tr>
<td>14</td>
<td>SAT0</td>
<td>0</td>
<td>10: Source address is incremented.</td>
</tr>
<tr>
<td>7</td>
<td>DAT1</td>
<td>1</td>
<td>Destination address update mode</td>
</tr>
<tr>
<td>6</td>
<td>DAT0</td>
<td>0</td>
<td>10: Destination address is incremented.</td>
</tr>
</tbody>
</table>

**5.4 RAM Usage**

This sample task does not use RAM.
6. Flowchart

6.1 init Function

```
init

H'80 \rightarrow CCR
Initialize CCR to disable interrupts.

H'00 \rightarrow SCKCR
System clock division ratio = 1/1

H'00 \rightarrow PLLCR
Frequency multiplication factor of the PLL circuit = \times 1

H'00 \rightarrow MSTPCRH
H'00 \rightarrow MSTPCRL
H'FF \rightarrow EXMSTPCRH
H'E5 \rightarrow EXMSTPCRH
Cancel module stop mode of all the modules.

BscInit
Initialization of the bus

main
```

---

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6.2 Bsclnit Function

- **Bsclnit**
  - (SYSCR U H'01) → SYSCR
    - Enable the on-chip RAM.
  - H'FF → PFCR0
    - Enable CS0 to CS7 pin outputs.
  - H'FF → PFCR1
    - Enable address outputs 23 to 16.
  - H'0F → PGDDR
    - Set the PG3 to PG0 pins as the CS3 to CS0 pins.
  - H'0F → PHDDR
    - Set the PG3 to PG0 pins as the CS7 to CS4 pins.
  - H'04 → ABWCR
    - Areas 7 to 3, 1, 0: 16-bit access space
    - Area 2: 8-bit access space
  - H'0E → PFCR2
    - Enable output of AS, LWR, and OE.
  - H'00 → RDNCR
    - In read access to areas 7 to 0, RD is negated at the end of the read cycle.
  - H'FF → ASTCR
    - Areas 7 to 0: 3-state access space
  - H'77 → WTCRAH, H'33 → WTCRAL
  - H'11 → WTCRBH, H'22 → WTCRBL
    - Set the number of program wait states.
    - Area 7: 7 states
    - Area 6: 7 states
    - Area 5: 3 states
    - Area 4: 3 states
    - Area 3: 1 state
    - Area 2: 1 state
    - Area 1: 2 states
    - Area 0: 2 states
  - H'1D00 → BCR
    - Disable bus release.
    - Enable wait insertion by the WAIT pin.

**Diagram**

- Start: H'00
- End: H'FF

- Area 7: 7 states
- Area 6: 7 states
- Area 5: 3 states
- Area 4: 3 states
- Area 3: 1 state
- Area 2: 1 state
- Area 1: 2 states
- Area 0: 2 states
### 6.3 main Function

```plaintext
main

tmp = EMDR_2
EDMDR_2 = H'0000
- Disable transfer.
- Dual-address mode
- Auto request
- Cycle steal mode
- Normal transfer
- Byte-size transfer

EDSAR_2 = H'200000
Set the transfer source address to H'200000 (CS1 flash memory).

EDDAR_2 = H'400000
Set the transfer destination address to H'400000 (CS2 SRAM).

EDTCR_2 = H'00000400
Set the transfer data size to H'00000400 (1024 bytes).

EDACR_2 = H'8080
Set so that the source and destination addresses are incremented.

EDA_2 = 1
Start transfer.

EDA_2 ≠ 1 ?
Transfer end?
== 0
Transfer end
== 1
Transfer in progress

End
```
### Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Mar.09.05</td>
<td>—</td>
<td>First edition issued</td>
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</table>
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