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April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

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H8S Family
Long-Period Pulse Output by Cascading the TPU Channels

Introduction
The two channels of 16-bit timer counters of the 16-bit timer pulse unit (TPU) are cascaded to function as a 32-bit timer counter. The resulting 32-bit timer counter outputs long-period pulses with a 0 to 100% variable duty cycle.

Target Device
H8S/2339

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1. Specifications

- Two channels of 16-bit counters are cascaded to function as a 32-bit counter. The resulting counter outputs long-period pulses with a variable duty cycle, which is controlled by varying the high pulse width as shown in figure 1.
- The duty cycle can be set in the range from 0 to 100%, with a resolution of \( \frac{1}{65536} \).
- In 20 MHz (19.6608 MHz) operation, the pulse period can be set in the range from approximately 6.66 ms to 218.23 s in 3.33-ms units.

![Figure 1: Example of Long-Period Pulse Output by Cascaded TPU Channels](image)

2. Applicable Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating frequency</td>
<td>Input clock: 19.6608 MHz&lt;br&gt;System clock: 19.6608 MHz&lt;br&gt;Peripheral module clock: 19.6608 MHz&lt;br&gt;Bus master clock: 19.6608 MHz</td>
</tr>
<tr>
<td>Operating mode</td>
<td>Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)</td>
</tr>
<tr>
<td>Development tool</td>
<td>HEW Version 3.01 (release1)</td>
</tr>
<tr>
<td>C/C++ compiler</td>
<td>H8S, H8/300 SERIES C/C++ Compiler Version 6.0.00.005&lt;br&gt;(from Renesas Technology Corp.)</td>
</tr>
<tr>
<td>Compile option</td>
<td>-cpu = 2000a:24, -code = machinecode, -optimize = 1</td>
</tr>
</tbody>
</table>
3. Description of Functions

Figure 2 shows a block diagram of the 16-bit timer pulse unit (TPU), and the following describes the registers of the TPU.

- **Timer Control Register (TCR0)**
  TCR sets the clearing condition and clock source of the timer counter, TCNT, for each channel.

- **Timer Mode Register (TMDR0)**
  TMDR sets the operating mode, normal operation or buffer operation, for each channel.

- **Timer I/O Control Registers (TIOR0H and TIOR0L)**
  TIOR controls output signals by setting the initial output value and output value in compare-match/input-capture operation for each TGR.

- **Timer Interrupt Enable Register (TIER0)**
  TIER enables or disables interrupts for each channel.

- **Timer Status Register (TSR0)**
  TSR indicates the statuses for each channel.

- **Timer Counter (TCNT0)**
  TCNT is a 16-bit counter that can be read or written to. Access to this counter must be in 16-bit units.

- **Timer General Registers (four registers from TGR0A to TGR0D)**
  TGR0A to TGR0D are 16-bit readable/writable registers that are used for output compare or input capture. Access to these registers must be in 16-bit units.

- **Timer Start Register (TSTR)**
  TSTR selects to start or stop the operation of TCNTs for channels 0 to 5.

Note: The register names with "0" in the above description are channel 0 registers. Each channel has a set of such registers.
**Figure 2  Block Diagram of TPU**
4. Description of Operation

Figure 3 illustrates the operation of this sample task. Long-period pulses are output through the hardware and software processing shown in the figure.

**Figure 3   Operation of Long-Period Pulse Output**

<table>
<thead>
<tr>
<th>Counter value of TPU1</th>
<th>Immediately after a reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>TGR1B</td>
<td></td>
</tr>
<tr>
<td>TGR1A</td>
<td></td>
</tr>
<tr>
<td>H'0000</td>
<td></td>
</tr>
<tr>
<td>TCNT2 overflow</td>
<td></td>
</tr>
<tr>
<td>Pulse output (TIOCA1)</td>
<td></td>
</tr>
</tbody>
</table>

**Hardware processing**

- None

**Software processing**

- Initial settings
  - (a) Select φ as the counter clock for TPU2 and set so that TPU1 counter is incremented on each TPU2 overflow.
  - (b) Set TPU1 to be cleared on compare-match B.
  - (c) Set TPU1 in PWM mode.
  - (d) Set so that a high level is output on compare-match with TGR1A and a high level is output on compare-match with TGR1B.
  - (e) Set the low pulse width in TGR1A and the pulse period in TGR1B.
  - (f) Start counting.

**Hardware processing**

- (a) Generate TPU1 compare-match A.
- (b) Output a high level from TIOCA1.

**Software processing**

- None

- (a) Generate TPU1 compare-match B.
- (b) Clear the counter.
- (c) Output a low level from TIOCA1.

**Software processing**

- None
5. Description of Software

5.1 Module

Table 2 describes the module of this sample task.

Table 2 Description of Module

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Label Name</th>
<th>Functions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>tpucasm</td>
<td>Outputs long-period pulses by cascading the TPU1 and TPU2 counters to form a 32-bit counter.</td>
</tr>
</tbody>
</table>

5.2 Arguments

Table 3 describes the arguments used in this sample task.

Table 3 Description of Arguments

<table>
<thead>
<tr>
<th>Label</th>
<th>Description</th>
<th>Data Length</th>
<th>Used in</th>
<th>I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>lpul_wid</td>
<td>Sets the timer value that determines the low-level width of the output pulse. Low pulse width (ms) = ((\text{timer value} + 1) \times (65535 + 1) \times \text{clock } \phi \text{ period}) (Clock (\phi) period is 50.86 ns when the operating frequency is 19.6608 MHz)</td>
<td>1 word</td>
<td>Main routine</td>
<td>Input</td>
</tr>
<tr>
<td>lpul_cyc</td>
<td>Sets the timer value that determines the period of the output pulse. Pulse period (ms) = ((\text{timer value} + 1) \times (65535 + 1) \times \text{clock } \phi \text{ period}) (Clock (\phi) period is 50.86 ns when the operating frequency is 19.6608 MHz)</td>
<td>1 word</td>
<td>Main routine</td>
<td>Input</td>
</tr>
</tbody>
</table>
5.3 Internal Registers

The internal registers used in this sample task are described in table 4.

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Function</th>
<th>Address</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSR1 TCFD</td>
<td>Timer Status Register (Count Direction Flag)</td>
<td>H'FFFFE5</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>TCFD = 0 indicates that TCNT is a down counter.</td>
<td>Bit 7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TCFD = 1 indicates that TCNT is an up counter.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TCFU</td>
<td>Timer Status Register (Underflow Flag)</td>
<td>H'FFFFE5</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>TCFU = 0 indicates that TCNT has not underflowed.</td>
<td>Bit 5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TCFU = 1 indicates that TCNT has underflowed.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(TCNT value has changed from H'0000 to H'FFFF.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TCFV</td>
<td>Timer Status Register (Overflow Flag)</td>
<td>H'FFFFE5</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>TCFV = 0 indicates that TCNT has not overflowed.</td>
<td>Bit 4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TCFV = 1 indicates that TCNT has overflowed.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>(TCNT value has changed from H'FFFF to H'0000.)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGFB</td>
<td>Timer Status Register (Input Capture/Output Compare Flag B)</td>
<td>H'FFFFE5</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>TGFB = 0 indicates TCNT ≠ TGFB.</td>
<td>Bit 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TGFB = 1 indicates TCNT = TGFB.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TGFA</td>
<td>Timer Status Register (Input Capture/Output Compare Flag A)</td>
<td>H'FFFFE5</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>TGFA = 0 indicates TCNT ≠ TGFA.</td>
<td>Bit 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TGFA = 1 indicates TCNT = TGFA.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TMDR1 BFB</td>
<td>Timer Mode Register (Buffer Operation B)</td>
<td>H'FFFFE1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>BFB = 0 selects normal operation of TGRB.</td>
<td>Bit 5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>BFB = 1 selects buffered operation of TGRB and TGRD.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BFA</td>
<td>Timer Mode Register (Buffer Operation A)</td>
<td>H'FFFFE1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>BFA = 0 selects normal operation of TGRA.</td>
<td>Bit 4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>BFA = 1 selects buffered operation of TGRA and TGRC.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MD3</td>
<td>Timer Mode Register (Mode 3 to 0)</td>
<td>H'FFFFE1</td>
<td>0,0,1,0</td>
</tr>
<tr>
<td>MD2</td>
<td>When MD3 to MD0 = 0000, the TPU operates in normal mode.</td>
<td>Bits 3 to 0</td>
<td></td>
</tr>
<tr>
<td>MD1</td>
<td>When MD3 to MD0 = 0010, the TPU operates in PWM mode 1.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MD0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Register Name | Function | Address | Setting
--- | --- | --- | ---
TCR1 | Timer Control Register (Counter Clear 1, 0)  
CCLR1 | When CCLR1 and CCLR0 = 00, clearing of TCNT is disabled.  
CCLR0 | When CCLR1 and CCLR0 = 10, TCNT is cleared on compare-match or input capture of TGRB.  
| |  | H'FFFFE0 | 1,0
| |  | Bit 6 |  
| |  | Bit 5 |  
| |  | CKEG1 | Timer Control Register (Clock Edge 1, 0)  
| |  | CKEG0 | When CKEG1 and CKEG0 = 00, TCNT counts the rising edges.  
| |  |  | When CKEG1 and CKEG0 = 01, TCNT counts the falling edges.  
| |  |  |  
| |  | TPSC2 | Timer Control Register (Timer Prescaler 2, 1, 0)  
| |  | TPSC1 | When TPSC2 to TPSC0 = 000, the clock source of TCNT is $\phi/1$.  
| |  | TPSC0 | When TPSC2 to TPSC0 = 111, TCNT counts the overflow or underflow of TCNT2.  
| |  |  |  
| TCNT1 | Timer Counter  
|  | 16-bit timer counter | H'FFFFE6 | H'0000
|  |  | Bits 15 to 0 |  
| TGR1A | Timer General Register A  
|  | 16-bit register that is used for output compare or input capture | H'FFFFE8 | H'0002
|  |  | Bits 15 to 0 |  
| TGR1B | Timer General Register B  
|  | 16-bit register that is used for output compare or input capture | H'FFFFEA | H'0004
|  |  | Bits 15 to 0 |  
| TIOR1 | Timer I/O Control Register (I/O Control B3 to B0)  
|  | These bits set the output level on compare-match with TGRB. | H'FFFFE2 | 0,1,0,1
|  |  | Bits 7 to 4 |  
|  | Timer I/O Control Register (I/O Control A3 to A0)  
|  | These bits set the output level on compare-match with TGRA. | H'FFFFE2 | 0,0,1,0
|  |  | Bits 3 to 0 |  
TCR2 | Timer Control Register (Counter Clear 1, 0)  
CCLR1 | When CCLR1 and CCLR0 = 00, clearing of TCNT is disabled.  
CCLR0 | When CCLR1 and CCLR0 = 10, TCNT is cleared on compare-match or input capture of TGRB.  
| |  |  |  
| |  | CKEG1 | Timer Control Register (Clock Edge 1, 0)  
| |  | CKEG0 | When CKEG1 and CKEG0 = 00, TCNT counts the rising edges.  
| |  |  | When CKEG1 and CKEG0 = 01, TCNT counts the falling edges.  
| |  | TPSC2 | Timer Control Register (Timer Prescaler 2, 1, 0)  
| |  | TPSC1 | When TPSC2 to TPSC0 = 000, the clock source of TCNT is $\phi/1$.  
| |  | TPSC0 | When TPSC2 to TPSC0 = 111, the clock source of TCNT is $\phi/1024$.  
| |  |  |  
| TCNT2 | Timer Counter  
|  | 16-bit timer counter | H'FFFFF6 | H'0000
|  |  | Bits 15 to 0 |  
| TSTR | Timer Start Register  
|  | A bit of this register starts/stops the operation of TCNT for the corresponding channel (channels 0 to 5). | H'FFFFC0 | H'06
5.4 RAM Usage

Table 5 describes the RAM usage in this sample task.

<table>
<thead>
<tr>
<th>Label Name</th>
<th>Function (Setting Used in This Sample Task)</th>
<th>Data Length</th>
<th>Used In</th>
</tr>
</thead>
<tbody>
<tr>
<td>lpul_wid</td>
<td>Stores the data to be set in TGR1A (H'0002)</td>
<td>1 word</td>
<td>Main routine</td>
</tr>
<tr>
<td>lpul_cyc</td>
<td>Stores the data to be set in TGR1B (H'0004)</td>
<td>1 word</td>
<td>Main routine</td>
</tr>
</tbody>
</table>
6. Flowchart

6.1 Main Routine

Main routine

Cancel module stop mode of the TPU.

Set TCR2 so that clearing of TCNT2 is disabled and TCNT2 is incremented on the rising edge of internal clock φ/1.

Set TCR1 so that the counter is cleared on compare-match with TGRB and is incremented when TPU2 overflow occurs.

Set TMDR1 to select PWM mode 1 for TPU1.

Set TIOR1 so that a high level is output on compare-match with TGR1A and a low level is output on compare-match with TGR1B.

Set the low-level width of the output pulse of TPU1 (lpul_wid) in TGR1A.

Set the period of the output pulse of TPU1 (lpul_cyc) in TGR1B.

Start counting operation of TPU1 and TPU2.
## Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Mar.09.05</td>
<td>—</td>
<td>—</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>
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