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April 1\textsuperscript{st}, 2010
Renesas Electronics Corporation

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H8S Family
Long-Cycle Pulse Output

Introduction
A pulse with variable cycle period in the range from 6.66 ms to 218.23 s is output using the 32-bit counter. The duty ratio is variable from 0 to 100%.

Target Device
H8S/2339

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1. Specifications

(1) Performs 32-bit counting and outputs a long-cycle pulse with a variable duty cycle (see figure 1).
(2) The duty ratio can be set to any value from 0 to 100%, with a resolution of 1/65535.
(3) In operation at 19.6608 MHz, the pulse period can be set to any value between 6.66 ms and 218.23 s, in 6.66-ms units.

![Figure 1 Example of Long-Cycle Pulse Output](image-url)
2. Description of Module Usage

(1) Two 16-bit counters, TPU1 and TPU2, are connected to operate as a 32-bit counter. The long-cycle pulse thus produced is output from TPU1.

The following features are used:

- Connection of two 16-bit counters to operate as a single 32-bit counter (cascade-connected operation)
- Automatic output of a pulse by hardware with no software intervention (output-compare)
- Generation of PWM output by TGR1A and TGR1B operating as a pair (PWM mode 1)

Figure 2 is a block diagram of the TPU elements used.
3. Principles of Operation

Task operation is as shown in figure 3. As the figure shows, long-cycle pulses are output through a combination of hardware and software processing.

![Diagram](image)

<table>
<thead>
<tr>
<th>Hardware processing</th>
<th>Software processing</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>None</td>
</tr>
</tbody>
</table>

Initial settings
(a) Take the TPU module out of stopped mode.
(b) Set φ to drive the TPU2 counter and overflows of TPU2 to drive TPU1
(c) Set compare-match B as the counter-clearing source for TPU1
(d) Set TPU1 in PWM mode 1
(e) Set TIOR1 to output a high level at TGR1A compare match, and to output a low level at TGR1B compare match
(f) Set the low width for the pulse in TGR1A and the pulse cycle in TGR1B
(g) Start counter operation

Software processing
(a) Generate TPU1 compare-match A
(b) Output a high level from TIOCA1
(c) Output a low level from TIOCA1

Note: Waveforms of low width:high width = 2:3 are created in the sample program. This figure is an example of operation.

Figure 3  Output of the Long-Cycle Pulse
4. Software Description

(1) Function

<table>
<thead>
<tr>
<th>Function</th>
<th>Label</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>LPULMN</td>
<td>Outputs a long-cycle pulse by using the counters of TPU1 and TPU2 in 32-bit</td>
</tr>
</tbody>
</table>

(2) Arguments

<table>
<thead>
<tr>
<th>Label</th>
<th>Description</th>
<th>Data Type</th>
<th>Used in</th>
<th>I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>lpul_wid</td>
<td>Sets the timer value that governs the low width of the output pulse. The low width of the pulse is obtained by the following expression: Low width (ms) = (timer value + 1) x external clock (= 3.33 ms in 19.6608-MHz operation)</td>
<td>unsigned short</td>
<td>Main routine</td>
<td>Input</td>
</tr>
<tr>
<td>lpul_cyc</td>
<td>Sets the timer value that governs the period of the output pulse. The period is obtained by the following expression: Period (ms) = (timer value + 1) x external clock (TCNT2 overflow output) (= 3.33 ms in 19.6608-MHz operation)</td>
<td>unsigned short</td>
<td>Main routine</td>
<td>Input</td>
</tr>
</tbody>
</table>

(3) Internal Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Description</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPU1</td>
<td>TSTR Starts and stops the timer counter</td>
<td>Main routine</td>
</tr>
<tr>
<td></td>
<td>TMDR1 Selects PWM mode 1</td>
<td>Main routine</td>
</tr>
<tr>
<td></td>
<td>TCR1 Sets the clock for input to TCNT1 and the source for counter-clearing</td>
<td>Main routine</td>
</tr>
<tr>
<td></td>
<td>TCNT1 Counts the overflow of TCNT2 and operates as the 32-bit counter</td>
<td>Main routine</td>
</tr>
<tr>
<td></td>
<td>TGR1A Sets the low width of the pulse</td>
<td>Main routine</td>
</tr>
<tr>
<td></td>
<td>TGR1B Sets the high width of the pulse</td>
<td>Main routine</td>
</tr>
<tr>
<td></td>
<td>TIOCA1 Outputs the pulse</td>
<td>Main routine</td>
</tr>
<tr>
<td>TPU2</td>
<td>TCR2 Selects the clock for input to TCNT2</td>
<td>Main routine</td>
</tr>
<tr>
<td></td>
<td>TCNT2 16-bit free-running counter</td>
<td>Main routine</td>
</tr>
</tbody>
</table>

(4) RAM Usage

<table>
<thead>
<tr>
<th>Element</th>
<th>Set Value of the Sample Task</th>
</tr>
</thead>
<tbody>
<tr>
<td>lpul_wid</td>
<td>H'0001</td>
</tr>
<tr>
<td>lpul_cyc</td>
<td>H'0004</td>
</tr>
</tbody>
</table>
5. PAD

(1) Main routine

```
while (1)
{
  Main routine
  LPULMN

  Take the TPU module out of stopped mode.
  Set TCR2 so that the input clock is φ.
  Set TCR1 to start counting of TPU2 overflows and compare-match B as the counter-clearing source.

  Set TMDR1 so that TPU1 is in PWM mode 1.
  Set TDIR1 so that a high level is output at TGR1A compare match and a low level is output at TGR1B compare match.

  Place the low-width value (lpul_wid) for TPU1 pulse output in TGR1A.
  Place the period (lpul_cyc) for TPU1 pulse output in TGR1B.

  Start counting by TPU1 and TPU2.
}
```
## Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Feb. 17.05</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>
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