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---

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April 1\(^{st}\), 2010
Renesas Electronics Corporation

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H8S Family

LCD Display Using 1/4 Duty Drive (LCD Controller/Driver)

Introduction
The segment-type LCD is turned on and off by 1/4 duty drive using the LCD controller/driver and the power-supply circuit.

Target Device
H8S/2268

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1. Specifications ................................................................. 2
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7. Link Addresses ............................................................ 17
1. Specifications

(1) This sample task shows how to use the LCD controller circuit and LCD driver circuit of the H8S/2268 to display information on an LCD module.

(2) Four common signals and 16 segment signals are used for 1/4 duty display.

(3) A sample LCD module connection diagram and LCD display example are shown in figure 1.

![Figure 1: Example of LCD Module Connections](image-url)
2. Functions Used

(1) Features of LCD Controller/Driver

In this sample task information is displayed on an LCD module using the H8S/2268 internal LCD controller/driver. The features of the LCD controller/driver are listed below.

- Display Capacity
  (a) Duty cycle: static (internal driver: 40 SEG)
  (b) Duty cycle: 1/2 (internal driver: 40 SEG)
  (c) Duty cycle: 1/3 (internal driver: 40 SEG)
  (d) Duty cycle: 1/4 (internal driver: 40 SEG)
- LCD RAM capacity: 8 bits × 20 bytes (160 bits)
- Byte or word access to LCD RAM is supported.
- The segment output pins can be used as ports in groups of eight.
- In the static mode and with 1/2 duty, common output pins not used because of the duty cycle can be used for common double-buffering (parallel connection).
- A choice of 11 frame frequencies is supported.
- A or B waveform is selectable by software.
- Built-in power supply split-resistors and LCD drive power supply.
- Display is possible in operating modes other than the standby mode and the module stop mode.
- Display is possible during low-voltage operation using built-in triple step-up voltage circuit.
- Module stop mode halts LCD operation when not in use.
(2) Block Diagram of LCD Controller/Driver

A block diagram of the LCD controller/driver used in this sample task is shown in figure 2.

Figure 2  Block Diagram of LCD Controller/Driver
(3) Functions of LCD Controller/Driver

- **LCD port control register (LPCR)**
  LPCR is an 8-bit readable/writable register that selects the duty cycle, LCD driver, and pin functions.

- **LCD control register (LCR)**
  LCR is an 8-bit readable/writable register that performs LCD drive power supply on/off control, display function activation control, display data control, and frame frequency selection.

- **LCD control register 2 (LCR2)**
  LCR2 is an 8-bit readable/writable register that controls switching between the A waveform and B waveform, selects the clock source for the triple step-up voltage circuit, selects the drive power supply, and selects the duty cycle for periods when the power supply split-resistors are connected to the power supply circuit.

- **Segment output pins (SEG40 to SEG1)**
  These pins are used to drive the LCD segments. All can also function as ports and their settings are programmable.

- **Common output pins (COM4 to COM1)**
  These are the common drive pins for the LCD. In the static mode and with 1/2 duty, these pins can be used in parallel.

- **LCD power supply pins (V1, V2, V3)**
  These pins are used when the H8S/2268 is connected to a bypass capacitor, and an external power supply is used. The V3 pin functions as the reference power supply input to the LCD when the triple step-up voltage circuit is used.

- **LCD step-up voltage capacitance pins (C1, C2)**
  These are the capacitance pins for the LCD drive power supply step-up voltage.

- **LCD RAM**
  Used to set the display data. The relationship between LCD RAM and the display segments differs depending on the duty cycle. After setting the registers required for display, data is written to the portions of LCD RAM corresponding to the duty cycle using normal RAM instructions. Display begins automatically when the LCD is powered on. Word- or byte-access instructions may be used for RAM setting.

(4) Connection Diagram

In this sample task an 8-digit 8-segment LCD and 1/4 duty cycle are used for LCD display. A connection diagram for the segment signals and common signals for the 8-digit 8-segment LCD used in the sample task is shown in figure 3.
(5) LCD RAM Map

A map of LCD RAM for 1/4 duty cycle operation is shown in figure 4.

<table>
<thead>
<tr>
<th>bit7</th>
<th>bit6</th>
<th>bit5</th>
<th>bit4</th>
<th>bit3</th>
<th>bit2</th>
<th>bit1</th>
<th>bit0</th>
</tr>
</thead>
<tbody>
<tr>
<td>H'FFFC40</td>
<td>SEG2</td>
<td>SEG2</td>
<td>SEG2</td>
<td>SEG2</td>
<td>SEG1</td>
<td>SEG1</td>
<td>SEG1</td>
</tr>
<tr>
<td>H'FFFC41</td>
<td>SEG4</td>
<td>SEG4</td>
<td>SEG4</td>
<td>SEG4</td>
<td>SEG3</td>
<td>SEG3</td>
<td>SEG3</td>
</tr>
<tr>
<td>H'FFFC42</td>
<td>SEG6</td>
<td>SEG6</td>
<td>SEG6</td>
<td>SEG5</td>
<td>SEG5</td>
<td>SEG5</td>
<td>SEG5</td>
</tr>
<tr>
<td>H'FFFC43</td>
<td>SEG8</td>
<td>SEG8</td>
<td>SEG8</td>
<td>SEG7</td>
<td>SEG7</td>
<td>SEG7</td>
<td>SEG7</td>
</tr>
<tr>
<td>H'FFFC44</td>
<td>SEG10</td>
<td>SEG10</td>
<td>SEG10</td>
<td>SEG9</td>
<td>SEG9</td>
<td>SEG9</td>
<td>SEG9</td>
</tr>
<tr>
<td>H'FFFC45</td>
<td>SEG12</td>
<td>SEG12</td>
<td>SEG12</td>
<td>SEG11</td>
<td>SEG11</td>
<td>SEG11</td>
<td>SEG11</td>
</tr>
<tr>
<td>H'FFFC46</td>
<td>SEG14</td>
<td>SEG14</td>
<td>SEG14</td>
<td>SEG13</td>
<td>SEG13</td>
<td>SEG13</td>
<td>SEG13</td>
</tr>
<tr>
<td>H'FFFC47</td>
<td>SEG16</td>
<td>SEG16</td>
<td>SEG16</td>
<td>SEG15</td>
<td>SEG15</td>
<td>SEG15</td>
<td>SEG15</td>
</tr>
<tr>
<td>H'FFFC48</td>
<td>SEG18</td>
<td>SEG18</td>
<td>SEG18</td>
<td>SEG17</td>
<td>SEG17</td>
<td>SEG17</td>
<td>SEG17</td>
</tr>
<tr>
<td>H'FFFC49</td>
<td>SEG20</td>
<td>SEG20</td>
<td>SEG20</td>
<td>SEG19</td>
<td>SEG19</td>
<td>SEG19</td>
<td>SEG19</td>
</tr>
<tr>
<td>H'FFFC4A</td>
<td>SEG22</td>
<td>SEG22</td>
<td>SEG22</td>
<td>SEG21</td>
<td>SEG21</td>
<td>SEG21</td>
<td>SEG21</td>
</tr>
<tr>
<td>H'FFFC4B</td>
<td>SEG24</td>
<td>SEG24</td>
<td>SEG24</td>
<td>SEG23</td>
<td>SEG23</td>
<td>SEG23</td>
<td>SEG23</td>
</tr>
<tr>
<td>H'FFFC4C</td>
<td>SEG26</td>
<td>SEG26</td>
<td>SEG26</td>
<td>SEG25</td>
<td>SEG25</td>
<td>SEG25</td>
<td>SEG25</td>
</tr>
<tr>
<td>H'FFFC4D</td>
<td>SEG28</td>
<td>SEG28</td>
<td>SEG28</td>
<td>SEG27</td>
<td>SEG27</td>
<td>SEG27</td>
<td>SEG27</td>
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<tr>
<td>H'FFFC4E</td>
<td>SEG30</td>
<td>SEG30</td>
<td>SEG30</td>
<td>SEG29</td>
<td>SEG29</td>
<td>SEG29</td>
<td>SEG29</td>
</tr>
<tr>
<td>H'FFFC4F</td>
<td>SEG32</td>
<td>SEG32</td>
<td>SEG32</td>
<td>SEG31</td>
<td>SEG31</td>
<td>SEG31</td>
<td>SEG31</td>
</tr>
<tr>
<td>H'FFFC50</td>
<td>SEG34</td>
<td>SEG34</td>
<td>SEG34</td>
<td>SEG33</td>
<td>SEG33</td>
<td>SEG33</td>
<td>SEG33</td>
</tr>
<tr>
<td>H'FFFC51</td>
<td>SEG36</td>
<td>SEG36</td>
<td>SEG36</td>
<td>SEG35</td>
<td>SEG35</td>
<td>SEG35</td>
<td>SEG35</td>
</tr>
<tr>
<td>H'FFFC52</td>
<td>SEG38</td>
<td>SEG38</td>
<td>SEG38</td>
<td>SEG37</td>
<td>SEG37</td>
<td>SEG37</td>
<td>SEG37</td>
</tr>
<tr>
<td>H'FFFC53</td>
<td>SEG40</td>
<td>SEG40</td>
<td>SEG40</td>
<td>SEG39</td>
<td>SEG39</td>
<td>SEG39</td>
<td>SEG39</td>
</tr>
</tbody>
</table>

Figure 4  Map of LCD RAM for 1/4 Duty Cycle

(6) Relationship between LCD Display and LCD RAM Setting Values

The relationship between the information displayed on the 8-digit 8-segment LCD used in this sample task and the LCD RAM setting values is shown in figure 5. Figure 5 shows the values set in the LCD RAM used to display “H8S.2268F” on the 8-digit 8-segment LCD.

<table>
<thead>
<tr>
<th>bit7</th>
<th>bit6</th>
<th>bit5</th>
<th>bit4</th>
<th>bit3</th>
<th>bit2</th>
<th>bit1</th>
<th>bit0</th>
</tr>
</thead>
<tbody>
<tr>
<td>H'FFFC51</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>H'FFFC50</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
| H'FFFC4F | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | Display data for "S."
| H'FFFC4E | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | Display data for "2"
| H'FFFC4D | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | Display data for "2"
| H'FFFC4C | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | Display data for "6"
| H'FFFC4B | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | Display data for "8"
| H'FFFC4A | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | Display data for "F"

Figure 5  Relationship between LCD Display and LCD RAM Setting Values
(7) LCD Display/Non-Display

The relationship between SEG21 and SEG22 of the 8-digit 8-segment LCD and the corresponding values set in the LCD RAM is shown in figure 6. As shown in figure 6, a setting of 1 for a bit in LCD RAM for a segment from 0 to 7 causes the corresponding segment to display, and a setting of 0 causes non-display.

![Diagram showing LCD Display/Non-Display relationship](diagram.png)

**Figure 6** Relationship between LCD Display/Non-Display and Corresponding LCD RAM Setting Values
(8) Display Data Examples

Display examples for SEG21 and SEG22 of the 8-digit 8-segment LCD and the corresponding display data are shown in table 1.

Table 1  Display Data Examples

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Display Address</th>
<th>Display Data</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Hexadecimal number</td>
<td>Binary number</td>
</tr>
<tr>
<td></td>
<td>H'FFFC4A</td>
<td>0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>-</td>
<td>H'FFFC4A</td>
<td>0 0 1 0 0 0 0 0</td>
</tr>
<tr>
<td>-</td>
<td>H'FFFC4A</td>
<td>0 0 0 0 1 0 0 0</td>
</tr>
<tr>
<td>0</td>
<td>H'FFFC4A</td>
<td>1 1 0 1 0 1 1 1</td>
</tr>
<tr>
<td>1</td>
<td>H'FFFC4A</td>
<td>0 0 0 0 0 1 1 0</td>
</tr>
<tr>
<td>2</td>
<td>H'FFFC4A</td>
<td>1 1 1 0 0 0 1 1</td>
</tr>
<tr>
<td>3</td>
<td>H'FFFC4A</td>
<td>1 0 1 0 0 1 1 1</td>
</tr>
<tr>
<td>4</td>
<td>H'FFFC4A</td>
<td>0 0 1 1 0 1 1 0</td>
</tr>
<tr>
<td>5</td>
<td>H'FFFC4A</td>
<td>1 0 1 1 0 1 0 1</td>
</tr>
<tr>
<td>6</td>
<td>H'FFFC4A</td>
<td>1 1 1 1 0 1 0 1</td>
</tr>
<tr>
<td>7</td>
<td>H'FFFC4A</td>
<td>0 0 0 0 0 1 1 1</td>
</tr>
<tr>
<td>8</td>
<td>H'FFFC4A</td>
<td>1 1 1 1 0 1 1 1</td>
</tr>
<tr>
<td>9</td>
<td>H'FFFC4A</td>
<td>1 0 1 1 0 1 1 1</td>
</tr>
<tr>
<td>A</td>
<td>H'FFFC4A</td>
<td>0 1 1 1 0 1 1 1</td>
</tr>
<tr>
<td>B</td>
<td>H'FFFC4A</td>
<td>1 1 1 1 0 1 0 0</td>
</tr>
<tr>
<td>C</td>
<td>H'FFFC4A</td>
<td>1 1 0 1 0 0 0 1</td>
</tr>
<tr>
<td>D</td>
<td>H'FFFC4A</td>
<td>1 1 1 0 0 1 1 0</td>
</tr>
<tr>
<td>E</td>
<td>H'FFFC4A</td>
<td>1 1 1 1 0 0 0 1</td>
</tr>
<tr>
<td>F</td>
<td>H'FFFC4A</td>
<td>0 1 1 1 0 0 0 1</td>
</tr>
</tbody>
</table>
(9) Assignment of Functions

Assignment of functions in this sample task is shown in table 2.

<table>
<thead>
<tr>
<th>Elements</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPCR</td>
<td>Selects the duty cycle, the LCD driver, and pin functions.</td>
</tr>
<tr>
<td>LCR</td>
<td>Performs LCD power supply on/off control, display function activation control, display data control, and frame frequency selection.</td>
</tr>
<tr>
<td>LCR2</td>
<td>Controls switching between the A and B waveforms, selects the clock source for triple step-up voltage circuit, selects drive power supply, and selects duty cycle for periods when power supply split-resistors are connected to the power supply circuit.</td>
</tr>
<tr>
<td>SEG36 to SEG21</td>
<td>Used to drive the LCD segments</td>
</tr>
<tr>
<td>COM4 to COM1</td>
<td>Used as common drivers</td>
</tr>
<tr>
<td>LCD RAM</td>
<td>Sets LCD display data (addresses H'FFFC40 to H'FFFC53)</td>
</tr>
</tbody>
</table>
3. Principles of Operation

(1) Hardware Settings
(a) LCD Drive Power Supply Settings
The H8S/2268 supports use of its built-in power supply circuit, or use of an external power supply circuit, as the LCD drive power supply. If an external power supply circuit is used as the LCD drive power supply, connect the V1 pin to the external power supply.
(b) Triple Step-up Voltage Circuit
The H8S/2268 uses a triple step-up voltage circuit so that a voltage three times the LCD input reference voltage from the V3 pin can be used to drive the LCD. In this sample task operation of the triple step-up voltage circuit is turned off (the SUPS bit = 0).

(2) Software Settings
The software settings for implementing LCD display are described below.
(a) Selecting the Duty Cycle and Common Function
The DTS1 and DTS0 bits are used to select the duty cycle setting from among static mode, 1/2 duty, 1/3 duty, and 1/4 duty. The CMX bit is used to select the common double-buffering function.
(b) Selecting the Segment Drivers
The SGS3 to SGS0 bits are used to select the segment drivers to be used.
(c) Selecting the Frame Frequency
The CKS3 to CKS0 bits are used to select the frame frequency. Select a frame frequency that matches the specifications of the LCD module used.
(d) Selecting A Waveform or B Waveform
The LCDAB bit is used to select the A waveform or the B waveform as the LCD waveform.
(e) Selecting the LCD Drive Power Supply
The SUPS bit can be used to select the power supply if the internal power supply circuit is used. To use an external power supply circuit, select $V_{CC}$ using SUPS and turn the LCD drive power supply off using the PSW bit.
(3) Principles of Operation

The principles of operation of this sample task are illustrated in figure 7.

![Figure 7 Principles of Operation](image-url)
4. Description of Software

(1) Modules

Table 3 shows the modules used in this sample task.

<table>
<thead>
<tr>
<th>Module</th>
<th>Label</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>main</td>
<td>Performs initial settings for LCD RAM and LCD controller/driver, and</td>
</tr>
<tr>
<td></td>
<td></td>
<td>displays information on LCD</td>
</tr>
</tbody>
</table>

(2) Arguments

No arguments are used in this sample task.

(3) Internal Registers Used

The internal registers used in this sample task are shown in table 4.

<table>
<thead>
<tr>
<th>Register</th>
<th>Bit Name</th>
<th>Description</th>
<th>Address</th>
<th>Set Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPCR</td>
<td>DTS1</td>
<td>Duty cycle select 1 and 0</td>
<td>Bit 7</td>
<td>DTS1 = 1</td>
</tr>
<tr>
<td></td>
<td>DTS0</td>
<td>The combination of DTS1 and DTS0 selects static mode, or 1/2, 1/3, or 1/4 duty.</td>
<td>Bit 6</td>
<td>DTS0 = 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• DTS1 = 1, DTS0 = 1: 1/4 duty selected</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>CMX</td>
<td>Common function select</td>
<td>Bit 5</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Specifies whether or not the same waveform is to be output from multiple pins to increase the common drive power when not all common pins are used because of the duty setting.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• CMX = 0: Same waveform not output from multiple common pins not used because of duty setting</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• CMX = 1: Same waveform output from multiple common pins not used because of duty setting</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>SGS3</td>
<td>Segment driver select 3 to 0</td>
<td>Bit 3</td>
<td>SGS3 = 0</td>
</tr>
<tr>
<td></td>
<td>SGS2</td>
<td>These bits select the segment drivers to be used.</td>
<td>Bit 2</td>
<td>SGS2 = 0</td>
</tr>
<tr>
<td></td>
<td>SGS1</td>
<td>• SGS3 = 0, SGS2 = 0, SGS1 = 1, SGS0 = 1: Pins</td>
<td>Bit 1</td>
<td>SGS1 = 1</td>
</tr>
<tr>
<td></td>
<td>SGS0</td>
<td>SEG40 to SEG17 function as segment drivers and SEG16 to SEG1 function as port pins</td>
<td>Bit 0</td>
<td>SGS0 = 1</td>
</tr>
<tr>
<td>Register</td>
<td>Bit Name</td>
<td>Description</td>
<td>Address</td>
<td>Set Value</td>
</tr>
<tr>
<td>----------</td>
<td>------------------------------</td>
<td>-----------------------------------------------------------------------------</td>
<td>-----------</td>
<td>-----------</td>
</tr>
<tr>
<td>LCR</td>
<td>LCD control register</td>
<td></td>
<td>H'FFFFFC1</td>
<td>H'31</td>
</tr>
</tbody>
</table>
| PSW      | LCD power supply split-resistor connection control | This bit can be used to disconnect the LCD power supply split-resistors from $V_{CC}$ when LCD display is not required in a power-down mode or when an external power supply is used. When the ACT bit is cleared to 0, and also in the standby mode, the LCD power supply split-resistors are disconnected from $V_{CC}$ regardless of the setting of this bit.  
* PSW = 0: LCD power supply split-resistors are disconnected from $V_{CC}$  
* PSW = 1: LCD power supply split-resistors are connected to $V_{CC}$ | Bit 6   | 0          |
| ACT      | Display function activate    | This bit specifies whether or not the LCD controller/driver is used. Clearing this bit to 0 halts operation of the LCD controller/driver. The LCD drive power supply is also turned off, regardless of the setting of the PSW bit. However, register contents are retained.  
* ACT = 0: LCD controller/driver operation disabled  
* ACT = 1: LCD controller/driver operation enabled | Bit 5   | 1          |
| DISP     | Display data control         | This bit specifies whether the contents of LCD RAM are displayed or blank data is displayed regardless of the LCD RAM contents.  
* DISP = 0: Blank data is displayed  
* DISP = 1: LCD RAM data is displayed | Bit 4   | 1          |
| CKS3     | Frame frequency select 3 to 0 |                                                                             | Bit 3     | CKS3 = 0  |
| CKS2     | These bits select the clock source and frame frequency. |                                                                             | Bit 2     | CKS2 = 0  |
| CKS1     |                                                                             |                                                                             | Bit 1     | CKS1 = 1  |
| CKS0     |                                                                             | CKS3 = 0, CKS2 = 0, CKS1 = 0, CKS0 = 1:  
* $\phi_{SUB/2}$ selected as the clock source and 64 Hz selected as the frame frequency | Bit 0   | CKS0 = 1   |
Table 4 Internal Registers Used (cont)

<table>
<thead>
<tr>
<th>Register</th>
<th>Bit Name</th>
<th>Description</th>
<th>Address</th>
<th>Set Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCR2</td>
<td>LCDAB</td>
<td>A waveform/B waveform switching control</td>
<td>H'FFFFC2</td>
<td>H'00</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Specifies whether the A waveform or B waveform is used as the LCD drive waveform.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• LCDAB = 0: Drive using the A waveform</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• LCDAB = 1: Drive using the B waveform</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HCKS</td>
<td></td>
<td>Triple step-up voltage circuit clock select</td>
<td>Bit 7</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Selects the clock used for the triple step-up voltage circuit. This bit selects a clock which is equivalent to the clock specified by the LCD operating control register (LCR) divided by 4 or 8 as the step-up voltage circuit clock.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• HCKS = 0: Clock equivalent to LCD operating clock divided by 4 selected as step-up voltage circuit clock</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• HCKS = 1: Clock equivalent to LCD operating clock divided by 8 selected as step-up voltage circuit clock</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SUPS</td>
<td></td>
<td>Drive power select, triple step-up voltage circuit control</td>
<td>Bit 5</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The triple step-up voltage circuit stops operating when Vcc is selected as the drive power supply. The triple step-up voltage circuit starts operating when the LCD input reference voltage (VLCD3) is selected as the drive power supply.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• SUPS = 0: Drive power supply is Vcc, triple step-up voltage circuit halts</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• SUPS = 1: Drive power supply is triple step-up voltage of the LCD input reference voltage (VLCD3); triple step-up voltage circuit operates</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CDS3</td>
<td>CDS2</td>
<td>Selection of duty cycle for charge/discharge pulse</td>
<td>Bit 3</td>
<td>CDS3 = 0</td>
</tr>
<tr>
<td>CDS2</td>
<td></td>
<td>Selects the duty cycle for periods when the power supply divider resistance is connected to the power supply circuit. A duty cycle of 0 specifies a fixed state in which the power supply divider resistance is separated from the power supply circuit. Therefore, it is necessary to supply power to pins V1, V2, and V3 from an external circuit.</td>
<td>Bit 2</td>
<td>CDS2 = 0</td>
</tr>
<tr>
<td>CDS1</td>
<td></td>
<td>• CDS3 = 0, CDS2 = 0, CDS1 = 0, CDS0 = 0: Duty cycle = 1</td>
<td>Bit 1</td>
<td>CDS1 = 1</td>
</tr>
<tr>
<td>CDS0</td>
<td></td>
<td>• CDS3 = 0, CDS2 = 0, CDS1 = 0, CDS0 = 1: Duty cycle = 1</td>
<td>Bit 0</td>
<td>CDS0 = 1</td>
</tr>
<tr>
<td>MSTPCRD</td>
<td>MSTPD6</td>
<td>Module stop control register D</td>
<td>H'FFFF60</td>
<td>H'BF</td>
</tr>
<tr>
<td>MSTPD6</td>
<td></td>
<td>• MSTPD6 = 0: LCD controller/driver module stop mode cleared</td>
<td>Bit 6</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• MSTPD6 = 1: LCD controller/driver module stop mode set</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(4) RAM Usage

No RAM is used in this sample task.
5. Flowchart

(1) Main Routine

```
main()

Set the I bit to 1 to disable interrupts

MSTPCRD = H'BF
Clear bit 6 to 0 to clear LCD controller/driver module stop mode

lcdram = LCD RAM
Set LCD RAM start address in lcdram

i = 0

i < 20
All 20 bytes of LCD RAM cleared?

All cleared

Some still not cleared

i++

lcdram = LCDRAM+H'00000A
Set LCD RAM addresses corresponding to SEG21 and SEG22 in lcdram

LPCR = H'C3
Set 1/4 duty and SEG21 to SEG36 in segment driver

LCR = H'31
Separate LCD power supply split-resistors from VCC
Operate LCD controller/driver
Display LCD RAM data
Use φSUB/2 as clock source
Frame 64 Hz

LCR2 = H'00
Select A waveform, halt triple step-up voltage circuit, select 1 as charge/discharge pulse duty cycle

lcdram[7]=H'76 "H"
lcdram[6]=H'F7 "8"
lcdram[5]=H'BD "S."
lcdram[4]=H'E3 "2"
lcdram[3]=H'E3 "2"
lcdram[2]=H'F5 "6"
lcdram[1]=H'F7 "8"
lcdram[0]=H'71 "F"
Set "H8S.2268F" in LCD RAM

Clear the I bit to 0 to enable interrupts

Note: *In this sample task the stack pointer is set by INIT.SRC (assembly language).
6. Program Listings

INIT. SRC program listing

```
.export _INIT
.import _main
;
.section P, CODE, ALIGN=2
_INIT:
    mov.l #h'ffefc0, er7
    ldc.b #b'10000000, ccr
    ldc.b #0, exr
    jmp @_main
;
.end
```

/*****************************/
/*
/* H8S/2000 Series -H8S/2268-
/* Application Note
/*
/* 'Liquid Crystal Display
/* -1/4 Duty Drive, Internal Driver-'
/*
/* Function
/* : LCD Controller / Driver
/*
/*
/* External Clock : 10MHz
/* Internal Clock : 10MHz
/* Sub Clock : 32.768kHz
/*
/*****************************/
#include <machine.h>
/*****************************/
/* Symbol Definition */
/*****************************/
#define LPCR *(volatile unsigned char *)0xFFFC30 /* LCD Port Control Register */
#define LCR *(volatile unsigned char *)0xFFFC31 /* LCD Control Register */
#define LCR2 *(volatile unsigned char *)0xFFFC32 /* LCD Control Register 2 */
#define LCD RAM (volatile unsigned char *)0xFFFC40 /* LCD RAM */
#define MSTPCRD *(volatile unsigned char *)0xFFFC60 /* Module Stop Control Registers D */
/*****************************/
/* Function define */
/*****************************/
extern void INIT ( void ); /* SP Set */
void main ( void );
/*****************************/
/* Vector Address */
/*****************************/
#pragma section V1 /* VECTOR SECTOIN SET */
void (*const VEC_TBL1[])(void) = { /* 0x00 - 0x0f */
    INIT /* 00 Reset */
};
#pragma section /* P */
/************************************************************/
/* Main Program                                              */
/************************************************************/

void main ( void )
{
  int i;
  unsigned char *LCD_RAM;
  set_imask_crr(1);       /* Interrupt Disable */
  MSTPCR = 0xBF;          /* module stop mode is cleared */
  LCD_RAM = LCD_RAM;      /* Set LCD RAM */
  for ( i = 0; i < 20; i++ )
  {
    LCD_RAM[i] = 0;        /* Initialize LCD RAM */
  }
  LCD_RAM = LCD_RAM + 0x00000A;    /* Set LCD RAM Address */
  LPCR = 0xC3;            /* 1/4 Duty / SEG40-SEG17 ON */
  LCR = 0x31;             /* LCD ON / Phi_sub/2 */
  LCR2 = 0x00;            /* A waveform / Drive power is Vcc */
  LCD_RAM[7] = 0x76;      /* "H " */
  LCD_RAM[6] = 0xF7;      /* "8 " */
  LCD_RAM[5] = 0xBD;      /* "S." */
  LCD_RAM[4] = 0xE3;      /* "2 " */
  LCD_RAM[3] = 0xE3;      /* "2 " */
  LCD_RAM[2] = 0xF5;      /* "6 " */
  LCD_RAM[1] = 0xF7;      /* "8 " */
  LCD_RAM[0] = 0x71;      /* "F " */
  set_imask_crr(0);      /* Interrupt Enable */
  while(1);
}

7. Link Addresses

<table>
<thead>
<tr>
<th>Section</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>CV1</td>
<td>H'000000</td>
</tr>
<tr>
<td>P</td>
<td>H'000100</td>
</tr>
<tr>
<td>Rev.</td>
<td>Date</td>
</tr>
<tr>
<td>------</td>
<td>------------</td>
</tr>
<tr>
<td>1.00</td>
<td>Mar.09.05</td>
</tr>
</tbody>
</table>
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