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April 1st, 2010
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H8S Family

Hardware Standby Mode

Introduction

This application note discusses how to handle transitions to and from hardware standby mode such that data in the on-chip RAM is retained.

Target Device

H8S/2377F

The procedures described in this application note also apply to other H8S family devices that have the same hardware standby functions as the H8S/2377F. However, since particular functions might be modified through the addition of functionality, etc., the information should be checked against the manual. Fully evaluate any utilization of this application note.

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1. Specifications

This application note covers how to handle transitions to and from hardware standby mode, under the conditions described below, such that data in the on-chip RAM is retained.

(1) When access to the on-chip RAM is enabled

The RAM enable bit (RAME) in the system control register (SYSCR) is set to 1, enabling access to the on-chip RAM.

(2) When access to the on-chip RAM is disabled

The RAME bit in SYSCR is cleared to 0, disabling access to the on-chip RAM.

2. Functional Description

2.1 Functions

This application note covers how to handle transitions to and from hardware standby mode such that data in the on-chip RAM is retained. The following explains hardware standby mode.

2.1.1 Hardware standby mode

(1) Transition to hardware standby mode

From any other state, hardware standby mode is entered when a low level is on the $\overline{\text{STBY}}$ pin.

In hardware standby mode, power consumption is significantly reduced because all modules are placed in the reset state and thus stopped. Data stored in the on-chip RAM is retained for as long as the minimum voltage is supplied. The I/O ports enter the high-impedance state.

To retain data in the on-chip RAM, disable access to the on-chip RAM by clearing the RAME bit in SYSCR to 0 or driving the $\overline{\text{RES}}$ pin low before driving the $\overline{\text{STBY}}$ pin low. Do not change the states of the mode pins (MD2 to MD0) during periods in hardware standby mode.

(2) Release from hardware standby mode

Release from hardware standby mode is handled through the $\overline{\text{STBY}}$ and $\overline{\text{RES}}$ pins. Driving the $\overline{\text{STBY}}$ pin high while maintaining a low level on the $\overline{\text{RES}}$ pin puts the system in reset mode and starts clock oscillation. During this time, the $\overline{\text{RES}}$ pin must be kept low until the clock oscillation becomes stable (for the required oscillation stabilization time, refer to the hardware manual).

2.1.2 Reset

The reset has the highest priority of all forms of exception handling. A low level on the $\overline{\text{RES}}$ pin halts all running processes and places the LSI in the reset state. To ensure that the LSI is reset, keep the $\overline{\text{RES}}$ pin low for at least 20 ms after power is supplied. In a reset, the internal states of the CPU and registers in the on-chip peripheral modules are initialized. The interrupt control mode is 0 immediately after a reset.

(1) Reset exception handling

When the signal on the $\overline{\text{RES}}$ pin is driven high after the above period at low level, reset exception handling starts and the LSI operates as described below.

1. The internal states of the CPU and registers in the on-chip peripheral modules are initialized. The T bit in EXR is cleared to 0 and the I bits in EXR and CCR are set.
2. The reset exception handler's vector address is read out and transferred to the PC, after which the LSI starts program execution from the address indicated by the PC.

3. Description of Operation

3.1 When Access to On-Chip RAM is Enabled

When the RAME bit in SYSCR is set to 1, enabling access to the on-chip RAM, data in the on-chip RAM is retained with the following procedure. Figure 1 shows the operation when access to the on-chip RAM is enabled.

(1) Transition to hardware standby mode

1. Set the RAME bit in SYSCR to 1 to enable access to the on-chip RAM.
2. Drive the $\overline{\text{RES}}$ line to low level. If $\overline{\text{STBY}}$ is driven low with arbitrary timing while the on-chip RAM is accessible, this LSI could enter hardware standby mode in the midst of access to the on-chip RAM. This corrupts the data in the on-chip RAM. To prevent this from happening, drive the $\overline{\text{RES}}$ line to low level before driving the $\overline{\text{STBY}}$ line low.
3. Drive the $\overline{\text{STBY}}$ line to low level for the transition to hardware standby mode.

(2) Release from hardware standby mode and transition to program execution

1. Drive the $\overline{\text{STBY}}$ line high to release the LSI from hardware standby mode.
2. Drive the $\overline{\text{RES}}$ line low to place the LSI in the reset exception handling state.
3. The state then makes the transition to the program execution state.

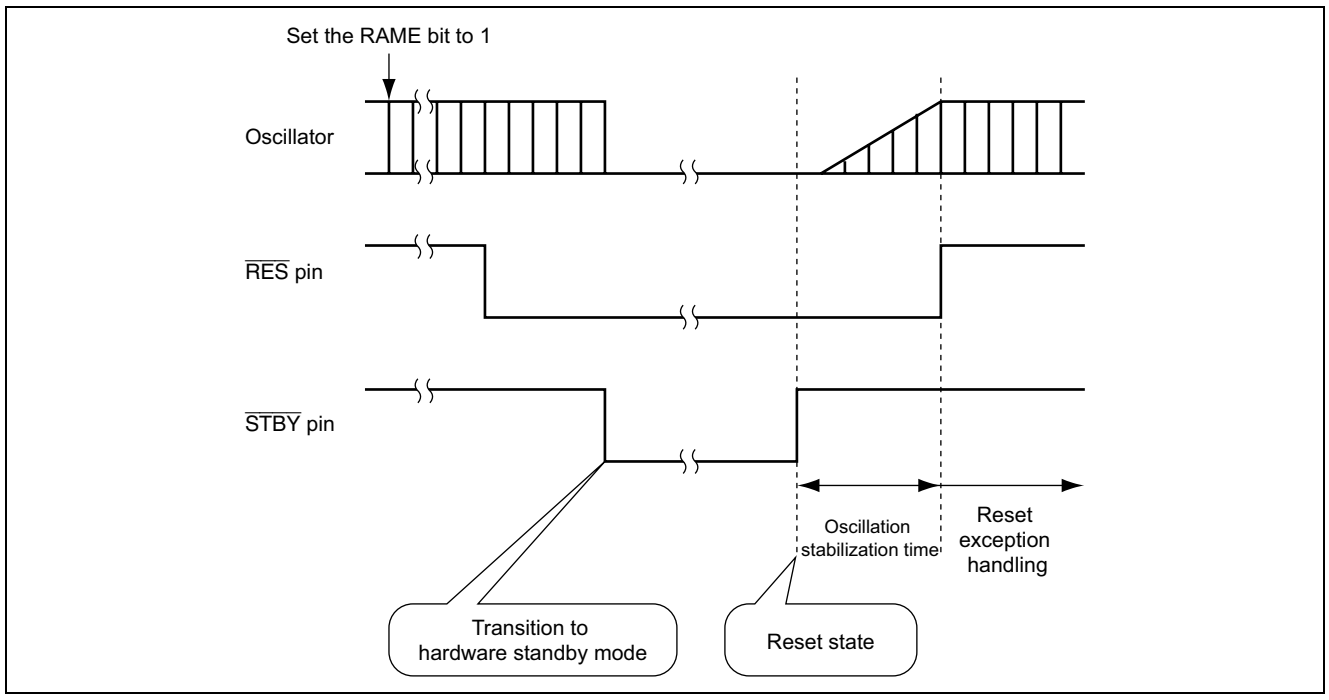

Figure 1 Operation while On-chip RAM Access is Enabled

3.2 When Access to On-Chip RAM is Disabled

When the RAME bit in SYSCR is set to 0, disabling access to the on-chip RAM, data in the on-chip RAM is retained with the following procedure. Figure 2 shows the operation when access to the on-chip RAM is disabled.

(1) Transition to hardware standby mode

1. Set the RAME bit in SYSCR to 0 to disable access to the on-chip RAM.
2. For the transition to hardware standby mode, drive the $\overline{\text{RES}}$ and $\overline{\text{STBY}}$ signals low in an arbitrary order. Since access to the on-chip RAM is disabled, data in the on-chip RAM is retained regardless of the order in which $\overline{\text{RES}}$ and $\overline{\text{STBY}}$ are driven low.

(2) Release from hardware standby mode and transition to program execution

1. Drive the $\overline{\text{STBY}}$ signal high to release the LSI from hardware standby mode.
2. Drive the $\overline{\text{RES}}$ signal low to place the LSI in the reset exception handling state.
3. The state then makes the transition to the program execution state.

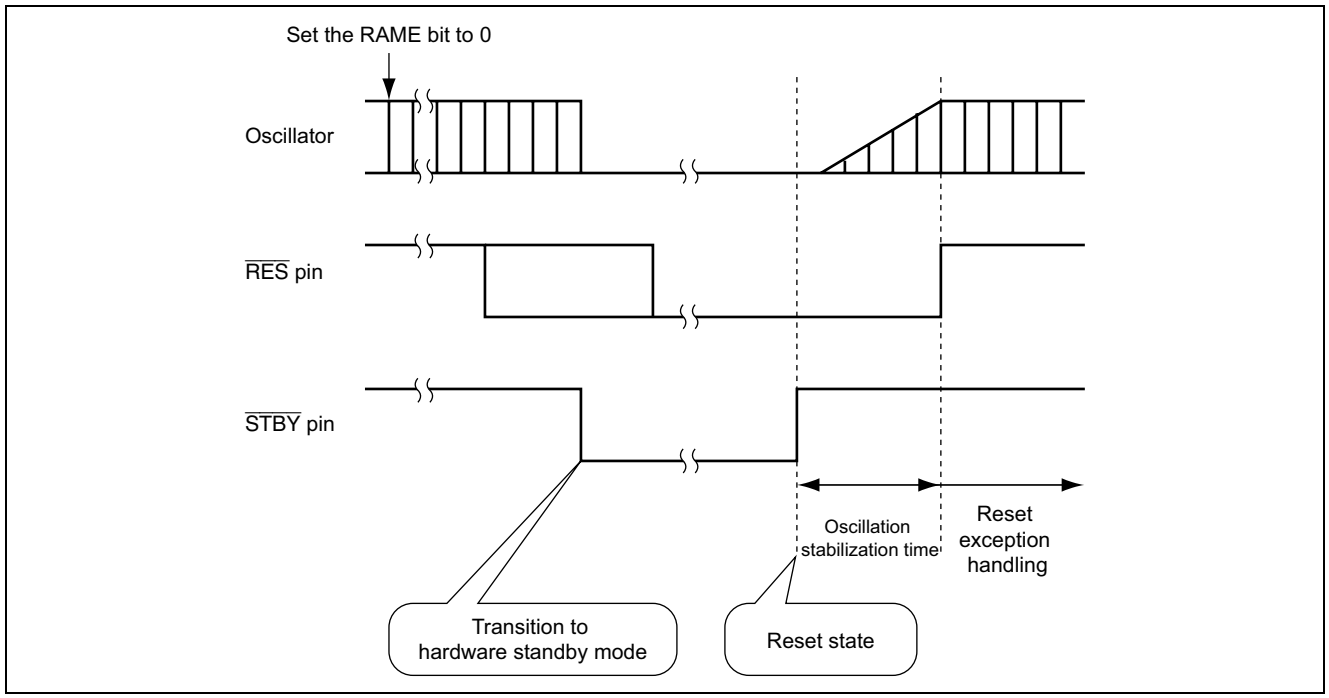

Figure 2 Operation while On-chip RAM Access is Disabled

4. Internal Registers

The register used in this application note is shown below.

- System control register (SYSCR) Address: H'FFFF3D

Bit	Bit Name	R/W	Function
0	RAME	R/W	RAM Enable Selects enabling/disabling of on-chip RAM. This bit is initialized to 1 on release from the reset state. 0: On-chip RAM disabled 1: On-chip RAM enabled

Revision Record

		Description	
Rev.	Date	Page	Summary
1.00	Jul.22.05	—	First edition issued

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