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H8S Family

Generating PWM Output by Using Buffer Operation of the TPU

Introduction

This application note discusses how to generate PWM waveform output by using the buffer operation of the output-compare function of the 16-bit timer pulse unit (TPU).

Target Device

H8S/2339

Contents

1. Specifications

- As shown in figure 1, a PWM waveform with varied high- and low-pulse widths is output.
- The period of output PWM pulses can be set within the range from approximately 102 ns to 3.33 ms (the value that can be set in the buffer register ranges from H'0001 to H'FFFF) when the operating frequency is 19.6608 MHz.

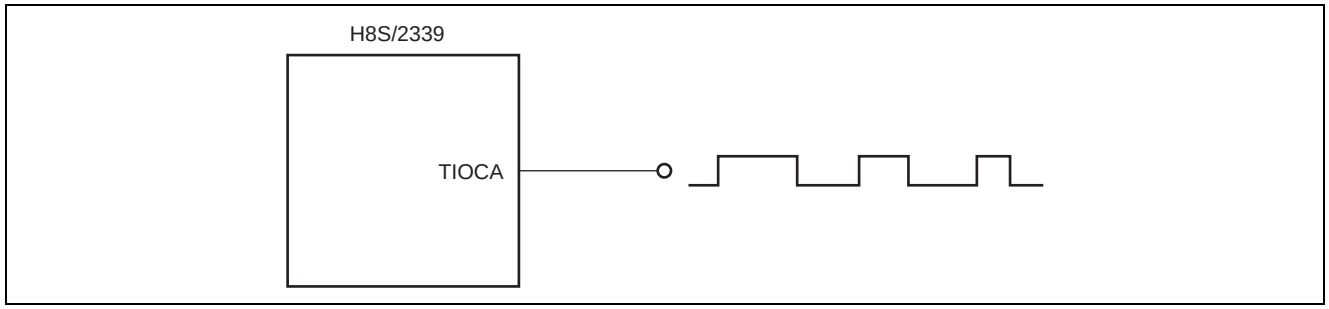


Figure 1 Example of PWM Waveform Output by TPU Buffer Operation

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Contents	
Operating frequency	Input clock:	19.6608 MHz
	System clock:	19.6608 MHz
	Peripheral module clock:	19.6608 MHz
	Bus master clock:	19.6608 MHz
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0)	
Development tool	HEW Version 3.01 (release 1)	
C/C++ compiler	H8S, H8/300 SERIES C/C++ Compiler Version 6.0.00.005 (from Renesas Technology Corp.)	
Compile option	-cpu = 2000a:24, -code = machinecode, -optimize = 1	

3. Description of Functions

Figure 2 shows a block diagram of the 16-bit timer pulse unit (TPU), and the following describes the registers of the TPU.

- Timer Control Register (TCR0)
  TCR sets the clearing condition and clock source of the timer counter, TCNT, for each channel.
- Timer Mode Register (TMDR0)
  TMDR sets the operating mode, normal operation or buffer operation, for each channel.
- Timer I/O Control Registers (TIOR0H and TIOR0L)
  TIOR controls output signals by setting the initial output value and output value in compare-match/input-capture operation for each TGR.
- Timer Interrupt Enable Register (TIER0)
  TIER enables or disables interrupts for each channel.
- Timer Status Register (TSR0)
  TSR indicates the statuses for each channel.
- Timer Counter (TCNT0)
  TCNT is a 16-bit counter that can be read or written to. Access to this counter must be in 16-bit units.
- Timer General Registers (four registers from TGR0A to TGR0D)
  TGR0A to TGR0D are 16-bit readable/writable registers that are used for output compare or input capture. Access to these registers must be in 16-bit units.
- Timer Start Register (TSTR)
  TSTR selects to start or stop the operation of TCNTs for channels 0 to 5.

Note The register names with “0” in the above description are channel 0 registers. Each channel has a set of such registers.

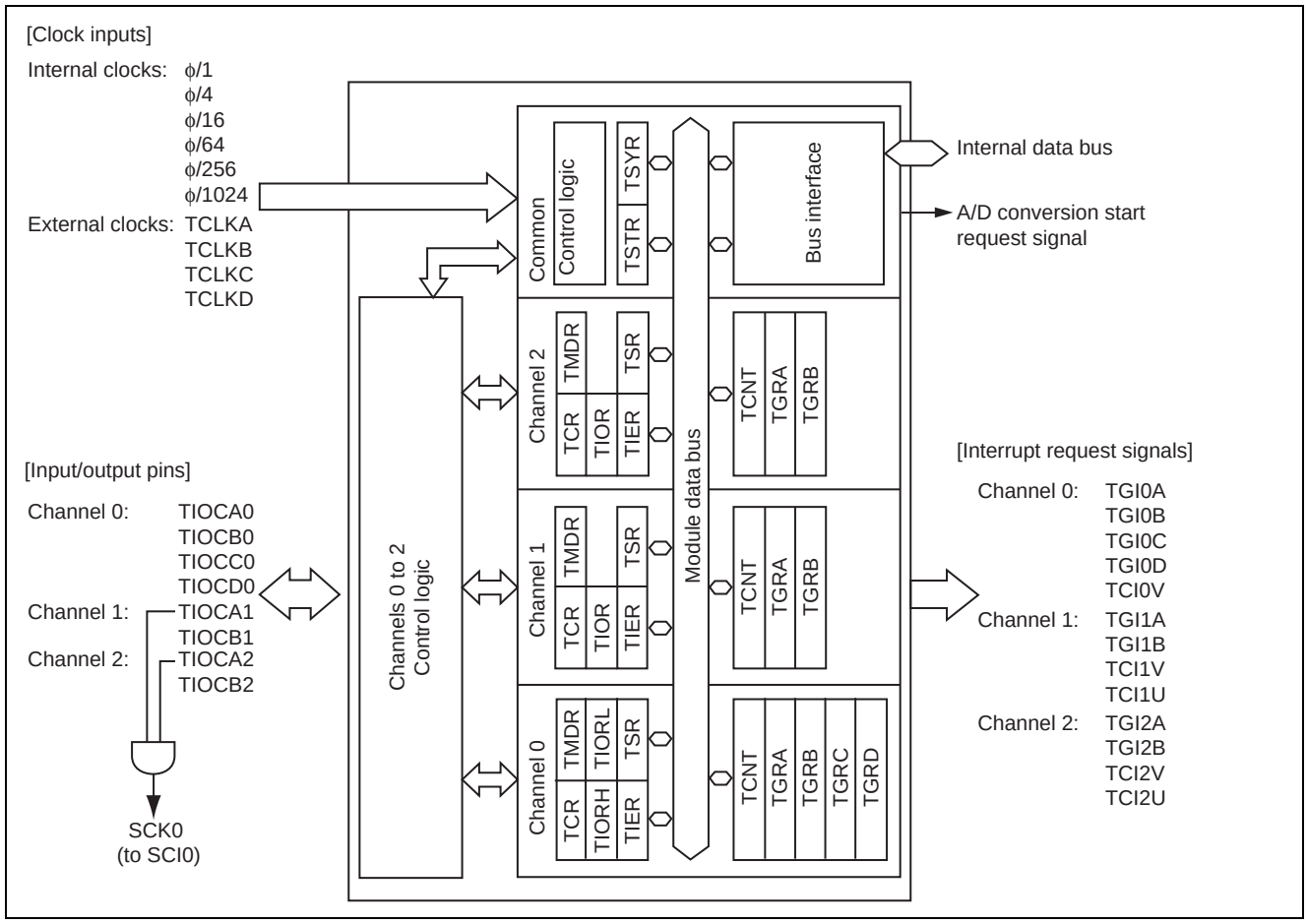


Figure 2 Block Diagram of TPU

4. Description of Operation

Figure 3 illustrates the operation of this sample task. PWM waveform is output based on TPU buffer operation through the hardware and software processing shown in the figure.

1. Channel 0 is set to PWM mode 1, and TGRA and TGRC are set to perform buffer operation. TCNT is cleared on compare-match B. A high level is output on compare-match A, and a low level on compare-match B.
2. When compare-match A occurs, output signal goes high and the value in the buffer register TGRC is transferred to TGRA at the same time. This operation is repeated each time a compare-match A occurs.
3. Although TGR0C is only set to H'0450 in this sample task, PWM pulses with different duty cycles can be output continuously by rewriting the TGR0C buffer (for example, H'0520 as is shown in the figure).

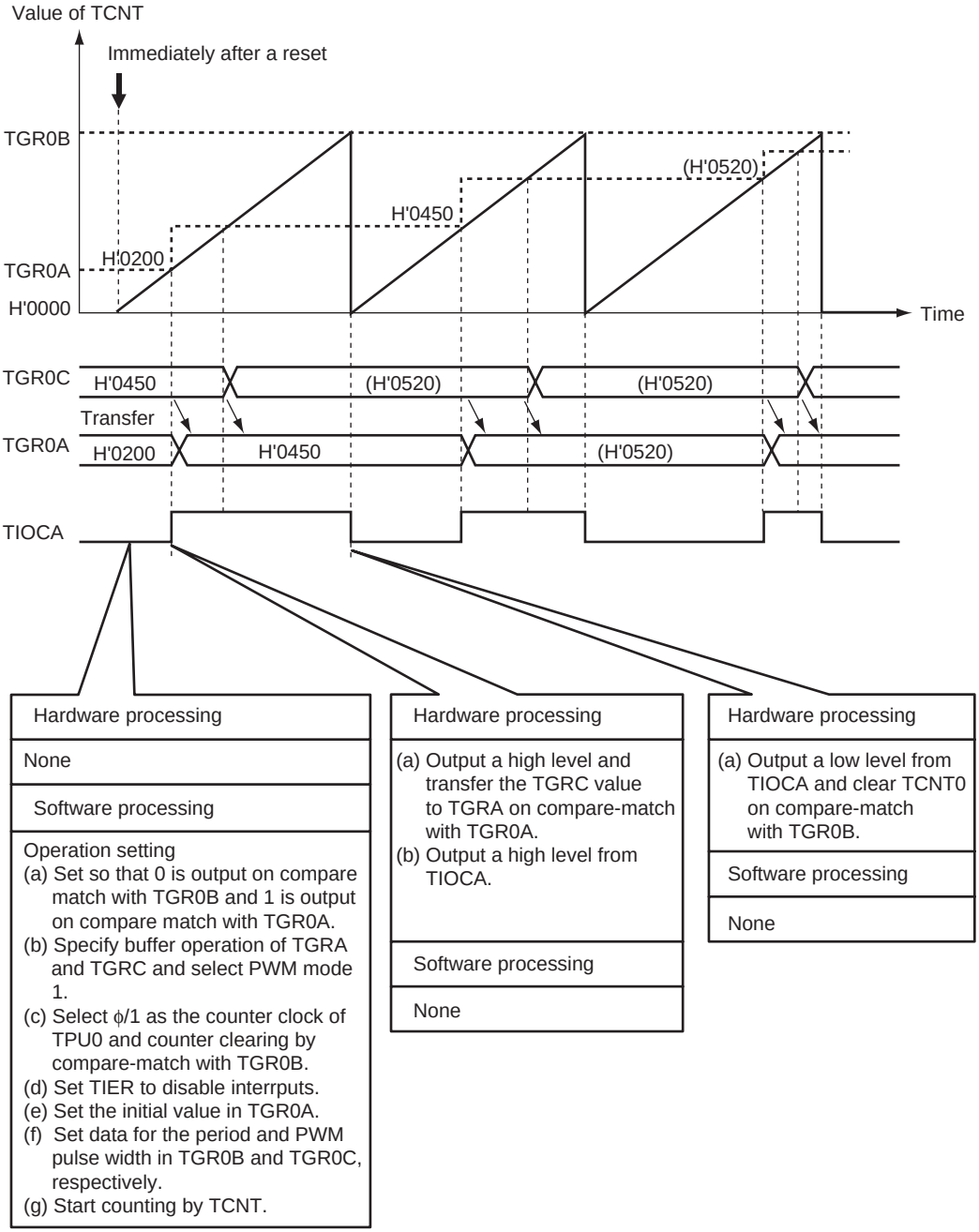


Figure 3 PWM Pulse Output Operation

5. Description of Software

5.1 Module

Table 2 describes the module of this sample task.

Table 2 Description of Module

Module Name	Label Name	Functions
Main routine	tpubfm	Selects buffer operation of TGRA and TGRC and outputs PWM waveform in PWM mode 1.

5.2 Arguments

Table 3 Description of Arguments

Label	Description	Data Length	Used in	I/O
pul_cyc1	The value of this argument is placed in TGR0B to set the counter reset period. This period is determined by: Period (ns) = (timer value +1) × clock (ϕ) period	1 word	Main routine	Input
pul_cyc2	The value of this argument is placed in TGR0C, which stores the data that is transferred to TGR0A on compare-match A. PWM high-pulse width (ns) = period – (pul_cyc2 +1)	1 word	Main routine	Input

5.3 Internal Registers

Table 4 Description of Internal Registers

Register Name		Function	Address	Setting
TSR0	TCFV	Timer Status Register (Overflow Flag) TCFV = 0 indicates that TCNT has not overflowed. TCFV = 1 indicates that TCNT has overflowed. (TCNT value has changed from H'FFFF to H'0000.)	H'FFFFD5 Bit 4	0
	TGFB	Timer Status Register (Input Capture/Output Compare Flag B) TGFB = 0 indicates TCNT ≠ TGFB. TGFB = 1 indicates TCNT = TGFB.	H'FFFFD5 Bit 1	0
	TGFA	Timer Status Register (Input Capture/Output Compare Flag A) TGFA = 0 indicates TCNT ≠ TGFA. TGFA = 1 indicates TCNT = TGFA.	H'FFFFD5 Bits 0	0

Register	Name	Function	Address	Setting
TMDR0	BFB	Timer Mode Register (Buffer Operation B) BFB = 0 selects normal operation of TGRB. BFB = 1 selects buffered operation of TGRB and TGRD.	H'FFFFD1 Bit 5	0
	BFA	Timer Mode Register (Buffer Operation A) BFA = 0 selects normal operation of TGRA. BFA = 1 selects buffered operation of TGRA and TGRC.	H'FFFFD1 Bit 4	1
	MD3 MD2 MD1 MD0	Timer Mode Register (Mode 3 to 0) When MD3 to MD0 = 0000, the TPU operates in normal mode. When MD3 to MD0 = 0010, the TPU operates in PWM mode 1.	H'FFFFD1 Bits 3 to 0	0,0,1,0
TCR0	CCLR1 CCLR0	Timer Control Register (Counter Clear 1, 0) When CCLR1 and CCLR0 = 00, clearing of TCNT is disabled. When CCLR1 and CCLR0 = 10, TCNT is cleared on compare-match or input capture of TGRB.	H'FFFFD0 Bits 6,5	1,0
	CKEG1 CKEG0	Timer Control Register (Clock Edge 1, 0) When CKEG1 and CKEG0 = 00, TCNT counts the rising edges. When CKEG1 and CKEG0 = 01, TCNT counts the falling edges.	H'FFFFD0 Bits 4,3	0,1
	TPSC2 TPSC1 TPSC0	Timer Control Register (Timer Prescaler 2, 1, 0) When TPSC2 to TPSC0 = 000, the clock source of TCNT is ϕ/1. When TPSC2 to TPSC0 = 111, TCNT counts overflow or underflow of TCNT2.	H'FFFFD0 Bits 2 to 0	0,0,0
TGR0A		Timer General Register A 16-bit register that is used for output compare or input capture	H'FFFFD8 Bits 15 to 0	H'0200
TGR0B		Timer General Register B 16-bit register that is used for output compare or input capture	H'FFFFDA Bits 15 to 0	H'0600
TGR0C		Timer General Register C 16-bit register that is used for output compare or input capture	H'FFFFDC Bits 15 to 0	H'0450
TIOR0H	IOB3 to IOB0	Timer I/O Control Register (I/O Control B3 to B0) These bits set the output level on compare-match with TGRB.	H'FFFFD2 Bits 7 to 4	0,1,0,1
	IOA3 to IOA0	Timer I/O Control Register (I/O Control A3 to A0) These bits set the output level on compare-match with TGRA.	H'FFFFD2 Bits 3 to 0	0,0,1,0

Register Name		Function	Address	Setting
TIER0	TTGE	Timer Interrupt Enable Register (A/D Conversion Start Request Enable) When TTGE = 0, generation of A/D conversion start requests is disabled. When TTGE = 1, generation of A/D conversion start requests is enabled.	H'FFFFD4 Bit 7	0
	TCIEV	Timer Interrupt Enable Register (Overflow Interrupt Enable) When TCIEV = 0, interrupt requests (TCIV) by the TCFV flag are disabled. When TCIEV= 1, interrupt requests (TCIV) by the TCFV flag are enabled.	H'FFFFD4 Bit 4	0
	TGIED	Timer Interrupt Enable Register (TGFD Interrupt Enable D) When TGIED = 0, interrupt requests (TGID) by the TGFD flag are disabled. When TGIED = 1, interrupt requests (TGID) by the TGFD flag are enabled.	H'FFFFD4 Bit 3	0
	TGIEC	Timer Interrupt Enable Register (TGFD Interrupt Enable C) When TGIEC = 0, interrupt requests (TGIC) by the TGFC flag are disabled. When TGIEC = 1, interrupt requests (TGIC) by the TGFC flag are enabled.	H'FFFFD4 Bit 2	0
	TGIEB	Timer Interrupt Enable Register (TGFD Interrupt Enable B) When TGIEB = 0, interrupt requests (TGIB) by the TGFB flag are disabled. When TGIEB = 1, interrupt requests (TGIB) by the TGFB flag are enabled.	H'FFFFD4 Bit 1	0
	TGIEA	Timer Interrupt Enable Register (TGFD Interrupt Enable A) When TGIEA = 0, interrupt requests (TGIA) by the TGFA flag are disabled. When TGIEA = 1, interrupt requests (TGIA) by the TGFA flag are enabled.	H'FFFFD4 Bit 0	0
TSTR		Timer Start Register A bit of this register starts/stops the operation of TCNT for the corresponding channel (channels 0 to 5).	H'FFFFC0 Bits 5 to 0	H'01

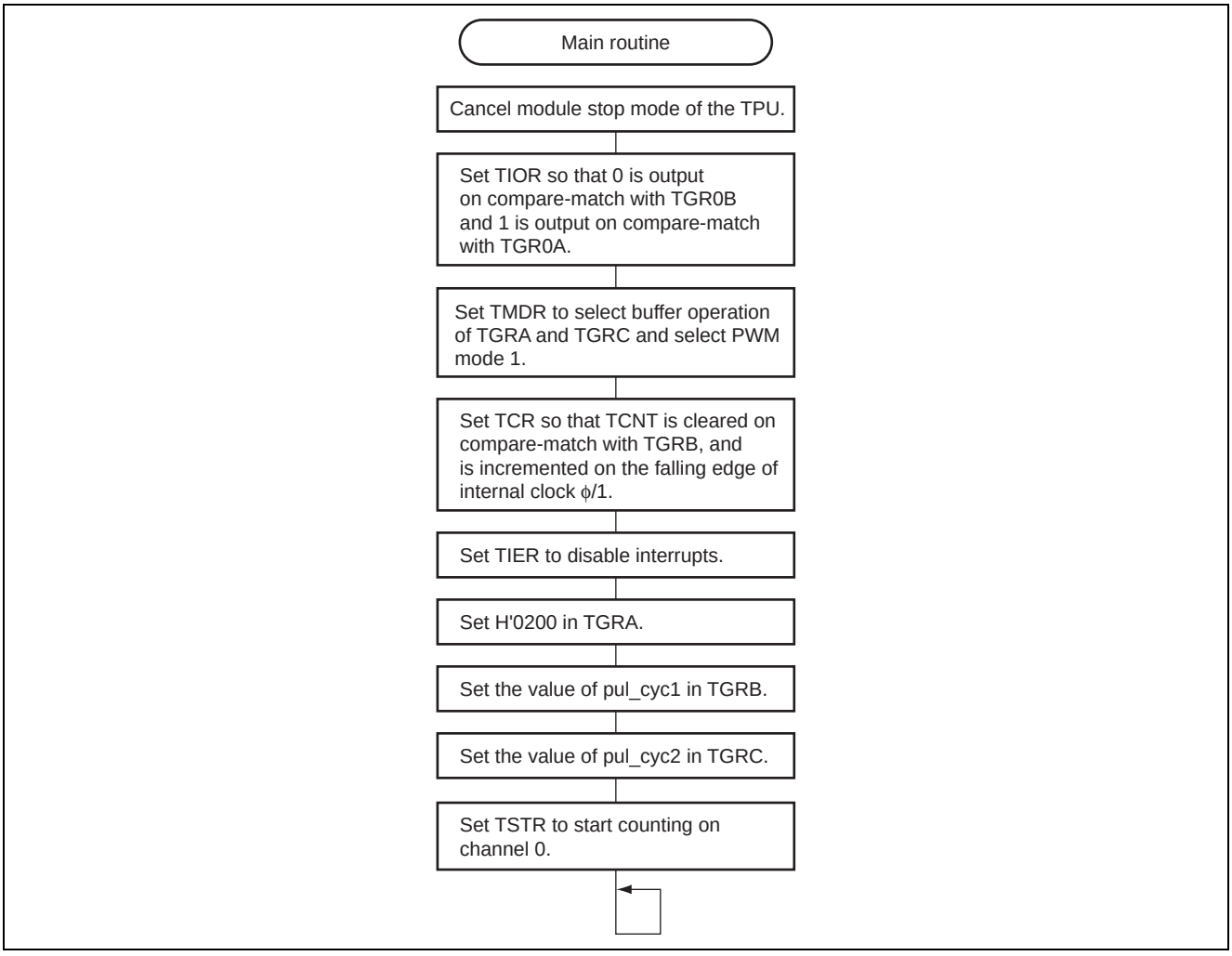
5.4 RAM Usage

Table 5 Description of RAM

Label Name	Function (Setting Used in This Sample Task)	Data Length	Used In
pul_cyc1	Stores the data to be set in TGR0B. (H'0600)	1 word	Main routine
pul_cyc2	Stores the data to be set in TGR0C. (H'0450)		

6. Flowchart

6.1 Main Routine



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		Description	
Rev.	Date	Page	Summary
1.00	Mar.09.05	—	First edition issued

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