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H8S Family
Duplex Transmission

Introduction
Transmits and receives 1-byte data, synchronizing with a clock between the H8S/2339 (master) and H8S/2215 (slave).

Target Device
H8S/2339

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1. Specifications

1. As shown in figure 1, this function transmits and receives 1-byte data between an H8S/2339 and H8S/2215.
2. Data is transmitted and received in the clock synchronous format. The master H8S/2339 provides the clock to the slave H8S/2215.
3. The H8S/2339 transmits data to and receives data from the H8S/2215 simultaneously.

![Block Diagram of Clock Synchronous SCI by H8S/2339](image-url)
2. Description of Functions

1. This sample task transmits and receives data, using SCI2. Port A is used for the communication control pins (RRQ and SRQ).

   A. The block diagram of SCI to be used by the sample task is shown in figure 2. This sample task uses the following functions of SCI to perform transmission and reception simultaneously.
   - Function that performs serial data communication, synchronizing with the clock (clock synchronous mode)
   - Function that performs transmission and reception simultaneously (duplex transmission function)
   - Function that generates an interrupt at completion of reception (RXI interrupt)

![Figure 2 SCI Block Diagram](image-url)
3. **Principles of Operation**

The principles of operations used of this task are shown in figure 3. This task performs software and hardware processing at the timing shown in figure 3 to interface with an H8S/2215 (slave).

![Figure 3 Principles of Operations Used for Duplex Transmission]

**Figure 3** Principles of Operations Used for Duplex Transmission
4. Description of Software

1. Description of Modules

<table>
<thead>
<tr>
<th>Module Name</th>
<th>Label Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>simtrmn</td>
<td>Performs initial setting of SCI and controls transmission and reception.</td>
</tr>
<tr>
<td>Data reception completion</td>
<td>rxend</td>
<td>Starts up by an RXI interrupt and receives data.</td>
</tr>
</tbody>
</table>

2. Description of Argument

<table>
<thead>
<tr>
<th>Label Name</th>
<th>Function</th>
<th>Data Length</th>
<th>Used in</th>
<th>I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>revend</td>
<td>Flag indicating reception completion</td>
<td>unsigned char</td>
<td>Data reception completion</td>
<td>Output</td>
</tr>
<tr>
<td></td>
<td>1: Reception completed</td>
<td></td>
<td>Main routine</td>
<td></td>
</tr>
<tr>
<td></td>
<td>0: Reception in progress</td>
<td></td>
<td></td>
<td>Input</td>
</tr>
</tbody>
</table>

3. Description of Internal Registers Used

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Function</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>SMR2</td>
<td>Sets the SCI mode (clock synchronous), the transfer format, and selected clock to the baud rate generator (φ clock input).</td>
<td>Main routine</td>
</tr>
<tr>
<td>SCR2</td>
<td>Enables an interrupt (RXI) and SCI transmission and reception.</td>
<td>Main routine</td>
</tr>
<tr>
<td>SSR2</td>
<td>Clears TDRE to instruct transmission to start.</td>
<td>Main routine</td>
</tr>
<tr>
<td>RDR2</td>
<td>Sets data received from an H8S/2215 (slave).</td>
<td>Data reception completion</td>
</tr>
<tr>
<td>TDR2</td>
<td>Sets data to be transmitted to an H8S/2215 (slave).</td>
<td>Main routine</td>
</tr>
<tr>
<td>BRR2</td>
<td>Sets the transfer rate.</td>
<td>Main routine</td>
</tr>
<tr>
<td>PADDR</td>
<td>Sets I/O of port A.</td>
<td>Main routine</td>
</tr>
<tr>
<td>PADR</td>
<td>Operates the RRQ and SRQ pins.</td>
<td>Main routine</td>
</tr>
<tr>
<td>MSTPCR</td>
<td>Cancels the SCI module stop mode.</td>
<td>Main routine</td>
</tr>
</tbody>
</table>

4. RAM Usage

Table below describes RAM usage in this sample task.

<table>
<thead>
<tr>
<th>Label Name</th>
<th>Function</th>
<th>Data Length</th>
<th>Used in</th>
</tr>
</thead>
<tbody>
<tr>
<td>rvdata</td>
<td>Sets received data.</td>
<td>unsigned char</td>
<td>Main routine</td>
</tr>
<tr>
<td>trdata</td>
<td>Sets data to be transmitted (in this sample task: H’32).</td>
<td>unsigned char</td>
<td>Main routine</td>
</tr>
</tbody>
</table>
5. PAD

1. Main Routine

```
while (P_PA.PORT.BIT.B1 = = 1)
  Set SCR2 to enable receive data full interrupt and to receive mode.
  while (!(P_SCI2.SSR.BYTE & 0x80))
    while (revend == 0)
      while (1)
        while (i < 500, increment i).
        if i < 4, increment i.
        while (P_PA.PORT.BIT.B1 = = 1)
          Output low from RQ pin.
        while (P_SCI2.SSR.BYTE & 0x80)
          Output high from RQ pin.
        Set transmit data in TDR2.
        Enable transmission.
        while (revend == 0)
          Store receive data in RAM.
          Clear TE and RE, and end transmission
        while (1)
      Set RIE of SCR2 to enable RXI and ER1 interrupts.
      Set the interrupt level to IPRF.
      Clear i flag to enable an interrupt.
      Set SCR2 to enable receive data full interrupt and to receive mode.
      Set PADR and PADDR.
      Clear TE and RE bits of SCR2 to 0.
      Select clock synchronous mode by SMR2.
      Set LSB-first transmission by SCMR2.
      Set transfer rate to BBR2.
      Clear I flag to enable an interrupt.
      Set PADR and PADDR.
      while (i < 4, increment i).
      if i < 4, increment i.
      Output low from RQ pin.
```

2. Data Reception Completion

```
while ((P_PA.PORT.BIT.B1 = = 1)
  Output low from RQ pin.
while ((P_SCI2.SSR.BYTE & 0x80))
  Output high from RQ pin.
Set transmit data in TDR2.
Enable transmission.
while (revend == 0)
  Store receive data in RAM.
  Clear TE and RE, and end transmission
while (1)
Set revend flag.
Clear reception completion status flag.
```
### Revision Record

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Feb.17.05</td>
<td></td>
<td>—</td>
<td>First edition issued</td>
</tr>
</tbody>
</table>

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