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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# H8S Family

## Data Transfer in the Single-Address Mode

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### Introduction

Uses the DMAC single-address mode to transfer data to an external device (H8S/2215). DMAC is started up at a falling edge of an external signal.

### Target Device

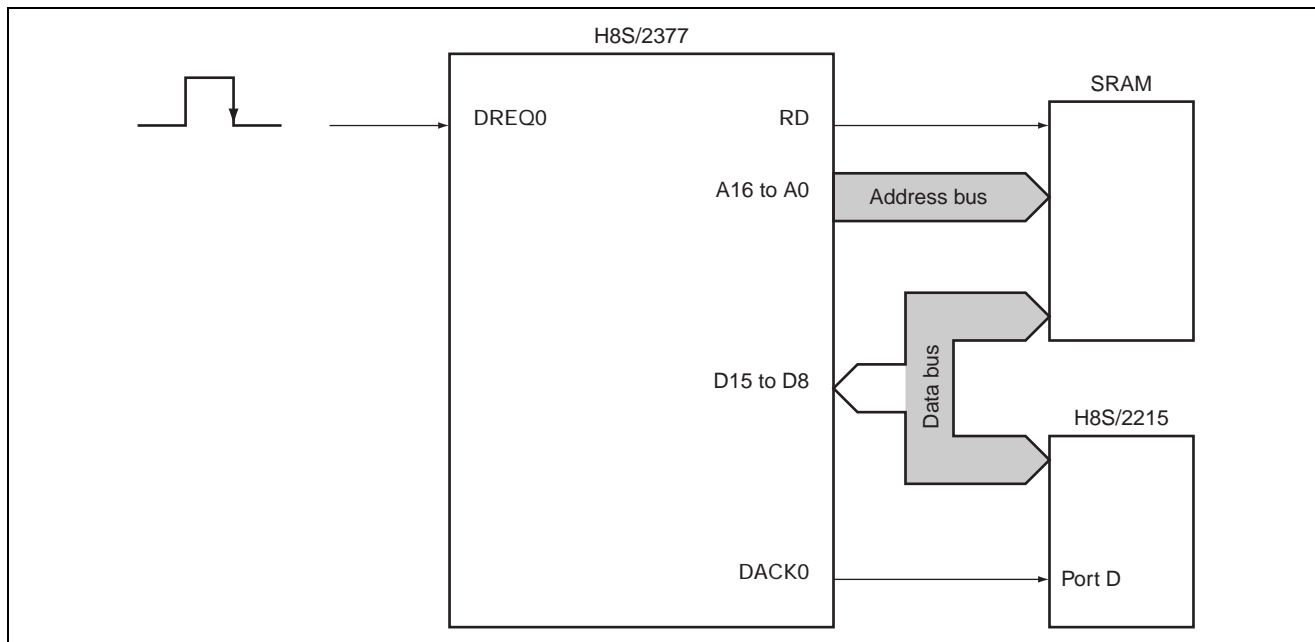
H8S/2377

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## 1. Specifications

1. As shown in figure 1, this sample task uses DMAC single-address mode to transfer data between the external space specified by a transfer source address or transfer destination address, and an external device that is selected by a DACK0 strobe independently of the address.
2. DMAC starts up at detection of a falling edge of an external signal.



**Figure 1 Data Bus in the Single-Address Mode**

## 2. Applicable Conditions

**Table 1 Applicable Conditions**

Item	Description
Operating frequency	Input clock: 19.6608 MHz System clock: 19.6608 MHz Peripheral module clock: 19.6608 MHz External bus clock: 19.6608 MHz
Operating mode	Mode 4 (MD2 = 1, MD1 = 0, MD0 = 0)
Development tool	High-performance Embedded Workshop version 3.01.02
C/C++ compiler	H8S, H8/300 series C/C++ compiler version 6.00.02 manufactured by Renesas Technology Corp.
Compiler options	-cpu=200a:24, -code=machinecode, -optimize=1, -regparam=3, -speed=(register,shift,struct,expression)

**Table 2 Applicable Conditions**

<b>Address</b>	<b>Section Name</b>	<b>Description</b>
H"000000	CV1	Reset vector
H"000144	CV2	DMAC DMTEND0B interrupt vector
H"001000	P	Program area
H'FF6000	B	RAM area

### 3. Description of Functions

1. This sample task uses the DMAC single-address mode (idle mode specification) to transfer data to the external device (H8S/2215) from the external memory (SRAM).

A. The block diagram of DMAC to be used in this sample task is shown in figure 2.

This sample task uses the following DMAC functions to transfer data blocks:

- Function that starts up DMAC on an external request (DMAC startup by DREQ0)
- Function that transfers one byte or one word between the external memory and external device per transfer request as many times as specified (single-address mode)

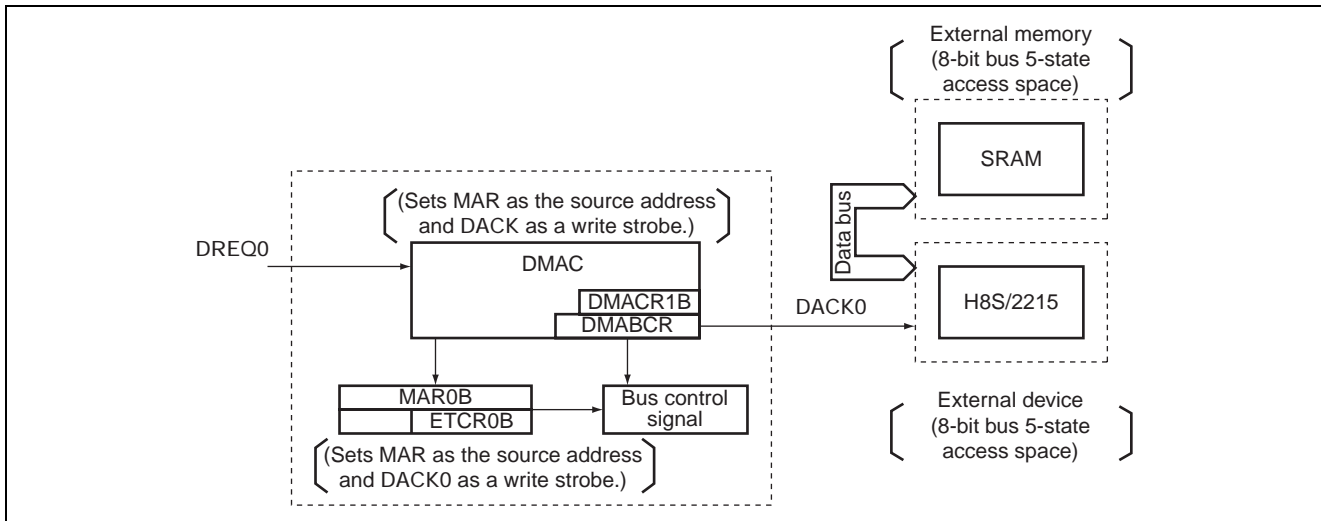


Figure 2 Block Diagram of DMA Controller

### 4. Principles of Operation

The principles of operations used are shown in figure 3. This sample task performs H8S/2377 hardware processing and software processing as shown in figure 3 to transfer one byte to the 8-bit 5-state access space in the external device from the external 8-bit 5-state access space.

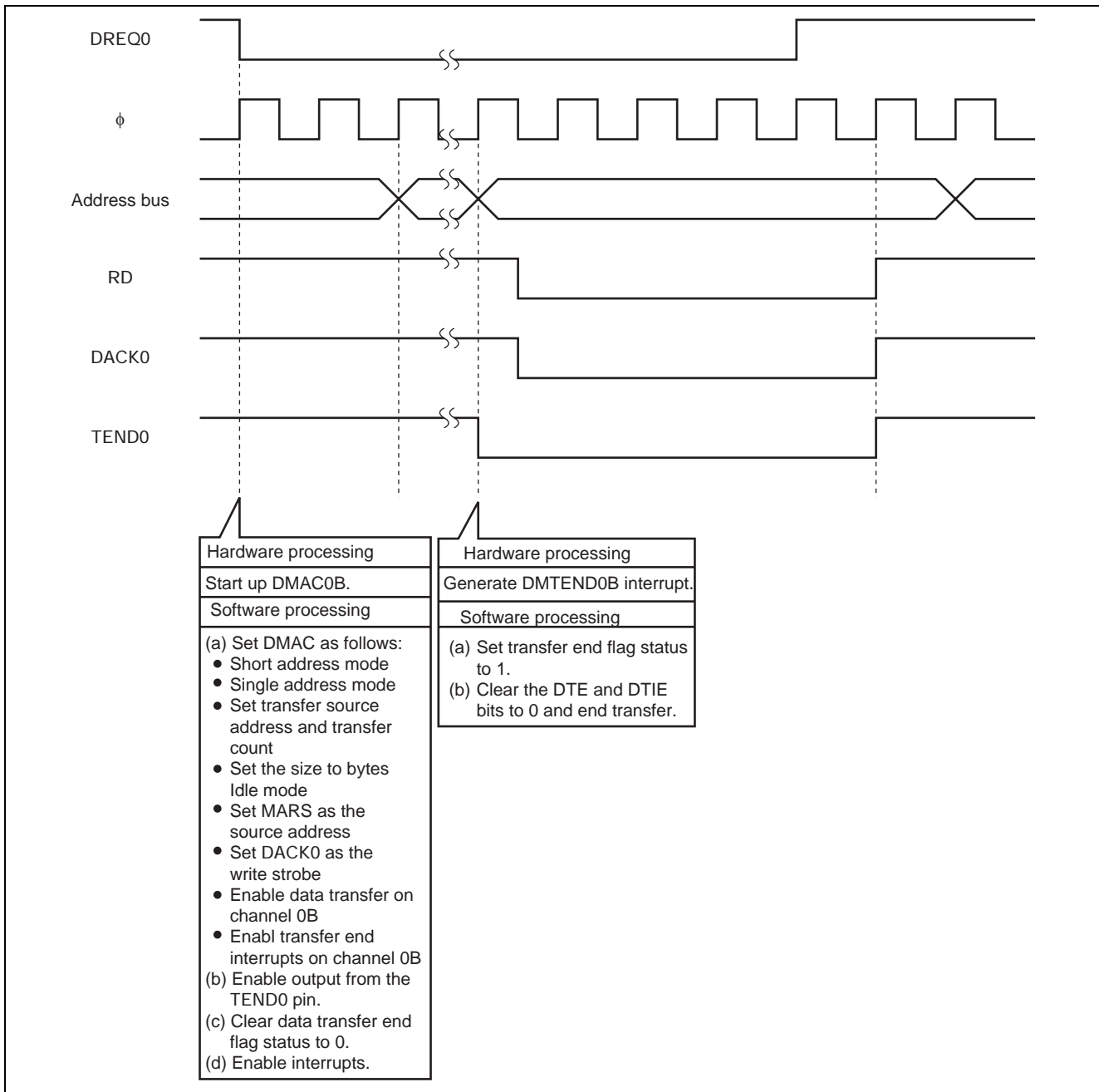


Figure 3 Principles of Operations Used of Transfer in the Single-Address Mode (Byte Read)

### 5. Description of Software

#### 5.1 Description of Functions

Function Name	Function
init	Initialization routine Makes condition code register (CCR) and clock settings, clears module stop mode, and calls functions Bsclnit and main.
Bsclnit	Bus state controller (BSC) setting Bus settings.
main	Main routine Performs initial setting of DMAC.
Dmtend0b_int	Data transfer end interrupt Sets the transfer end flag.

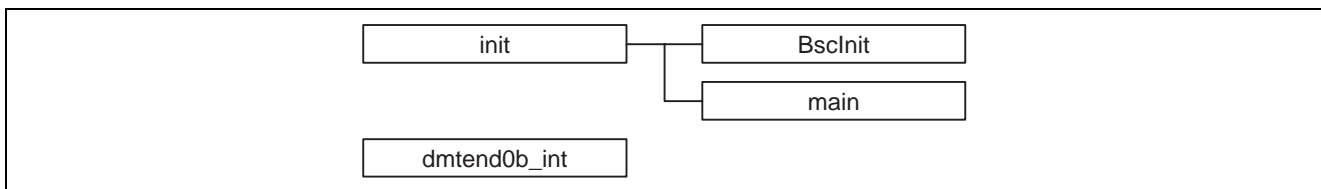


Figure 4 Hierarchy Structure

#### 5.2 Description of Arguments

No arguments are used in this sample task.

#### 5.3 Description of Internal Registers Used

- System clock control register (SCKCR) Address: H'FFFF3B

Bit	Bit Name	Set Value	Description
2	SCK2	0	System clock select 2 to 0
1	SCK1	0	000: Selected division ratio is 1/1.
0	SCK0	0	

- PLL control register (PLLCR) Address: H'FFFF45

Bit	Bit Name	Set Value	Description
1	STC1	0	Frequency multiplication factor used by the PLL circuit
0	STC0	0	00: 1/1



- Module stop control register H, L (MSTPCRH, MSTPCRL)      Address: H'FFFF40, H'FFFF41

Bit	Bit Name	Set Value	Description
15	ACSE	0	All-module-clock-stop mode enable 0: All-module-clock-stop mode disabled 1: All-module-clock-stop mode enabled
14	MSTP14	0	EXDMA controller (EXDMAC) 0: Takes EXDMAC out of module stop mode 1: Sets EXDMAC in module stop mode
13	MSTP13	0	DMA controller (DMAC) 0: Takes DMAC out of module stop mode 1: Sets DMAC in module stop mode
12	MSTP12	0	Data transfer controller (DTC) 0: Takes DTC out of module stop mode 1: Sets DTC in module stop mode
11	MSTP11	0	16-bit timer-pulse unit (TPU) 0: Takes TPU out of module stop mode 1: Sets TPU in module stop mode
10	MSTP10	0	Programmable pulse generator (PPG) 0: Takes PPG out of module stop mode 1: Sets PPG in module stop mode
9	MSTP9	0	D/A converter (channels 0 and 1) 0: Takes D/A converter (channels 0 and 1) out of module stop mode 1: Sets D/A converter (channels 0 and 1) in module stop mode
8	MSTP8	0	D/A converter (channels 2 and 3) 0: Takes D/A converter (channels 2 and 3) out of module stop mode 1: Sets D/A converter (channels 2 and 3) in module stop mode
7	MSTP7	0	D/A converter (channels 4 and 5) 0: Takes D/A converter (channels 4 and 5) out of module stop mode 1: Sets D/A converter (channels 4 and 5) in module stop mode
6	MSTP6	0	A/D converter 0: Takes A/D converter out of module stop mode 1: Sets A/D converter in module stop mode
5	MSTP5	0	Serial communication interface 4 (SCI_4) 0: Takes SCI_4 out of module stop mode 1: Sets SCI_4 in module stop mode
4	MSTP4	0	Serial communication interface 3 (SCI_3) 0: Takes SCI_3 out of module stop mode 1: Sets SCI_3 in module stop mode
3	MSTP3	0	Serial communication interface 2 (SCI_2) 0: Takes SCI_2 out of module stop mode 1: Sets SCI_2 in module stop mode
2	MSTP2	0	Serial communication interface 1 (SCI_1) 0: Takes SCI_1 out of module stop mode 1: Sets SCI_1 in module stop mode
1	MSTP1	0	Serial communication interface 0 (SCI_0) 0: Takes SCI_0 out of module stop mode 1: Sets SCI_0 in module stop mode

Bit	Bit Name	Set Value	Description
0	MSTP0	0	8-bit timer (TMR) 0: Takes TMR out of module stop mode 1: Sets TMR in module stop mode

- Extension module stop control register H, L (EXMSTPCRH, EXMSTPCRL) Address: H'FFFF43

Bit	Bit Name	Set Value	Description
4	MSTP20	0	I <sup>2</sup> C bus interface 2_1 (IIC2_1) 0: Takes IIC2_1 out of module stop mode 1: Sets IIC2_1 in module stop mode
3	MSTP19	0	I <sup>2</sup> C bus interface 2_0 (IIC2_0) 0: Takes IIC2_0 out of module stop mode 1: Sets IIC2_0 in module stop mode

- System control register (SYSCR) Address: H'FFF3D

Bit	Bit Name	Set Value	Description
0	RAME	1	RAM enable 0: Disables internal RAM 1: Enables internal RAM

- Port function control register 0 (PFCR0) Address: H'FFFE32

Bit	Bit Name	Set Value	Description
7	CS7E	1	These bits enable or disable the corresponding CS <sub>n</sub> output. 0: Pin is designated as I/O port 1: Pin is designated as CS <sub>n</sub> output pin (n = 7 to 0)
6	CS6E	1	
5	CS5E	1	
4	CS4E	1	
3	CS3E	1	
2	CS2E	1	
1	CS1E	1	
0	CS0E	1	

- Port function control register 1 (PFCR1) Address: H'FFFE33

Bit	Bit Name	Set Value	Description
7	A23E	1	Address A23 to A16 enable
6	A22E	1	These bits enable or disable address signals A23 to A16. 0: DR output when PAnDDR = 1 (n = 7 to 1) 1: Amm output when PAnDDR = 1 (n = 7 to 0, mm = 23 to 16)
5	A21E	1	
4	A20E	1	
3	A19E	1	
2	A18E	1	H'FF: Enable address outputs A23 to A16
1	A17E	1	
0	A16E	1	

- Port function control register 1 (PFCR2) Address: H'FFFE34

Bit	Bit Name	Set Value	Description
3	ASOE	1	AS output enable 0: PF6 is designated as I/O port 1: PF6 is designated as AS output pin
2	LWROE	1	LWR output enable 0: PF3 is designated as I/O port 1: PF3 is designated as LWR output pin

- Port A data direction register (PADDR) Address: H'FFFE29  
Function: Sets PA7 to PA0 pins to address output pins.  
Set value: H'FF
- Port B data direction register (PBDDR) Address: H'FFFE2A  
Function: Sets PB7 to PB0 pins to address output pins.  
Set value: H'FF
- Port C data direction register (PCDDR) Address: H'FFFE2B  
Function: Sets PC7 to PC0 pins to address output pins.  
Set value: H'FF
- Port F data direction register (PFDDR) Address: H'FFFE2E  
Function: Sets PF7 to  $\phi$  output. Sets PF6 to PF0 pins to input pins.  
Set value: H'80
- Port G data direction register (PGDDR) Address: H'FFFE2F  
Function: Sets PG3 to PG0 pins to CS3 to CS0 input pins.  
Set value: H'0F
- Port H data direction register (PHDDR) Address: H'FFFE74  
Function: Sets PH3 to PH0 pins CS7 to CS4 input pins.  
Set value: H'0F
- Bus width control register (ABWCR) Address: H'FFFE00  
Function: Sets areas 7 to 3, 1, and 0 to 16-bit access space, and area 2 to 8-bit access space.  
Set value: H'04
- Access state control register (ASTCR) Address: H'FFFE01  
Function: Sets areas 7 to 0 to 3-state access space.  
Set value: H'FF
- Wait control register A (WTCRA) Address: H'FFFE02  
Function: Sets the number of program wait states. Areas 7 and 6 are set to 7 states, and areas 5 and 4 are set to 3 states.  
Set value: H'7733
- Wait control register B (WTCRB) Address: H'FFFE04  
Function: Sets the number of program wait states. Areas 3, and 2 are set to 1 state, and areas 1 and 0 are set to 2 states.  
Set value: H'1122

- Read strobe timing control register (RDNCR)                      Address: H'FFFE66  
Function: Sets the RD negation timing at the end of the read cycle when one of areas 7 to 0 is read.  
Set value: H'00

- Bus control register 1 (BCR)                                      Address: H'FFFECC

Bit	Bit Name	Set Value	Description
15	BRLE	0	External bus release enable/disable 0: Disables external bus release 1: Enables external bus release
12	IDLC	1	Number of Idle cycle states selection Specifies the number of states in the idle cycles set by ICIS2, ICIS1, and ICIS0. 0: The idle cycle comprises 1 state 1: The idle cycle comprises 2 states
11	ICIS1	1	Idle cycle insertion 1 Specifies whether or not to insert an idle cycle between the bus cycles when consecutive external read cycles are performed for different areas. 0: Does not insert an idle cycle 1: Inserts an idle cycle
10	ICIS0	1	Specifies whether or not to insert an idle cycle between the bus cycles when an external read cycle and external write cycle are performed consecutively. 0: Does not insert an idle cycle 1: Inserts an idle cycle
8	WAITE	1	WAIT pin enable/disable 0: Disables wait input from the WAIT pin The WAIT pin can be used as I/O port. 1: Enables wait input from the WAIT pin
2	ICIS2	0	Idle cycle insertion 2 Specifies whether or not to insert an idle cycle between the bus cycles when an external write cycle and external read cycle are performed consecutively. 0: Does not insert an idle cycle 1: Inserts an idle cycle

- Memory address register\_0B (MAR\_0B) at address H'FFFEE8  
Function: Sets the transfer source address.  
Set value: H'00400000
- Execute transfer count register\_0B (ETCR\_0B) at address H'FFFEEE  
Function: Sets the number of transfer.  
Set value: H'01
- DMA terminal control register (DMATCR) at address H'FFFF21

Bit	Bit Name	Set Value	Function
4	TEE0	1	Transfer end pin enable 0 0: Disable TEND0 signal output 1: Enable TEND0 signal output

- DMA control register\_0B (DMACR\_0B) at address H'FFFF23

Bit	Bit Name	Set Value	Function
7	DTSZ	0	Data transfer size 0: Byte for one data size to be transferred 1: Word for one data size to be transferred
5	RPE	1	Repeat enable When the DTIE bit of DMABCR is 1: 0: Sequential mode 1: Idle mode
4	DTDIR	0	Data transfer direction When the SAE bit of DMABCR is 1: 0: MAR is the source address, and DACK0 is the write strobe 1: DACK0 is the read strobe, and MAR is the write destination address
3	DTF3	0	Data transfer factor 3 to 0
2	DTF2	0	0010: Activation source of data transfer is the falling edge of the DREQ0 signal.
1	DTF1	1	
0	DTF0	0	

- DMA band control register H, and L (DMABCRH, and DMABCRL) at addresses H'FFFF26, and H'FFFF27

Bit	Bit Name	Set Value	Function
14	FAE0	0	Full address enable 0 0: Short address mode 1: Full address mode
12	SAE0	1	Single address enable 0 0: Dual address mode 1: Single address mode
5	DTE0B	1	Data transfer enable 0B 0: Data transfer end 1: Data transfer enabled
1	DTIE0B	1	Data transfer end interrupt enable 0B 0: Disable transfer end interrupt 1: Enable transfer end interrupt

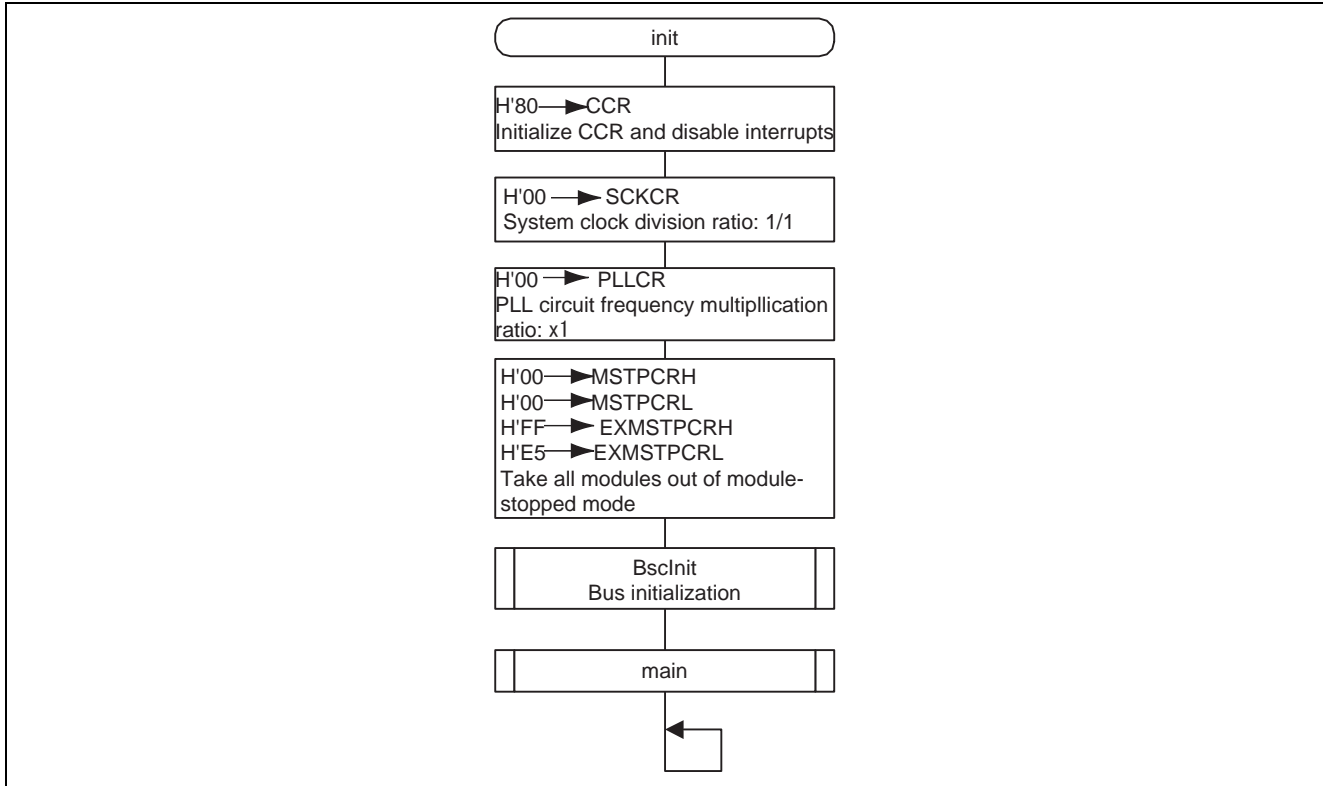
## 5.4 RAM Usage

Table below describes RAM usage in this sample task.

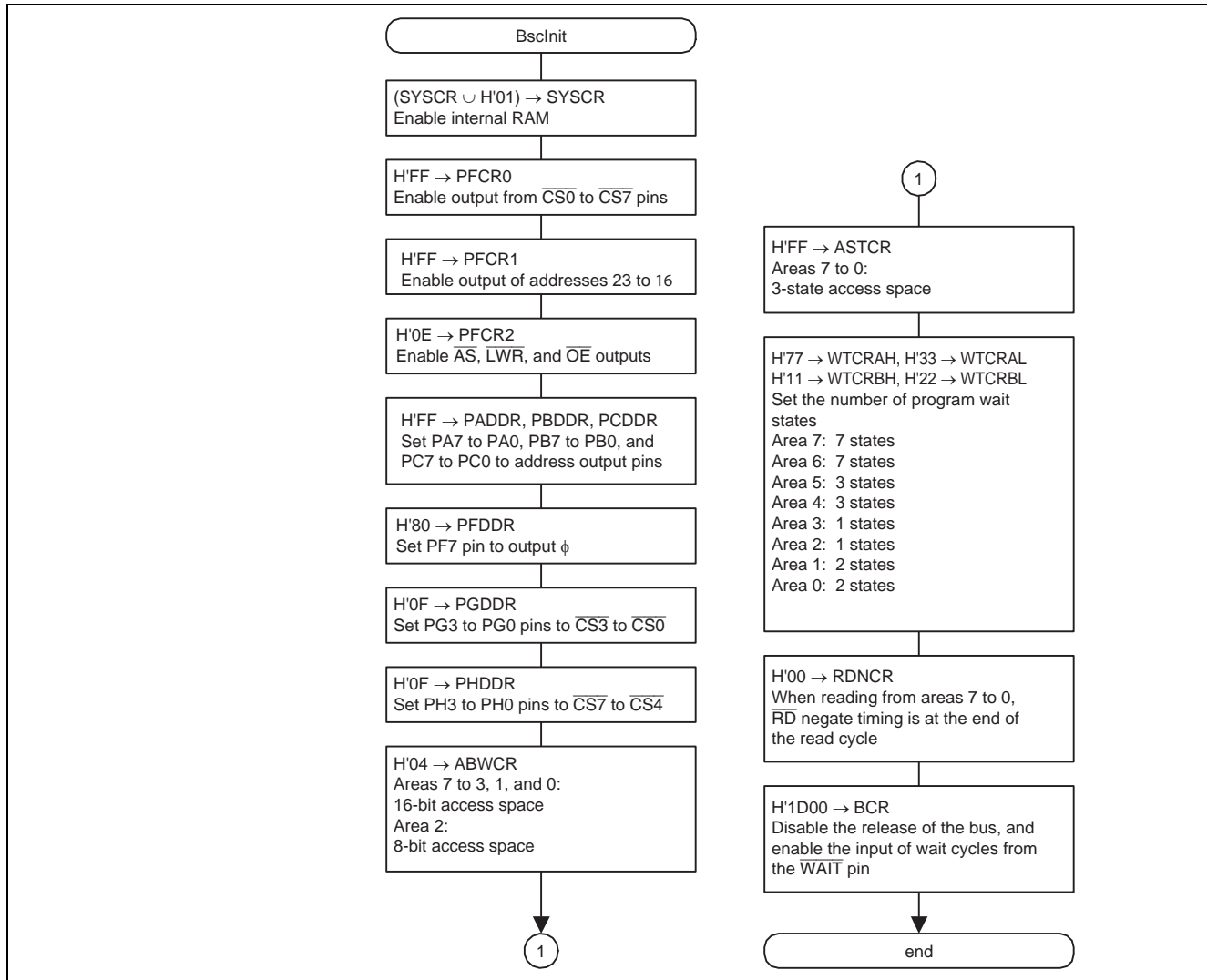
Label	Function	Data Length	Used in
status	Data transfer end flag 0: Data transfer in progress 1: Data transfer end	1 byte	main, dmtend0b_int

6. Flowchart

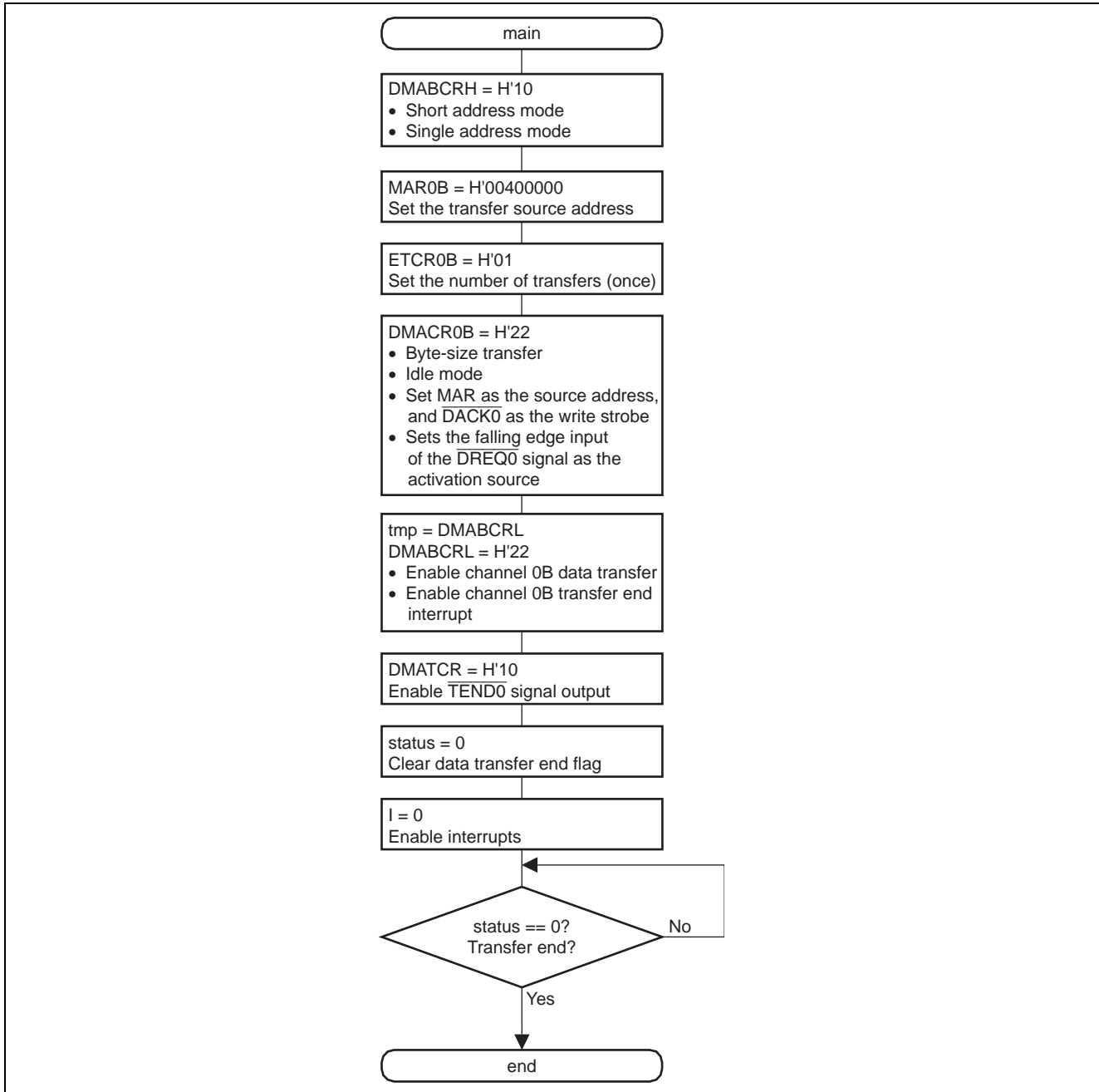
6.1 init Function



### 6.2 BscInIt Function

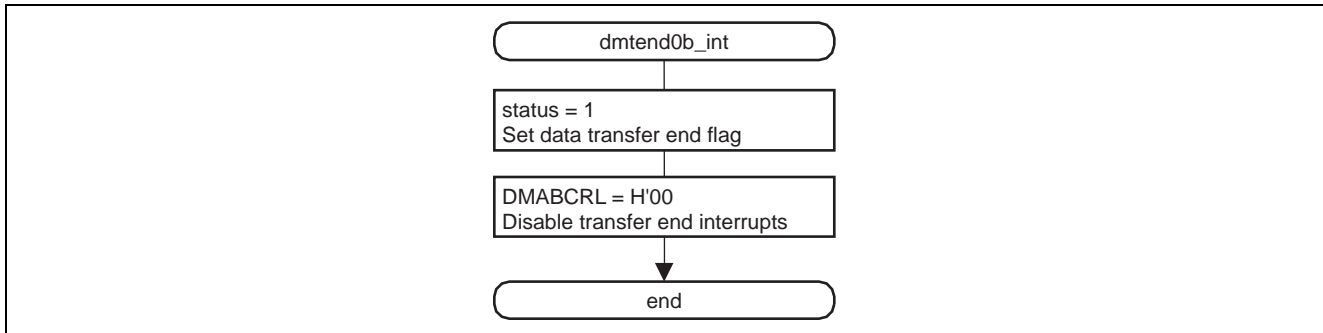


6.3 main Function





6.4 Data Transfer End



**Revision Record**

Rev.	Date	Description	
		Page	Summary
1.00	Feb.17.05	—	First edition issued

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