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H8/38602R Group

RTC Operation

Introduction

This application note discusses the time counting operation by the on-chip Realtime Clock (RTC).

Target Device

H8/38602R

Contents

1. Specifications

The RTC operation is performed. After the initial settings have been made, a mode transition is made to watch mode, and then to subactive mode in response to a one-second periodic interrupt request from the RTC. The day, hour, minute and second data are read and stored in on-chip RAM, after which a transition is made back to watch mode. The subclock is generated by the subclock oscillator circuit that uses a 32.768-kHz crystal resonator.

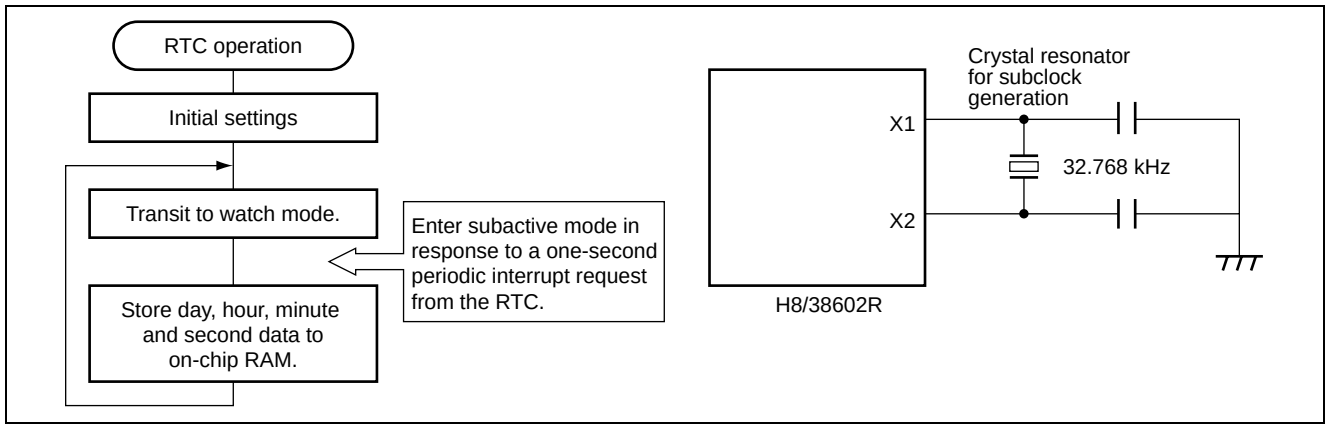


Figure 1 RTC Operation

2. Description of Functions

2.1 Functions

The H8/38602R's functions used in this sample task are described below.

2.1.1 RTC Function

The realtime clock (RTC) is a timer used to count times ranging from a second to a week. The RTC can generate periodic interrupts at intervals ranging from 0.25 seconds to a week. A block diagram of the RTC is shown in figure 2.

- Second Data Register/Free Running Counter Data Register (RSECDR)
  RSECDR counts the seconds and represents the count values in BCD code. The count range is decimal 00 to 59.
- Minute Data Register (RMINDR)
  RMINDR counts the minutes on the carry that occurs once per minute in RSECDR. RMINDR represents the count values in BCD code. The count range is decimal 00 to 59.
- Hour Data Register (RHRDR)
  RHRDR counts the hours on the carry that occurs once per hour in RMINDR and represents the count values in BCD code. The count range is either decimal 00 to 11 or 00 to 23 depending on the setting of the 12/24 bit in RTCCR1.
- Day-of-Week Data Register (RWKDR)
  RWKDR counts the day-of-week on the carry that occurs once per day in RHRDR. It represents the count values in binary code representing 0 to 6 using bits WK2 to WK0.
- RTC Control Register 1 (RTCCR1)
  RTCCR1 controls the start/stop, operating mode, interrupt generation timing and reset of the clock timer.
- RTC Control Register 2 (RTCCR2)
  RTCCR2 controls the periodic interrupts of the RTC for the week, day, hour, minute, one second, 0.5 seconds, and 0.25 seconds. If these interrupts are enabled, the corresponding flag in the RTC interrupt flag register (RTCFLG) is set to 1 when the interrupt occurs.
- Clock Source Select Register (RTCCSR)
  RTCCSR selects the clock source. When a clock other than 32.768 kHz is selected, the RTC operation is disabled and the module operates as an 8-bit free running counter. The start/stop of the free the running counter operation is controlled by the RUN bit in RTCCR1.
- RTC Interrupt Flag Register (RTCFLG)
  When an RTC interrupt occurs, the corresponding flag in RTCFLG is set. Each flag is not automatically cleared even if the interrupt is accepted. To clear the flag, a 0 should be written to the flag.

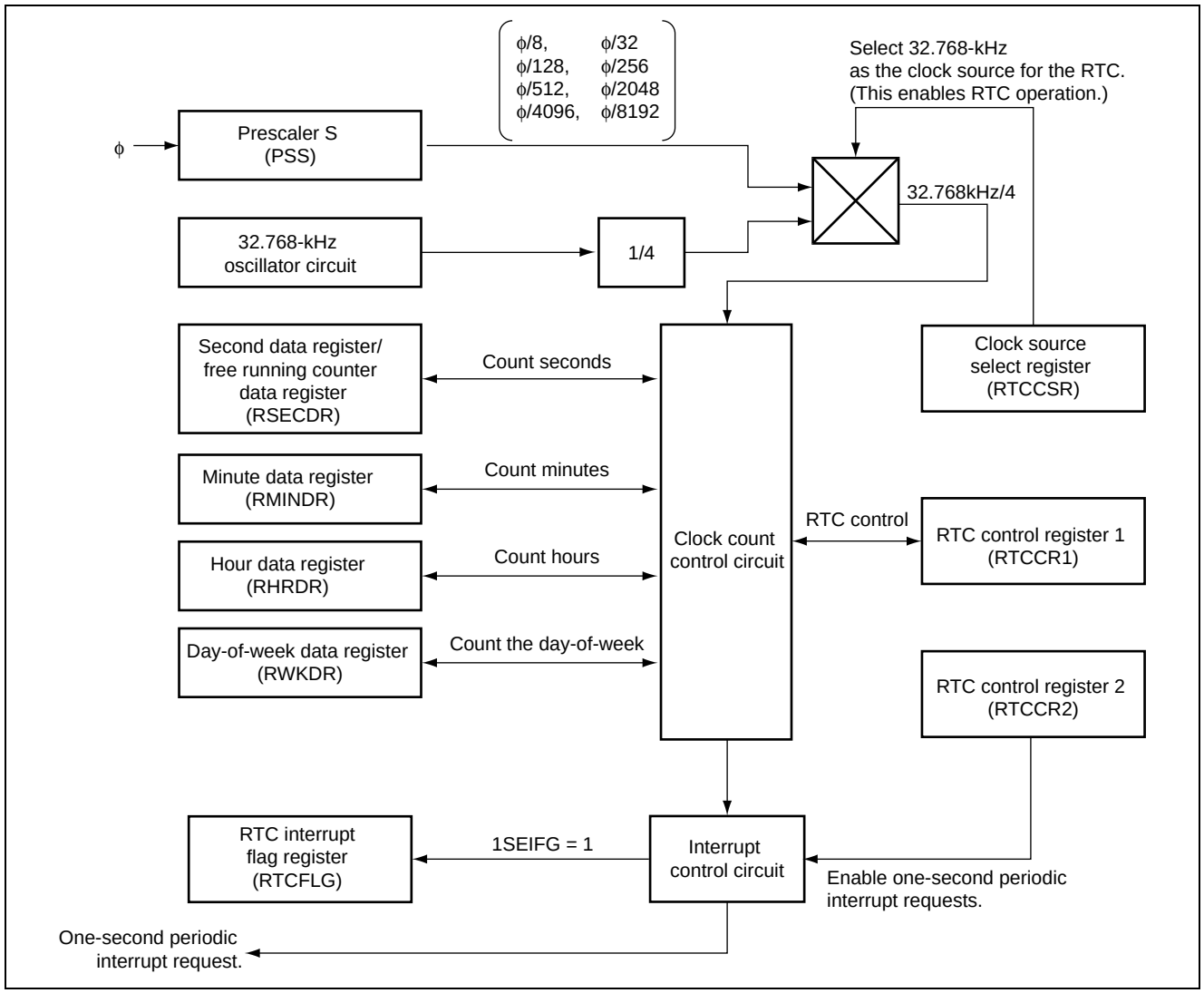


Figure 2 Block Diagram of RTC

2.1.2 Watchdog Timer Function

The H8/38602R includes a watchdog timer. The watchdog timer is active after reset. The timer counter WD (TCWD) is incremented and, if the TCWD overflows, the H8/38602R is internally reset. This sample task does not use the watchdog timer function, and thus stops this timer.

- Timer Control/Status Register WD1 (TCSRWD1)
  TCSRWD1 controls writing to TCSRWD1 and TCWD. TCSRWD1 also controls the watchdog timer operation and indicates the operating status. TCSRWD1 must be rewritten by using the MOV instruction. Bit manipulation instructions cannot be used to change the setting value.

2.1.3 Power-Down Mode (Watch Mode) Function

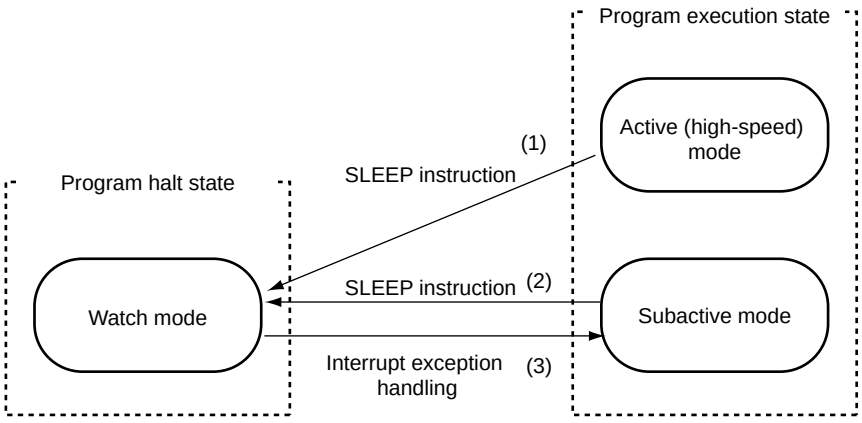
In watch mode, the system clock oscillator and CPU operation stop, and most of the on-chip peripheral modules stop functioning except the WDT, RTC, timer B1, asynchronous event counter, and the comparators. However, as long as the rated voltage is supplied, the contents of the CPU registers, some on-chip peripheral module registers, and on-chip RAM are retained. The I/O ports retain their state before the transition.

Watch mode is cleared by an interrupt. When an interrupt is requested, watch mode is cleared and interrupt exception handling starts. When watch mode is cleared by an interrupt, a transition is made to active (high-speed) mode, active (medium-speed) mode, or subactive mode depending on the settings of the LSON bit in SYSCR1 and the MSON bit in SYSCR2. When a transition is made to active mode, interrupt exception handling starts after the wait time set by the STS2 to STS0 bits in SYSCR1 has elapsed. Watch mode will not be cleared if the I bit in CCR is set to 1 or the requested interrupt is disabled by the interrupt enable register.

In this sample task, a transition is made from active (high-speed) mode to watch mode after a reset. The watch mode is cleared in response to a one-second periodic interrupt request from the RTC and subactive mode is entered. After the exception handling for the one-second periodic interrupt from the RTC is completed, a transition is made back to watch mode.

Figure 3 shows a mode transition block diagram for this sample task.

- System control register 1 (SYSCR1)
  SYSCR1 controls the power-down modes, in combination with SYSCR2.
- System control register 2 (SYSCR2)
  SYSCR2 controls the power-down modes, in combination with SYSCR1.



Conditions for SLEEP instruction execution

	LSON	MSON	SSBY	TMA3	DTON
(1)	x	x	1	1	0
(2)	x	x	1	1	0

Condition for clearing the mode by interrupt exception handling

	Interrupt sources
(3)	NMI, IRQ0, IRQ1, IRQAEC, COMP, RTC, WDT, AEC, and timer B1

Figure 3 Mode Transition Diagram

2.1.4 Exception Handling Function

In this sample task, watch mode is cleared by exception handling caused by the one-second periodic interrupt from the RTC, and the day, hour, minute and second data are stored to on-chip RAM.

- Interrupt Enable Register 1 (IENR1)
  IENR1 enables the RTC interrupts.

2.2 Assignment of Functions

Table 1 lists the function assignment for this sample task. By assigning the functions as shown in table 1, RTC operation is performed.

Table 1 Assignment of Functions

Register	Description
RSECDR	Second counting data
RMINDR	Minute counting data
RHRDR	Hour counting data
RWKDR	Day-of-week counting data
RTCCR1	Controls start/stop, operating mode, reset and interrupt generation timing of the RTC
RTCCR2	Enables one-second periodic interrupt requests.
RTCCSR	Sets the RTC clock source to 32.768 kHz.
RTCFLG	Register containing one-second periodic interrupt request flag
TCSRWD1	Stops the watchdog timer.
SYSCR1	Controls direct transition to subactive mode, in combination with SYSCR2.
SYSCR2	Controls direct transition to subactive mode, in combination with SYSCR1.
IENR1	Enables RTC interrupt requests.

3. Principles of Operation

This sample task performs RTC operation. After the initial settings have been made, a mode transition is made to watch mode, and then to subactive mode in response to a one-second periodic interrupt request from the RTC. The day, hour, minute and second data are read and stored in on-chip RAM, after which a transition is made back to watch mode. The subclock is generated by the subclock oscillator circuit that uses a 32.768-kHz crystal resonator. The RTC operation is explained below.

3.1 RTC Initial Setting Procedure

Figure 4 shows the procedure for the initial setting of the RTC.

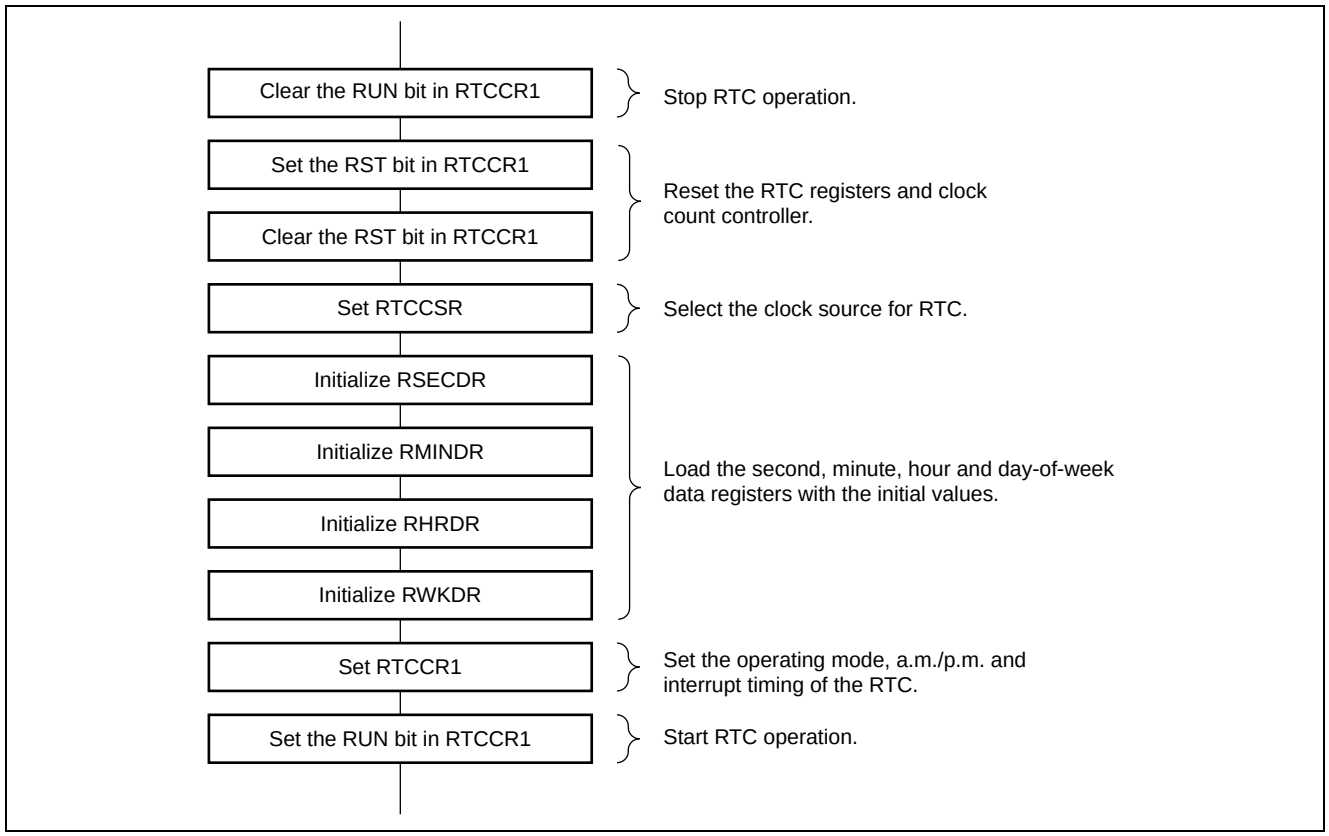


Figure 4 RTC Initial Setting Procedure

3.2 Time Data Reading Procedure

If the seconds, minutes, hours, or day-of-week data are updated while the time data is being read, the data obtained may not be correct, and thus the time data must be read again. Figure 5 shows an example in which correct data is not obtained. In this example, since only RSECDR is read after data update, about 1-minute inconsistency results.

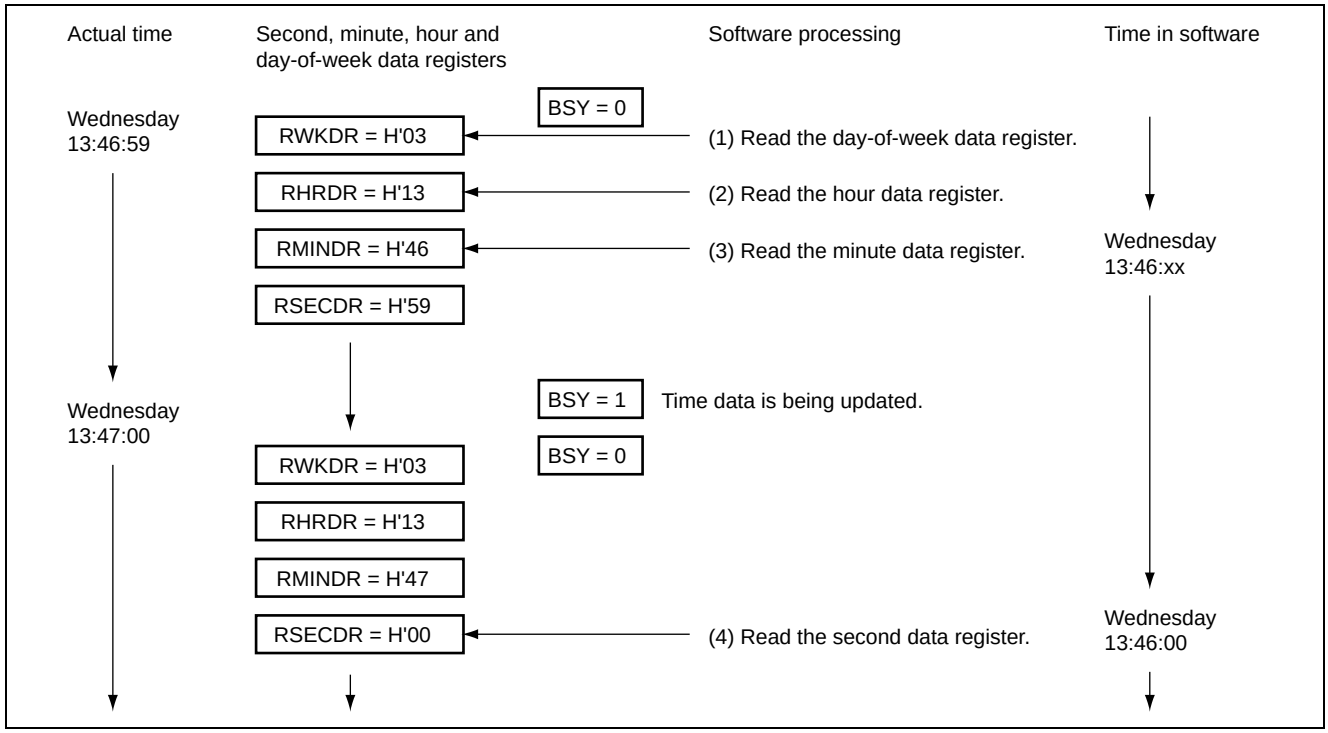


Figure 5 Example Case when Inaccurate Time Data are Read

To avoid reading inaccurate time data, the following three methods are available:

- Check the BSY bit, and after the BSY bit has changed from 1 to 0, read the second, minute, hour, and day-of-week registers. The register values are updated about 62.5 ms after the BSY bit is set to 1, and the BSY bit is cleared to 0.
- Making use of the interrupts, read the second, minute, hour, and day-of-week registers after the relevant flag in RTCFLG is set to 1 and the BSY bit is confirmed to be 0.
- Read the second, minute, hour, and day-of-week registers twice in a row, and if there is no change in the read data, the read data is used.

3.3 INT Bit

The INT bit in RTCCR1 can be used to control interrupt generation timing. When interrupts are used to read accurate time data as described in the second method above, the procedure of reading the second, minute, hour and day-of-week data registers differs according to the INT bit setting. Figure 6 shows how the INT bit is used. In this sample task, the INT bit is set to 1.

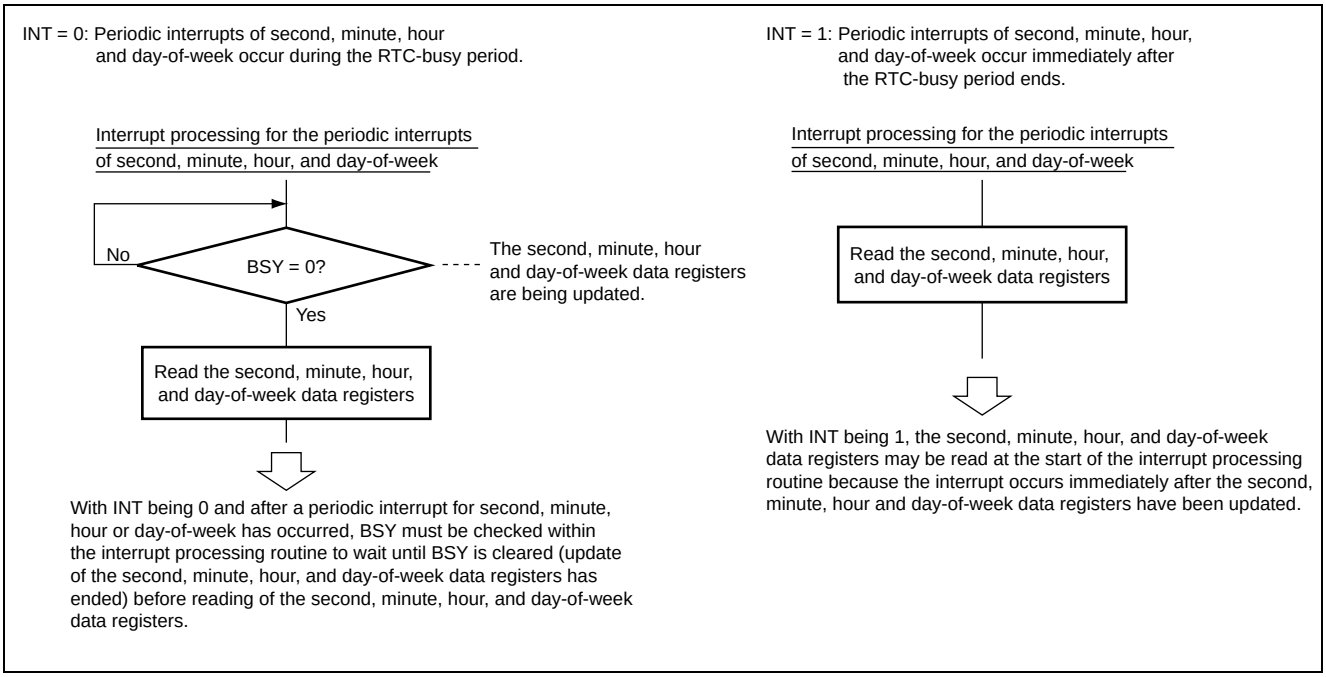


Figure 6 Usage of INT Bit

4. Description of Software

4.1 Modules

Table 2 describes the modules used in this sample task.

Table 2 Description of Modules

Function Name	Description
main	Stops the watchdog timer, sets initial values for the RTC, enables interrupts, and makes a transition to watch mode.
int_rtc	One-second periodic interrupt processing that stores the second, minute, hour and day-of-week data in on-chip RAM

4.2 Arguments

This sample program does not use arguments.

4.3 Internal Registers Used

The following describes the internal registers used in this sample task.

- Second Data Register/Free Running Counter Data Register (RSECDR) Address H'F068

Bit	Bit Name	Setting	R/W	Function
7	BSY	0	R	RTC Busy This bit is set to 1 when the RTC is updating (computing) the values of second, minute, hour, and day-of-week data registers. The values of the second, minute, hour, and day-of-week data registers must be used while this bit is 0.
6	SC12	0	R/W	Ten's Position of Seconds
5	SC11	0	R/W	The value of these bits is incremented from 0 to 5 to count 60
4	SC10	0	R/W	seconds.
3	SC03	0	R/W	One's Position of Seconds
2	SC02	0	R/W	The value of these bits is incremented every second from 0 to 9.
1	SC01	0	R/W	When there is a carry, the ten's position is incremented by 1.
0	SC00	0	R/W	

- Minute Data Register (RMINDR) Address H'F069

Bit	Bit Name	Setting	R/W	Function
7	BSY	0	R	RTC Busy This bit is set to 1 when the RTC is updating (computing) the values of second, minute, hour, and day-of-week data registers. The values of the second, minute, hour, and day-of-week data registers must be used while this bit is 0.
6	MN12	0	R/W	Ten's Position of Minutes
5	MN11	0	R/W	The value of these bits is incremented from 0 to 5 to count 60
4	MN10	0	R/W	minutes.
3	MN03	0	R/W	One's Position of Minutes
2	MN02	0	R/W	The value of these bits is incremented every minute from 0 to 9.
1	MN01	0	R/W	When there is a carry, the ten's position is incremented by 1.
0	MN00	0	R/W	

- Hour Data Register (RHRDR) Address H'F06A

Bit	Bit Name	Setting	R/W	Function
7	BSY	0	R	RTC Busy This bit is set to 1 when the RTC is updating (computing) the values of second, minute, hour, and day-of-week data registers. The values of the second, minute, hour, and day-of-week data registers must be used while this bit is 0.
5	HR11	0	R/W	Ten's Position of Hours
4	HR10	0	R/W	The value of these bits is incremented from 0 to 2.
3	HR03	0	R/W	One's Position of Hours
2	HR02	0	R/W	The value of these bits is incremented every hour from 0 to 9. When
1	HR01	0	R/W	there is a carry, the ten's position is incremented by 1.
0	HR00	0	R/W	

- Day-of-Week Data Register (RWKDR) Address H'F06B

Bit	Bit Name	Setting	R/W	Function
7	BSY	0	R	RTC Busy This bit is set to 1 when the RTC is updating (computing) the values of second, minute, hour, and day-of-week data registers. The values of the second, minute, hour, and day-of-week data registers must be used while this bit is 0.
2	WK2	0	R/W	Day-of-Week Count
1	WK1	0	R/W	These bits indicate a day-of-week in binary code.
0	WK0	0	R/W	000: Sunday 001: Monday 010: Tuesday 011: Wednesday 100: Thursday 101: Friday 110: Saturday 111: Reserved (setting prohibited)

- RTC Control Register 1 (RTCCR1) Address H'F06C

Bit	Bit Name	Setting	R/W	Function
7	RUN	1	R/W	RTC Operation Start 0: Stops RTC operation 1: Starts RTC operation
6	12/24	1	R/W	Operating Mode 0: RTC operates in 12-hour mode. Incrementation of RHRDR is from 0 to 11. 1: RTC operates in 24-hour mode. Incrementation of RHRDR is from 0 to 23.
4	RST	0	R/W	Reset 0: Normal operation 1: Resets all the registers and control circuits of the RTC except RTCCSR and this bit. This bit must be cleared to 0 after set to 1.
3	INT	1	R/W	Interrupt Generation Timing 0: Periodic interrupts of second, minute, hour, and day-of-week are generated during the RTC busy period. 1: Periodic interrupts of second, minute, hour, and day-of-week are generated immediately after the RTC busy period ends.

- RTC Control Register 2 (RTCCR2) Address H'F06D

Bit	Bit Name	Setting	R/W	Function
2	1SEIE	1	R/W	One-Second Periodic Interrupt Enable 0: Disables one-second periodic interrupts. 1: Enables one-second periodic interrupts.

- Clock Source Select Register (RTCCSR) Address H'F06F

Bit	Bit Name	Setting	R/W	Function
3	RCS3	1	R/W	Clock Source Selection
2	RCS2	0	R/W	0000: ϕ/8 (Free running counter operation)
1	RCS1	0	R/W	0001: ϕ/32 (Free running counter operation)
0	RCS0	0	R/W	0010: ϕ/128 (Free running counter operation)
				0011: ϕ/256 (Free running counter operation)
				0100: ϕ/512 (Free running counter operation)
				0101: ϕ/2048 (Free running counter operation)
				0110: ϕ/4096 (Free running counter operation)
				0111: ϕ/8192 (Free running counter operation)
				1xxx: 32.768 kHz (RTC operation)

[Legend] x: Don't care.

- RTC Interrupt Flag Register (RTCFLG) Address H'F067

Bit	Bit Name	Setting	R/W	Function
2	1SEIFG	0	R/(W)*	[Setting condition]
				When a one-second periodic interrupt occurs
				[Clearing condition]
				0 is written to 1SEIFG when 1SEIFG = 1

Note: * Only 0 can be written to clear the flag.

- Timer Control/Status Register WD1 (TCSRWD1) Address H'FFB1

Bit	Bit Name	Setting	R/W	Function
7	B6WI	1	R/W	Bit 6 Write Disable Writing to the TCWE bit is only enabled when 0 is written to the B6WI bit. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable Writing to the timer counter WD (TCWD) is enabled when the TCWE bit is set to 1. When writing to this bit, 0 must be written to the B6WI bit.
5	B4WI	1	R/W	Bit 4 Write Disable Writing to the TCSRWE bit is only enabled when 0 is written to the B4MI bit. The B4WI bit is always read as 1.
4	TCSRWE	0	R/W	Timer Control/Status Register WD1 Write Enable Writing to the WDON and WRST bits are enabled when the TCSRWE bit is set to 1. When writing to this bit, 0 must be written to the B4WI bit.
3	B2WI	1	R/W	Bit 2 Write Disable Writing to the WDON is only enabled when 0 is written to the B2WI bit. This bit is always read as 1.

Bit	Bit Name	Setting	R/W	Function
2	WDON	0	R/W	Watchdog Timer On The TDWD starts counting up when the WDON bit is set to 1 and stops counting when the WDON bit is cleared to 0. [Setting condition] • If 0 is written to the B2WI bit and 1 to the WDON bit while the TCSRWE bit is 1. • Reset [Clearing condition] • If 0 is written to the B2WI and WDON bits while the TCSRWE bit is 1.
1	B0WI	1	R/W	Bit 0 Write Disable Writing to the WRST bit is only enabled when 0 is written to the B0WI bit. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] • When the TCWD overflows and an internal reset signal is generated. [Clearing condition] • Reset by the $\overline{\text{RES}}$ pin • If 0 is written to both the BOWI and WRST bits while the TCSRWE bit is 1.

- System Control Register 1 (SYSCR1) Address H'FFF0

Bit	Bit Name	Setting	R/W	Function
7	SSBY	1	R/W	Software Standby Selects the mode to which the transition is made after the SLEEP instruction is executed. 0: Transition is made to sleep mode or subsleep mode. 1: Transition is made to standby mode or watch mode.
3	LSON	1	R/W	Low Speed on Flag Selects the system clock (ϕ) or subclock (ϕSUB) as the CPU operating clock after watch mode is cleared. 0: The CPU operates on the system clock (ϕ) 1: The CPU operates on the subclock (ϕSUB)
2	TMA3	1	R/W	Selects the mode to which the transition is made after the SLEEP instruction is executed, in combination with bits SSBY and LSON in SYSCR1 and bits DTON and MSON in SYSCR2.

- System Control Register 2 (SYSCR2) Address H'FFF1

Bit	Bit Name	Setting	R/W	Function
3	DTON	0	R/W	Direct Transfer ON Flag Selects the mode to which the transition is made after the SLEEP instruction is executed, in combination with bits SSBY, TMA3, and LSON in SYSCR1 and bit MSON in SYSCR2.
2	MSON	0	R/W	Medium Speed ON Flag Selects whether the chip operates in active (high-speed) or active (medium-speed) mode after standby, watch, or sleep mode is cleared. 0: Active (high-speed) mode 1: Active (medium-speed) mode
1	SA1	0	R/W	Subactive Mode Clock Select 1 and 0
0	SA0	0	R/W	These bits select the operating clock frequency in subactive and subsleep modes. The operating clock frequency changes to the set frequency after the SLEEP instruction is executed. 00: ϕw/8 01: ϕw/4 10: ϕw/2 11: ϕw

- Interrupt Enable Register 1 (IENR1) Address H'FFF3

Bit	Bit Name	Setting	R/W	Function
7	IENRTC	1	R/W	RTC Interrupt Request Enable RTC interrupt requests are enabled when this bit is set to 1.

4.4 RAM Usage

Table 3 describes the RAM usage in this sample task.

Table 3 Description of RAM

Label Name	Function	Size	Used In
sec_cnt	Stores BCD-coded second data	1 byte	main, int_rtc
min_cnt	Stores BCD-coded minute data	1 byte	main, int_rtc
hr_cnt	Stores BCD-coded hour data	1 byte	main, int_rtc
wk_cnt	Stores binary-coded day-of-week data	1 byte	main, int_rtc

- Second Data (sec_cnt) Address H'FB80

Bit	Bit Name	Initial Value	Function
7	—	0	Not used
6	sec_12	0	Ten's Position of Seconds
5	sec_11	0	The value of these bits is incremented from 0 to 5 to count 60
4	sec_10	0	seconds.
3	sec_03	0	One's Position of Seconds
2	sec_02	0	The value of these bits is incremented every second from 0 to 9.
1	sec_01	0	When there is a carry, the ten's position is incremented by 1.
0	sec_00	0	

- Minute Data (min_cnt) Address H'FB81

Bit	Bit Name	Initial Value	Function
7	—	0	Not used
6	min_12	0	Ten's Position of Minutes
5	min_11	0	The value of these bits is incremented from 0 to 5 to count 60
4	min_10	0	minutes.
3	min_03	0	One's Position of Minutes
2	min_02	0	The value of these bits is incremented every minute from 0 to 9.
1	min_01	0	When there is a carry, the ten's position is incremented by 1.
0	min_00	0	

- Hour Data (hr_cnt) Address H'FB82

Bit	Bit Name	Initial Value	Function
7	—	0	Not used
6	—	0	Not used
5	hr_11	0	Ten's Position of Hours
4	hr_10	0	The value of these bits is incremented from 0 to 2.
3	hr_03	0	One's Position of Hours
2	hr_02	0	The value of these bits is incremented every hour from 0 to 9. When
1	hr_01	0	there is a carry, the ten's position is incremented by 1.
0	hr_00	0	

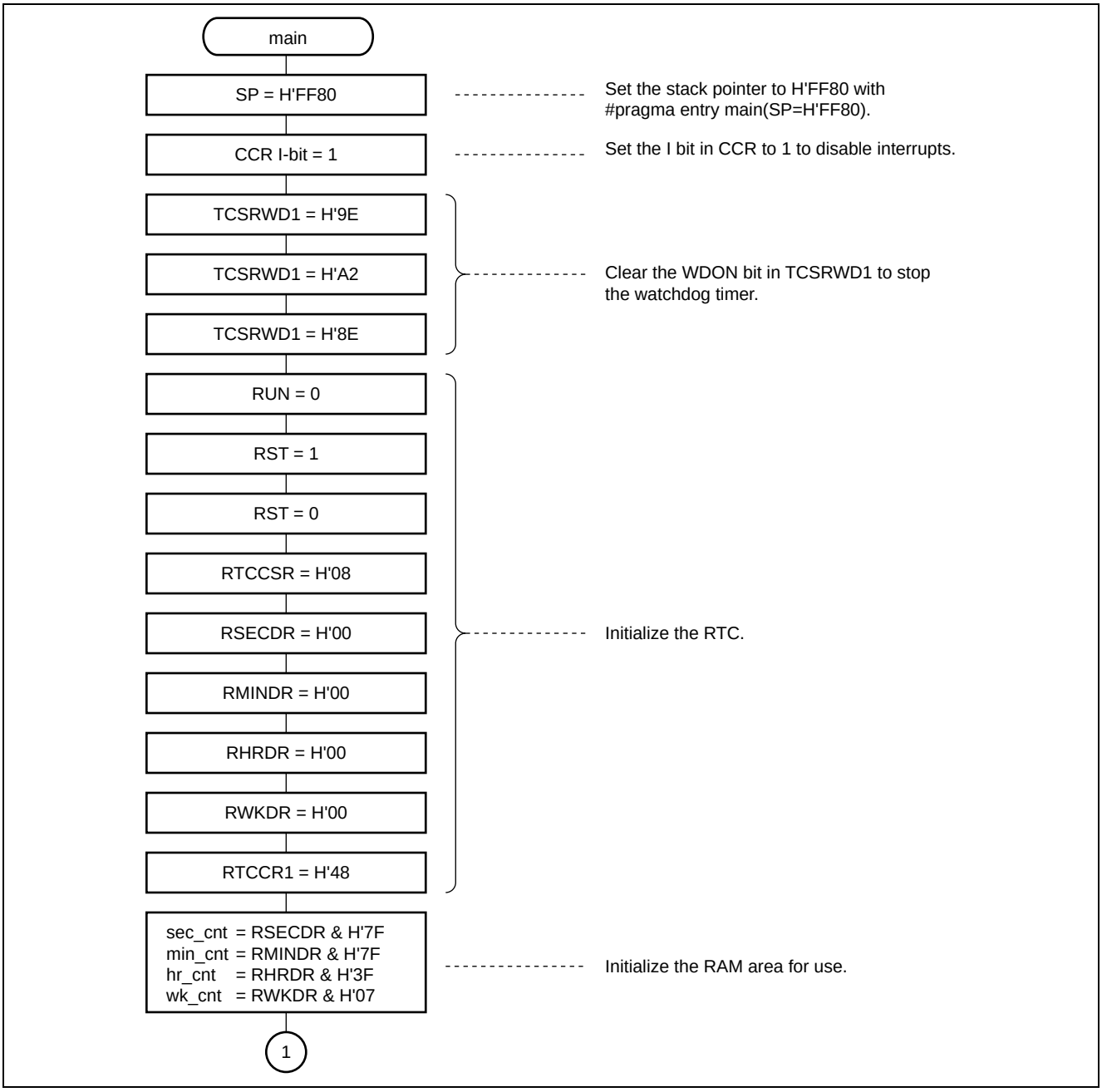
Note: Hour data (hr_cnt) is indicated in 24-hour mode in this sample task.

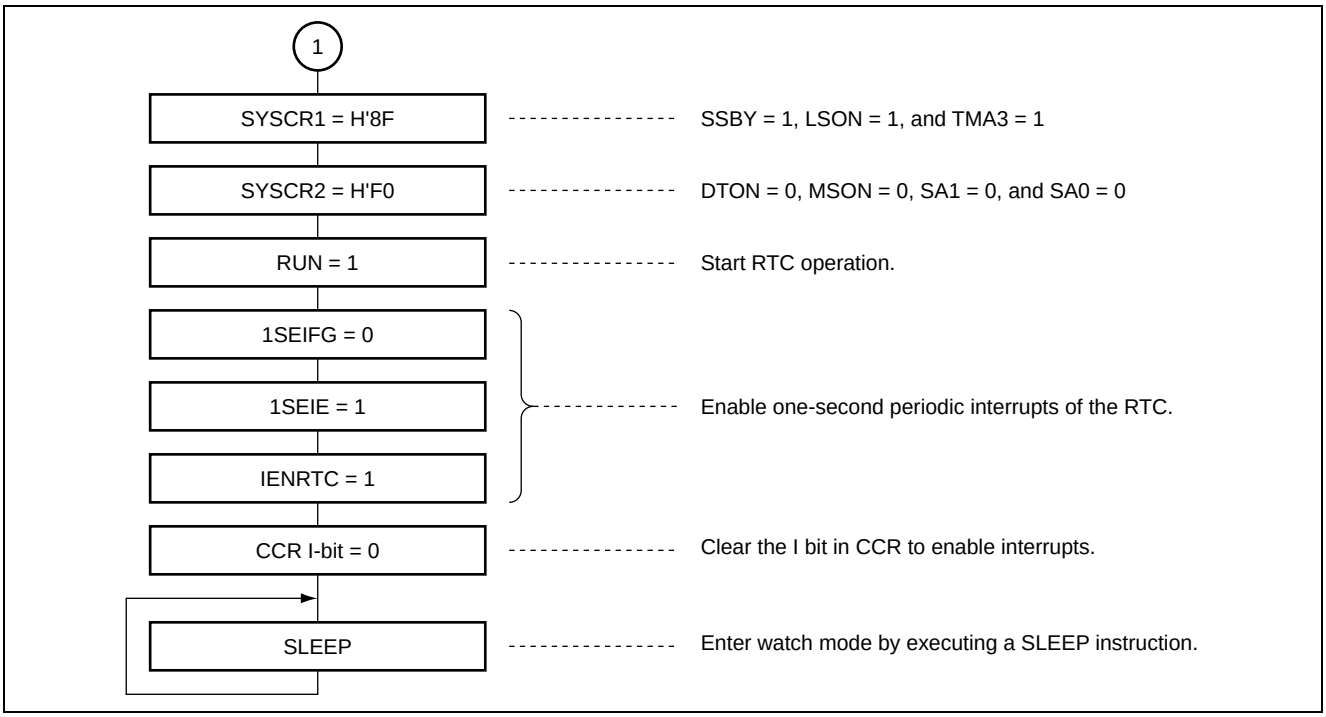
- Day-of-Week Data (wk_cnt) Address H'FB82

Bit	Bit Name	Initial Value	Function
7	—	0	Not used
6	—	0	Not used
5	—	0	Not used
4	—	0	Not used
3	—	0	Not used
2	wk_02	0	Day-of-Week Count
1	wk_01	0	These bits indicate a day-of-week in binary code.
0	wk_00	0	000: Sunday 001: Monday 010: Tuesday 011: Wednesday 100: Thursday 101: Friday 110: Saturday

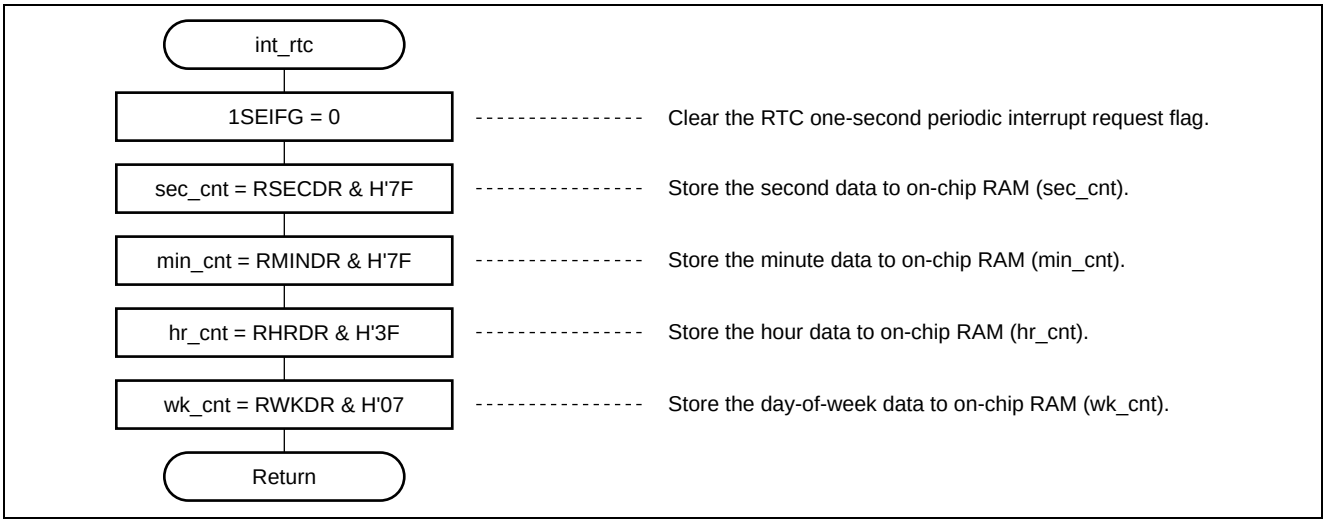
5. Flowchart

5.1 main





5.2 int_rtc



5.3 Link Address Specification

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'FB80

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.05	—	First edition issued

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