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H8/38602R Group

Voltage Comparison by Comparator (External Voltage Reference)

Introduction

The H8/38602R's comparator function is used to compare the voltage applied to the comparator analog input pin 0 (pin COMP0) with a reference voltage input from the VCref pin.

Target Device

H8/38602R

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1. Specifications

- A reference voltage is input from the VCref pin.
- The voltage input to the COMP0 pin is compared with the reference voltage by using the comparator function.
- The result of voltage comparison is stored to RAM. The value 0 indicates that COMP0 pin voltage ≤ reference voltage, and 1 indicates that COMP0 pin voltage > reference voltage.

Figure 1 shows the connection for this sample task.

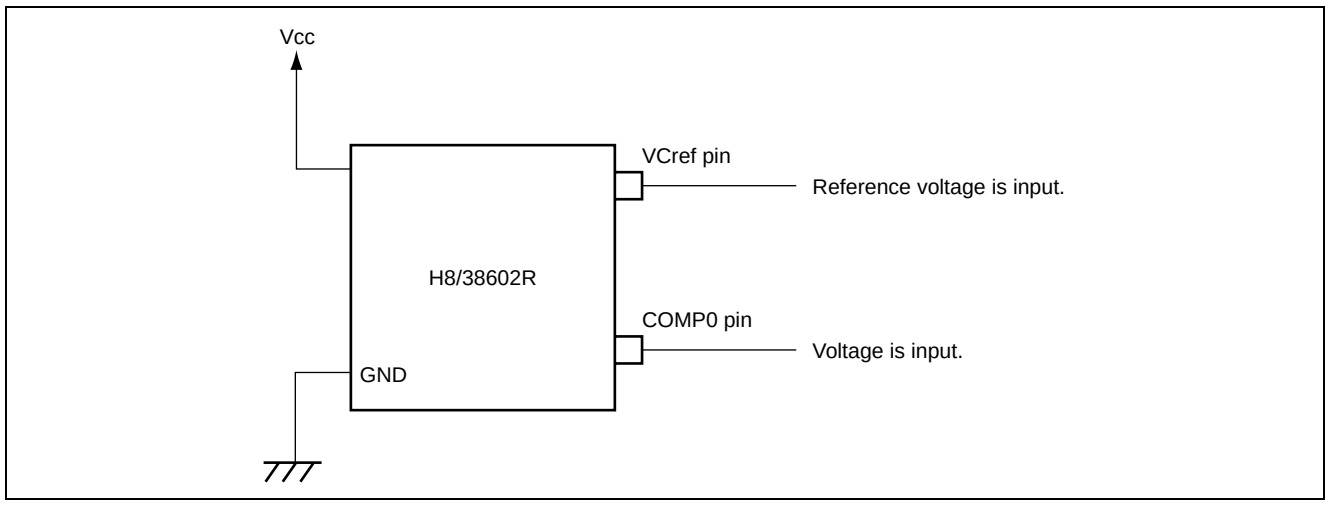


Figure 1 Connection Diagram

2. Description of Functions

2.1 Functions

In this sample task, a reference voltage is provided from the VCref pin. A voltage applied to the COMP0 pin is compared with the reference voltage using the comparator function. Figure 2 shows a block diagram of the comparators,and below is the explanation of the MCU's functions used in this sample task.

2.1.1 Comparator Function

A voltage applied to the VCref pin is specified as the reference voltage, and a voltage input to the COMP0 pin is compared with the reference voltage.

- Compare Control Register 0 (CMCR0)
  CMCR0 controls the comparator.
- Compare Data Register (CMDR)
  CMDR stores the result of comparing the voltage on the analog input pin with the reference voltage.

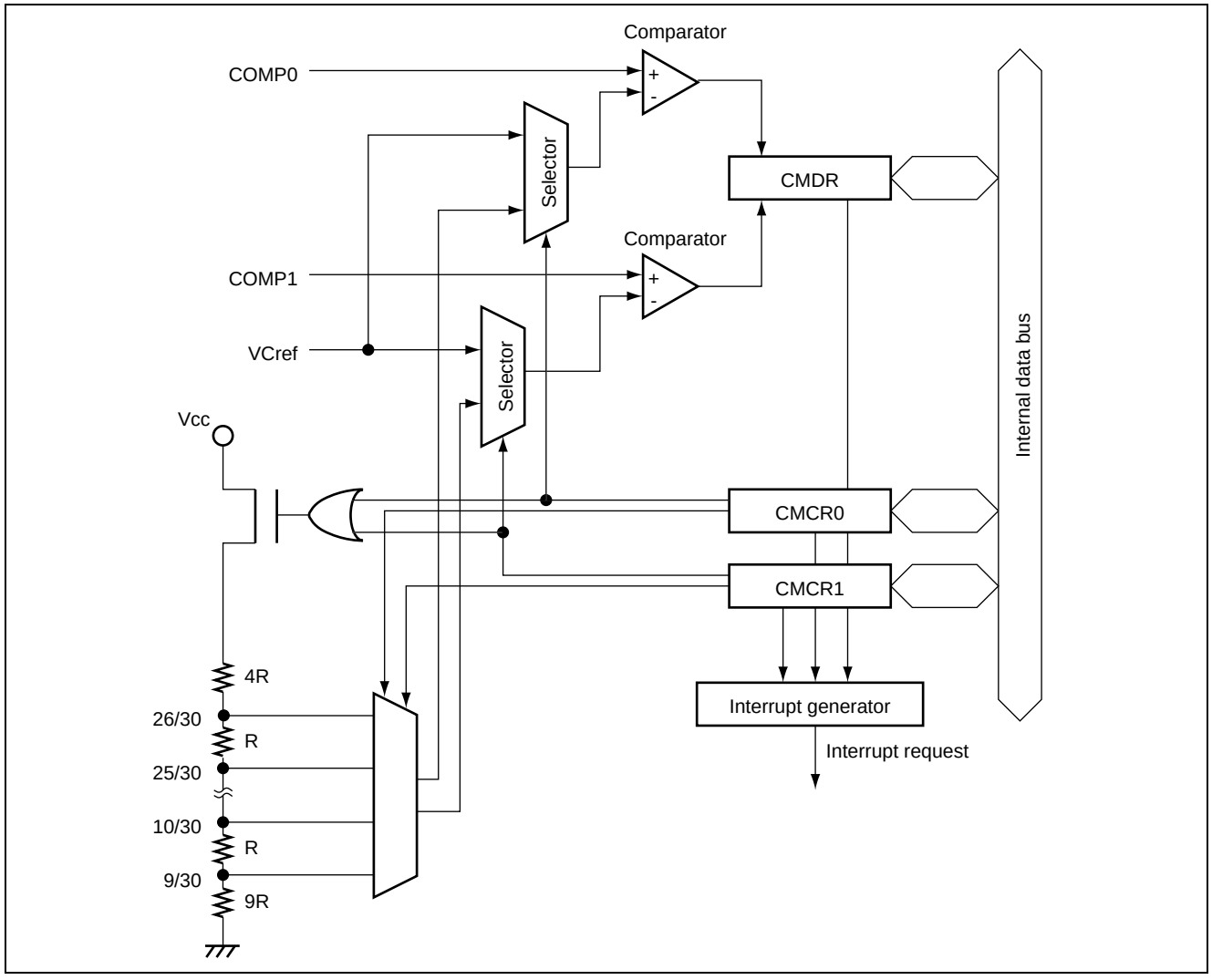


Figure 2 Block Diagram of Comparator Function

2.1.2 Watchdog Timer Function

The H8/38602R includes a watchdog timer, which is active after a reset. The timer counter WD (TCWD) counts up, and the H8/38602R is internally reset if the TCWD overflows. This sample task does not use the watchdog timer function, and thus stops this timer.

- Timer Control/Status Register WD1 (TCSRWD1)
  TCSRWD1 controls writing to TCSRWD1 and TCWD. TCSRWD1 also controls the watchdog timer operation and indicates the operating status. TCSRWD1 must be rewritten by using the MOV instruction. The setting value cannot be changed by bit manipulation instructions.

2.1.3 I/O Port Function

The function of the port 30 pin is set as the VCref pin.

- Port Mode Register 3 (PMR3)
  PMR3 selects the functions for port 3 pins.

2.1.4 Module Standby Function

By the module standby function, the comparators are placed in module standby mode after a reset. Module standby mode of the comparators can be cancelled by setting the COMPCKSTP bit in Clock Halt Register 2 (CKSTPR2) to 1.

- Clock Halt Register 2 (CKSTPR2)
  CKSTPR2 controls the standby state of the on-chip peripheral modules in module units.

2.2 Function Assignment

Table 1 lists the function assignment for this sample task. By assigning the functions as shown in table 1, the voltage input to the COMP0 pin is compared with the reference voltage from the VCref pin using the comparator function.

Table 1 Assignment of Functions

Elements	Description
COMP0	Enables the comparator and specifies the voltage input from the VCref pin as a reference voltage.
CMDR	Stores the result of comparing the COMP0 pin voltage with the reference voltage.
PMR3	Sets the P30 pin to function as the VCref pin.
CKSTPR2	Cancels the comparator module standby state.
TCSRWD1	Stops the watchdog timer.

3. Description of Operation

Figure 3 illustrates the operation of this sample task along with the hardware and software processing. The voltage input to the COMP0 is compared with the VCref pin voltage using the comparator function.

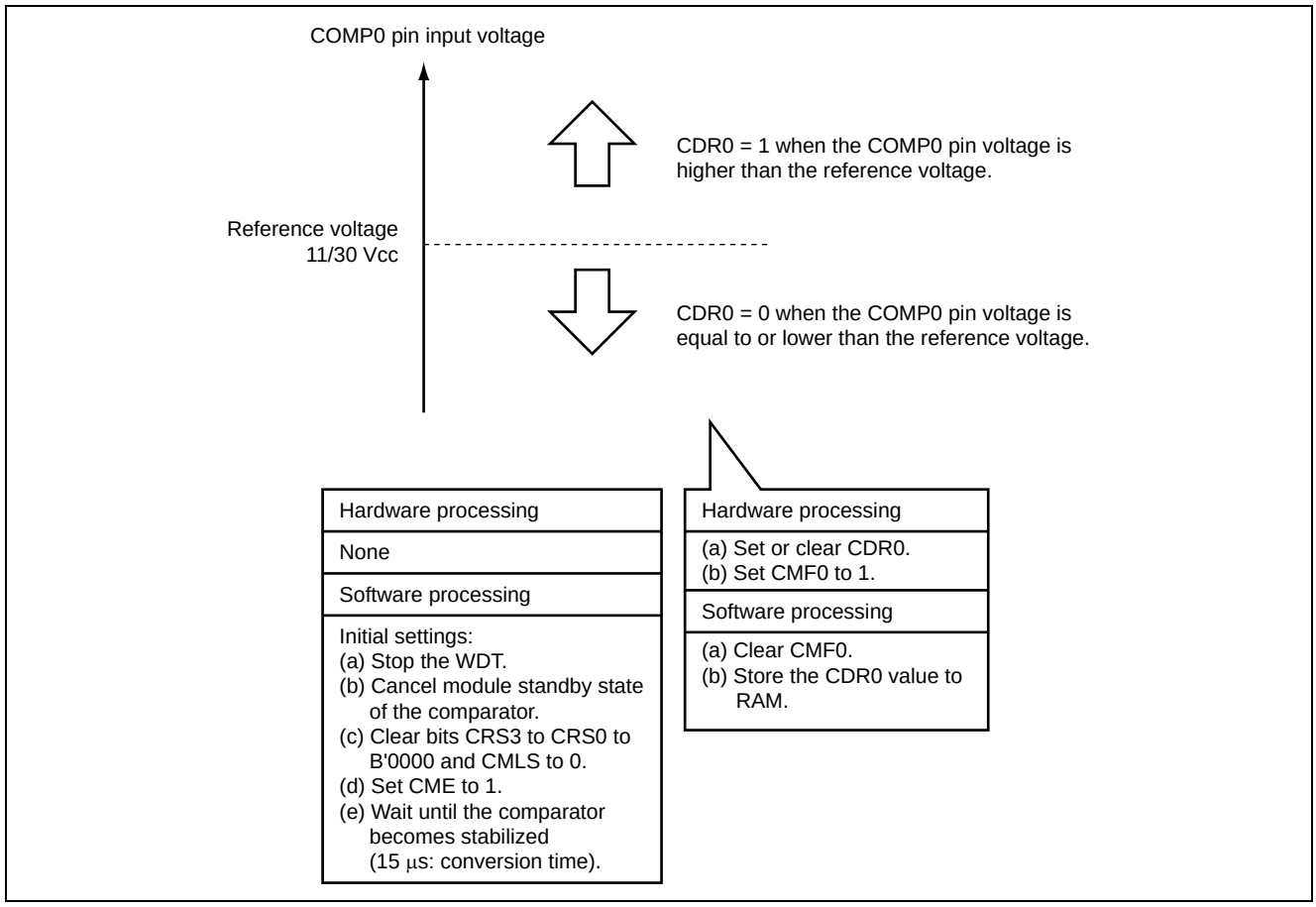


Figure 3 Comparison Operation

4. Description of Software

4.1 Module

Table 2 describes the module of this sample task.

Table 2 Description of Module

Function Name	Description
main	Stops the watchdog timer, cancels the comparator module standby state and configures the comparator.

4.2 Arguments

This sample program does not use arguments.

4.3 Internal Registers

The following describes internal registers used in this sample task.

- Compare Control Register 0 (CMCR0) Address H'F0DC

Bit	Bit Name	Setting	R/W	Function
7	CME	1	R/W	Comparator Enable 0: Comparator halted. 1: Comparator operates.
5	CMR	1	R/W	Comparator Reference Voltage Select 0: Selects internal power supply as the reference voltage. 1: Reference voltage is input from the VCref pin. For the combination of the CMR and CMLS bits, see table 3.
4	CMLS	0 (Default)	R/W	Comparator Hysteresis Select 0: Selects no hysteresis 1: Selects hysteresis When CMR = 1, clear this bit to 0. For the combination of the CMR and CMLS bits, see table 3.

Table 3 Combination of CMR and CMLS Bits

CMR	CMLS	Function
0	0	The internal power supply (the voltage, VIH, set by the CRS3 to CRS0 bits in CMCR) and the COMP pin voltage are compared. No hysteresis.
	1	The internal power supply and the COMP pin voltage are compared. With hysteresis. VIH and VIL are set by the CRS3 to CRS0 bits.
1	0	VCref and COMP pin voltages are compared. No hysteresis.
	1	Setting prohibited

- Compare Data Register (CMDR) Address H'F0DE

Bit	Bit Name	Setting	R/W	Function
4	CMF0	—	R/(W)*	COMP0 Interrupt Flag [Setting condition] When COMP0 interrupt occurs [Clearing condition] 0 is written to CMF0 after reading CMF0 = 1
0	CDR0	—	R	[Setting condition] COMP0 pin > Reference voltage [Clearing condition] COMP0 pin ≤ Reference voltage

Note: Only 0 can be written to clear the flag.

- Port Mode Register 3 (PMR3) Address H'FFC2

Bit	Bit Name	Setting	R/W	Function
0	VCref	1	R/W	P30/SCK3/VCref Pin Function Switch 0: P30 or SCK3 I/O pin 1: Comparator reference voltage (VCref) pin

- Timer Control/Status Register WD1 (TCSRWD1) Address H'FFB1

Bit	Bit Name	Setting	R/W	Function
7	B6WI	1	R/W	Bit 6 Write Disable Writing to the TCWE bit is only enabled when 0 is written to the B6WI bit. This bit is always read as 1.
6	TCWE	0	R/W	Timer Counter WD Write Enable Writing to the timer counter WD (TCWD) is enabled when the TCWE bit is set to 1. When writing to this bit, 0 must be written to the B6WI bit.
5	B4WI	1	R/W	Bit 4 Write Disable Writing to the TCSRWE bit is only enabled when 0 is written to the B4MI bit. The B4WI bit is always read as 1.
4	TCSRWE	0	R/W	Timer Control/Status Register WD1 Write Enable Writing to the WDON and WRST bits are enabled when the TCSRWE bit is set to 1. When writing to this bit, 0 must be written to the B4WI bit.
3	B2WI	1	R/W	Bit 2 Write Disable Writing to the WDON is only enabled when 0 is written to the B2WI bit. This bit is always read as 1.

Bit	Bit Name	Setting	R/W	Function
2	WDON	0	R/W	Watchdog Timer On The TDWD starts counting up when the WDON bit is set to 1 and stops counting when the WDON bit is cleared to 0. [Setting condition] • If 0 is written to the B2WI bit and 1 to the WDON bit while the TCSRWE bit is 1. • Reset [Clearing condition] • If 0 is written to the B2WI and WDON bits while the TCSRWE bit is 1.
1	B0WI	1	R/W	Bit 0 Write Disable Writing to the WRST bit is only enabled when 0 is written to the B0WI bit. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Setting condition] • When the TCWD overflows and an internal reset signal is generated. [Clearing condition] • Reset by the $\overline{\text{RES}}$ pin • If 0 is written to both the BOWI and WRST bits while the TCSRWE bit is 1.

- Clock Halt Register 2 (CKSTPR2) Address H'FFFB

Bit	Bit Name	Setting	R/W	Function
1	COMPCKSTP	1	R/W	Comparator Module Standby The comparators enter a standby state when this bit is cleared to 0. 1: Cancels module standby state.

4.4 RAM Usage

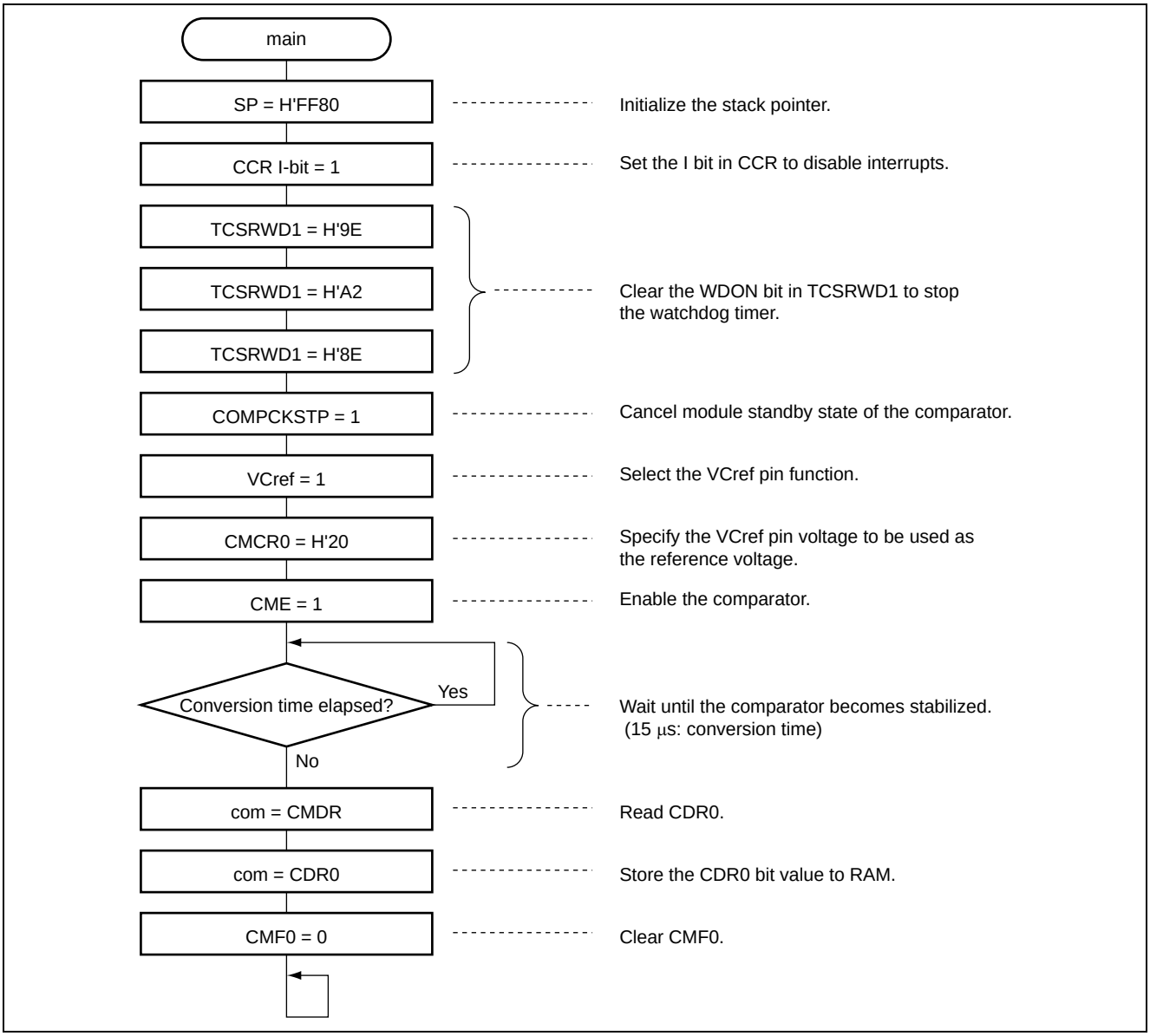
Table 4 describes the RAM usage in this sample task.

Table 4 Description of RAM

Label Name	Function	Data Length	Used In
com	Stores the result of comparing the VCref and COMP0 pin voltages.	One byte	main

5. Flowchart

5.1 main



5.2 Link Address Specification

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'FB80

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.05	—	First edition issued

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